NXP USA Inc. - MPC8248CZQPIEA Datasheet

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	300MHz
Co-Processors/DSP	Communications; RISC CPM, Security; SEC
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8248czqpiea

This figure shows the block diagram of the SoC.

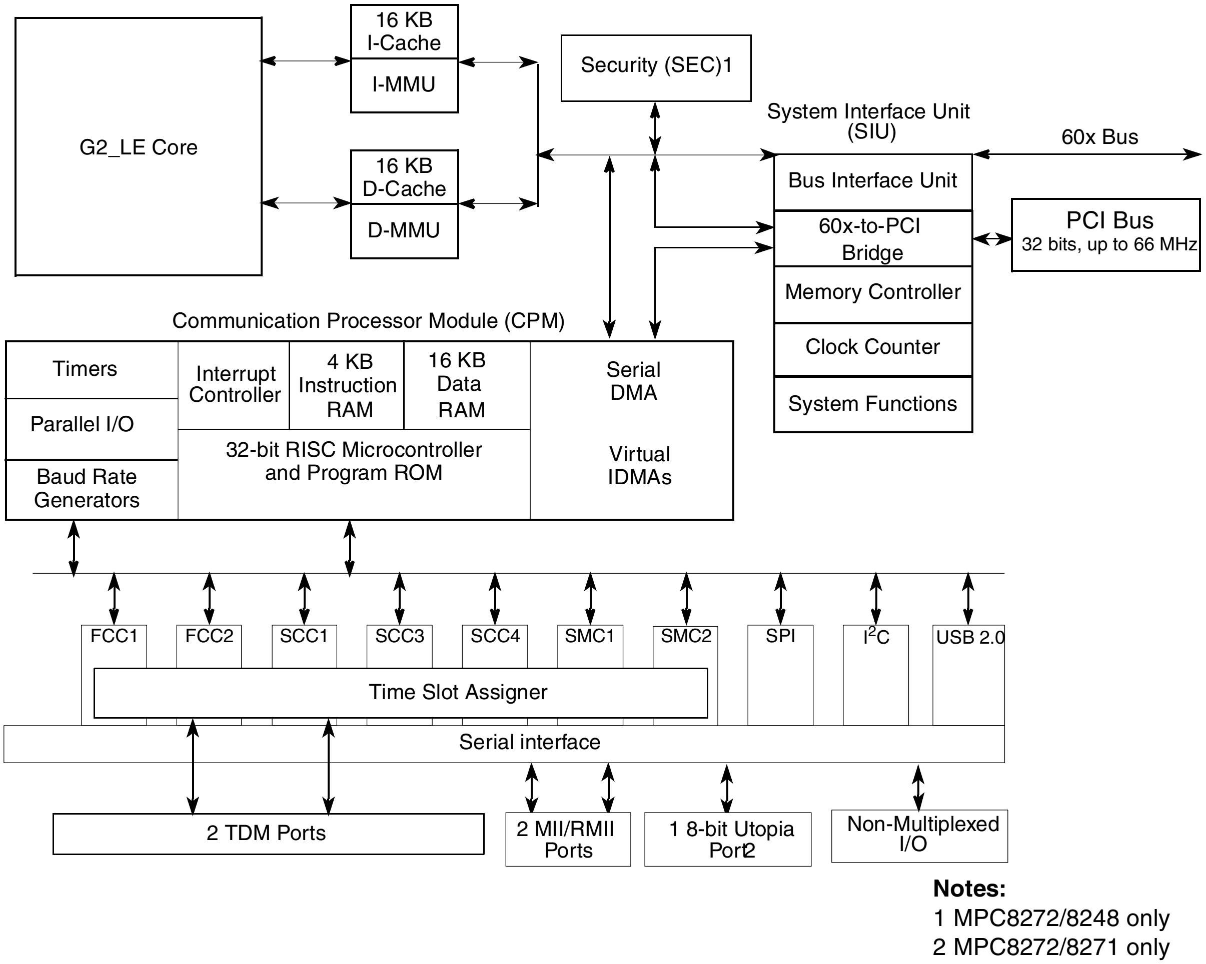


Figure 1. SoC Block Diagram

1.1 Features

The major features of the SoC are as follows:

- Dual-issue integer (G2_LE) core
  - A core version of the MPC603e microprocessor
  - System core microprocessor supporting frequencies of 266–400 MHz
  - Separate 16 KB data and instruction caches:
    - Four-way set associative
    - Physically addressed
    - LRU replacement algorithm
  - Power Architecture®-compliant memory management unit (MMU)
  - Common on-chip processor (COP) test interface
  - Supports bus snooping for cache coherency

This table lists recommended operational voltage conditions.

Table 4. Recommended Operating Conditions[1]

Rating	Symbol	Value	Unit
Core supply voltage	VDD	1.425 – 575	V
PLL supply voltage	VCCSYN	1.425 – 575	V
I/O supply voltage	VDDH	3.135 – 3.465	V
Input voltage	VIN	GND (–0.3) – 3.465	V
Junction temperature (maximum)	T_j	105[2]	°C
Ambient temperature	T_A	0–70[2]	°C

[1] **Caution:** These are the recommended and tested operating conditions. Proper operation outside of these conditions is not guaranteed.

[2] Note that for extended temperature parts the range is (-40)$_{T_A}$– 105$_{T_j}$.

This SoC contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

This figure shows the undershoot and overshoot voltage of the 60x bus memory interface of the SoC. Note that in PCI mode the I/O interface is different.

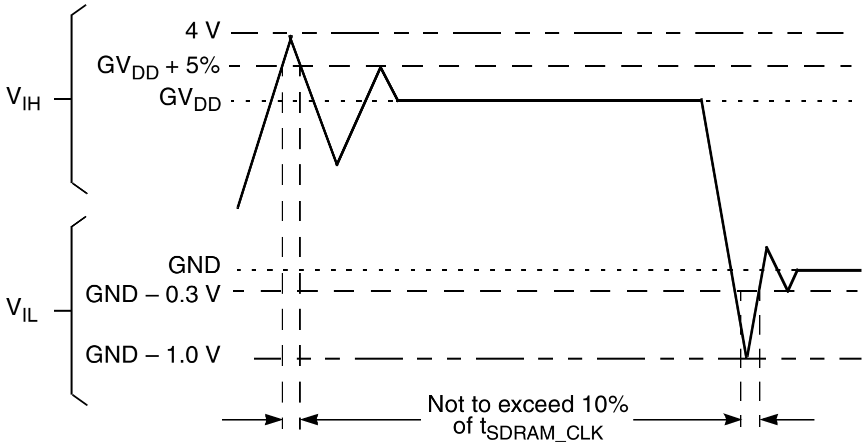


Figure 2. Overshoot/Undershoot Voltage

[5] MPC8272 and MPC8271 only.

Table 6.

Characteristic	Symbol	Min	Max	Unit
Input high voltage—all inputs except TCK, $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$[1]	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
CLKIN input high voltage	V_{IHC}	2.4	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0.4	V
Input leakage current, V_{IN} = VDDH[2]	I_{IN}	—	10	µA
Hi-Z (off state) leakage current, V_{IN} = VDDH[2]	I_{OZ}	—	10	µA
Signal low input current, V_{IL} = 0.8 V[3]	I_L	—	1	µA
Signal high input current, V_{IH} = 2.0 V	I_H	—	1	µA
Output high voltage, I_{OH} = –2 mA except UTOPIA mode, and open drain pins In UTOPIA mode[4] (UTOPIA pins only): I_{OH} = -8.0mA	V_{OH}	2.4	—	V
In UTOPIA mode[4] (UTOPIA pins only): I_{OL} = 8.0mA	V_{OL}	—	0.5	V
I_{OL} = 6.0mA $\overline{\text{BR}}$ $\overline{\text{BG}}$ $\overline{\text{ABB}}$/$\overline{\text{IRQ2}}$ $\overline{\text{TS}}$ A[0-31] TT[0-4] $\overline{\text{TBST}}$ TSIZE[0–3] $\overline{\text{AACK}}$ $\overline{\text{ARTRY}}$ $\overline{\text{DBG}}$ $\overline{\text{DBB}}$/$\overline{\text{IRQ3}}$ D[0-63] //$\overline{\text{EXT\_BR3}}$ //$\overline{\text{EXT\_BG3}}$ /$\overline{\text{TBEN}}$/$\overline{\text{EXT\_DBG3}}$/$\overline{\text{CINT}}$ $\overline{\text{PSDVAL}}$ $\overline{\text{TA}}$ $\overline{\text{TEA}}$ $\overline{\text{GBL}}$/$\overline{\text{IRQ1}}$ $\overline{\text{CI}}$/BADDR29/$\overline{\text{IRQ2}}$ $\overline{\text{WT}}$/BADDR30/$\overline{\text{IRQ3}}$ BADDR31/$\overline{\text{IRQ5}}$/$\overline{\text{CINT}}$ $\overline{\text{CPU\_BR}}$ $\overline{\text{IRQ0}}$/$\overline{\text{NMI\_OUT}}$ /$\overline{\text{PCI\_RST}}$ $\overline{\text{HRESET}}$ $\overline{\text{SRESET}}$ $\overline{\text{RSTCONF}}$	V_{OL}	—	0.4	V

4.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

4.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages, especially PBGA packages, is strongly dependent on the board temperature.

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)
T_B = board temperature (ºC)
P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

This table lists CPM input characteristics.

NOTE: Rise/Fall Time on CPM Input Pins

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

Table 11. AC Characteristics for CPM Inputs[1]

Spec Number		Characteristic	Value (ns)							
			Setup				Hold			
Setup	Hold		66 MHz	83 MHz	100 MHz	133 MHz	66 MHz	83 MHz	100 MHz	133 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	6	6	6	6	0	0	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	2.5	2.5	2.5	2.5	2	2	2	2
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	6	6	6	6	0	0	0	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	4	4	4	4	2	2	2	2
sp20	sp21	TDM inputs/SI	3	3	3	3	2.5	2.5	2.5	2.5
sp22	sp23	PIO/TIMER/IDMA inputs	8	8	8	8	0.5	0.5	0.5	0.5

[1] Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

NOTE

Although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the FCC internal clock.

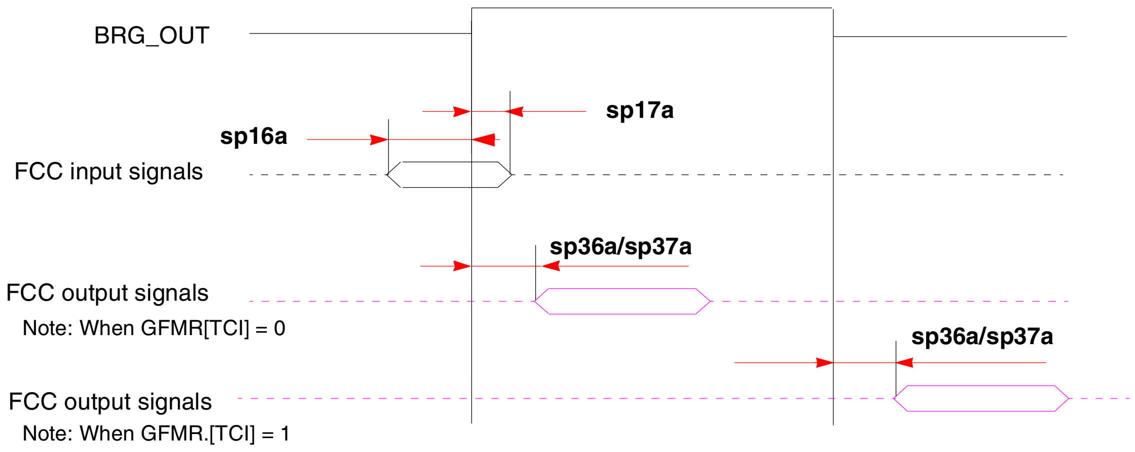
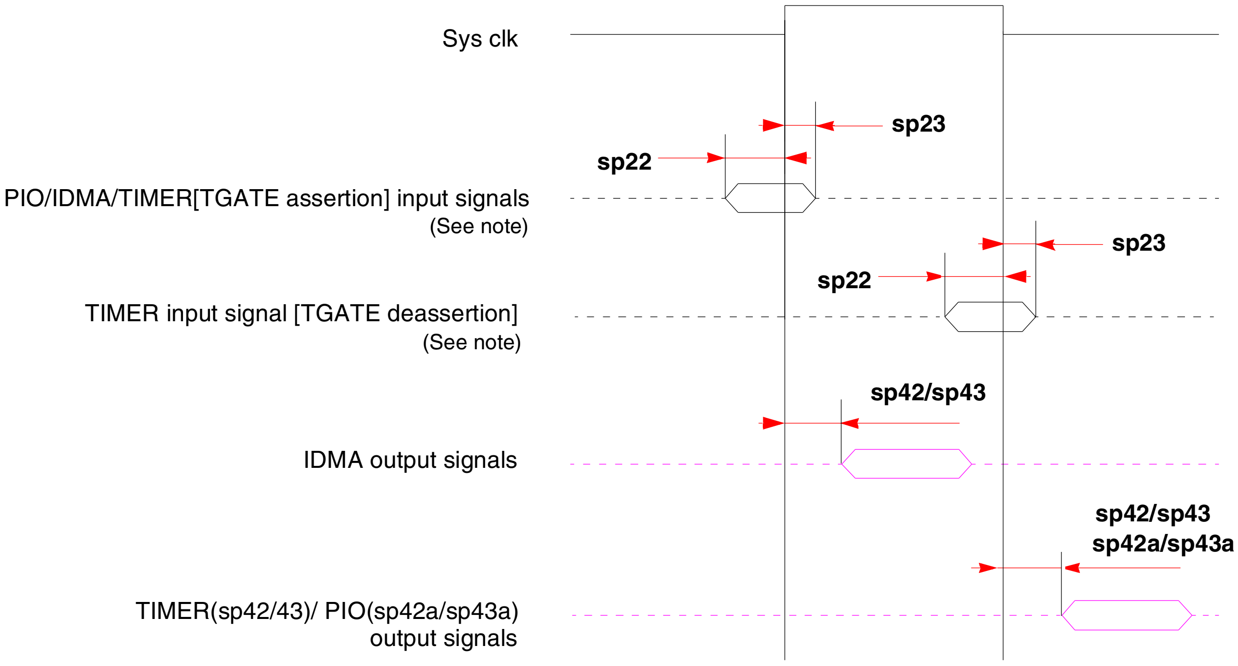


Figure 3. FCC Internal Clock Diagram

This figure shows PIO and timer signals.



Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

Figure 8. PIO and Timer Signal Diagram

6.2 SIU AC Characteristics

This table lists SIU input characteristics.

NOTE: CLKIN Jitter and Duty Cycle

The CLKIN input to the SoC should not exceed +/– 150 psec of jitter (peak-to-peak). This represents total input jitter—the combination of short term (peak-to-peak) and long term (cumulative). The duty cycle of CLKIN should not exceed the ratio of 40:60.

NOTE: Spread Spectrum Clocking

Spread spectrum clocking is allowed with 1% input frequency down-spread at maximum 60 KHz modulation rate regardless of input frequency.

NOTE: PCI AC Timing

The SoC meets the timing requirements of *PCI Specification Revision 2.2*. See Section 7, “Clock Configuration Modes,” and “Note: Tval (Output Hold)” to determine if a specific clock configuration is compliant.

7 Clock Configuration Modes

As shown in this table, the clocking mode is set according to two sources:

- PCI_CFG[0]— An input signal. Also defined as "PCI_HOST_EN." See Chapter 6, "External Signals," and Chapter 9, "PCI Bridge," in the SoC reference manual.
- PCI_MODCK—Bit 27 in the Hard Reset Configuration Word. See Chapter 5, "Reset," in the SoC reference manual.

Table 16. SoC Clocking Modes

Pins		Clocking Mode	PCI Clock Frequency Range (MHz)	Reference
PCI_CFG[0][1]	PCI_MODCK[2]			
0	0	PCI host	50–66	Table 17
0	1		25–50	Table 18
1	0	PCI agent	50–66	Table 19
1	1		25–50	Table 20

[1] PCI_HOST_EN

[2] Determines PCI clock frequency range.

Within each mode, the configuration of bus, core, PCI, and CPM frequencies is determined by seven bits during the power-on reset—three hardware configuration pins (MODCK[1–3]) and four bits from hardware configuration word[28–31] (MODCK_H). Both the PLLs and the dividers are set according to the selected clock operation mode as described in the following sections.

NOTE

Clock configurations change only after PORESET is asserted.

NOTE: Tval (Output Hold)

The minimum Tval = 2 ns when PCI_MODCK = 1, and the minimum Tval = 1 ns when PCI_MODCK = 0. Therefore, designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

7.1 PCI Host Mode

These tables show configurations for PCI host mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device. Note that in PCI host mode the input clock is the bus clock.

Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	Bus Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		PCI Division Factor[6]	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
0100_001	25.0	50.0	6	150.0	300.0	6	150.0	300.0	6	25.0	50.0
0100_010	25.0	50.0	6	150.0	300.0	7	175.0	350.0	6	25.0	50.0
0100_011	25.0	50.0	6	150.0	300.0	8	200.0	400.0	6	25.0	50.0
0101_000	60.0	100.0	2	120.0	200.0	2.5	150.0	250.0	4	30.0	50.0
0101_001	50.0	100.0	2	100.0	200.0	3	150.0	300.0	4	25.0	50.0
0101_010	50.0	100.0	2	100.0	200.0	3.5	175.0	350.0	4	25.0	50.0
0101_011	50.0	100.0	2	100.0	200.0	4	200.0	400.0	4	25.0	50.0
0101_100	50.0	100.0	2	100.0	200.0	4.5	225.0	450.0	4	25.0	50.0
0101_101	42.9	83.3	3	128.6	250.0	3.5	150.0	291.7	5	25.7	50.0
0101_110	41.7	83.3	3	125.0	250.0	4	166.7	333.3	5	25.0	50.0
0101_111	41.7	83.3	3	125.0	250.0	4.5	187.5	375.0	5	25.0	50.0
0110_000	60.0	120.0	2.5	150.0	300.0	2.5	150.0	300.0	6	25.0	50.0
0110_001	60.0	120.0	2.5	150.0	300.0	3	180.0	360.0	6	25.0	50.0
0110_010	60.0	120.0	2.5	150.0	300.0	3.5	210.0	420.0	6	25.0	50.0
0110_011	60.0	120.0	2.5	150.0	300.0	4	240.0	480.0	6	25.0	50.0
0110_100	60.0	120.0	2.5	150.0	300.0	4.5	270.0	540.0	6	25.0	50.0
0110_101	60.0	120.0	2.5	150.0	300.0	5	300.0	600.0	6	25.0	50.0
0110_110	60.0	120.0	2.5	150.0	300.0	6	360.0	720.0	6	25.0	50.0
0111_000	Reserved										
0111_001	50.0	100.0	3	150.0	300.0	3	150.0	300.0	6	25.0	50.0
0111_010	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
0111_011	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
0111_100	50.0	100.0	3	150.0	300.0	4.5	225.0	450.0	6	25.0	50.0
1000_000	Reserved										
1000_001	66.7	133.3	3	200.0	400.0	3	200.0	400.0	8	25.0	50.0

Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	Bus Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		PCI Division Factor[6]	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1000_010	66.7	133.3	3	200.0	400.0	3.5	233.3	466.7	8	25.0	50.0
1000_011	66.7	133.3	3	200.0	400.0	4	266.7	533.3	8	25.0	50.0
1000_100	66.7	133.3	3	200.0	400.0	4.5	300.0	600.0	8	25.0	50.0
1000_101	66.7	133.3	3	200.0	400.0	6	400.0	800.0	8	25.0	50.0
1000_110	66.7	133.3	3	200.0	400.0	6.5	433.3	866.7	8	25.0	50.0
1001_000	Reserved										
1001_001	Reserved										
1001_010	57.1	114.3	3.5	200.0	400.0	3.5	200.0	400.0	8	25.0	50.0
1001_011	57.1	114.3	3.5	200.0	400.0	4	228.6	457.1	8	25.0	50.0
1001_100	57.1	114.3	3.5	200.0	400.0	4.5	257.1	514.3	8	25.0	50.0
1001_101	42.9	85.7	3.5	150.0	300.0	5	214.3	428.6	6	25.0	50.0
1001_110	42.9	85.7	3.5	150.0	300.0	5.5	235.7	471.4	6	25.0	50.0
1001_111	42.9	85.7	3.5	150.0	300.0	6	257.1	514.3	6	25.0	50.0
1010_000	75.0	150.0	2	150.0	300.0	2	150.0	300.0	6	25.0	50.0
1010_001	75.0	150.0	2	150.0	300.0	2.5	187.5	375.0	6	25.0	50.0
1010_010	75.0	150.0	2	150.0	300.0	3	225.0	450.0	6	25.0	50.0
1010_011	75.0	150.0	2	150.0	300.0	3.5	262.5	525.0	6	25.0	50.0
1010_100	75.0	150.0	2	150.0	300.0	4	300.0	600.0	6	25.0	50.0
1010_101	100.0	200.0	2	200.0	400.0	2.5	250.0	500.0	8	25.0	50.0
1010_110	100.0	200.0	2	200.0	400.0	3	300.0	600.0	8	25.0	50.0
1010_111	100.0	200.0	2	200.0	400.0	3.5	350.0	700.0	8	25.0	50.0
1011_000	Reserved										
1011_001	80.0	160.0	2.5	200.0	400.0	2.5	200.0	400.0	8	25.0	50.0
1011_010	80.0	160.0	2.5	200.0	400.0	3	240.0	480.0	8	25.0	50.0
1011_011	80.0	160.0	2.5	200.0	400.0	3.5	280.0	560.0	8	25.0	50.0
1011_100	80.0	160.0	2.5	200.0	400.0	4	320.0	640.0	8	25.0	50.0

Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	Bus Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		PCI Division Factor[6]	PCI Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1011_101	80.0	160.0	2.5	200.0	400.0	4.5	360.0	720.0	8	25.0	50.0
1101_000	50.0	100.0	2.5	125.0	250.0	3	150.0	300.0	5	25.0	50.0
1101_001	50.0	100.0	2.5	125.0	250.0	3.5	175.0	350.0	5	25.0	50.0
1101_010	50.0	100.0	2.5	125.0	250.0	4	200.0	400.0	5	25.0	50.0
1101_011	50.0	100.0	2.5	125.0	250.0	4.5	225.0	450.0	5	25.0	50.0
1101_100	50.0	100.0	2.5	125.0	250.0	5	250.0	500.0	5	25.0	50.0
1101_101	62.5	125.0	2	125.0	250.0	3	187.5	375.0	5	25.0	50.0
1101_110	62.5	125.0	2	125.0	250.0	4	250.0	500.0	5	25.0	50.0
1110_000	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
1110_001	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
1110_010	50.0	100.0	3	150.0	300.0	4.5	225.0	450.0	6	25.0	50.0
1110_011	50.0	100.0	3	150.0	300.0	5	250.0	500.0	6	25.0	50.0
1110_100	50.0	100.0	3	150.0	300.0	5.5	275.0	550.0	6	25.0	50.0
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

[1] The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

[2] PCI_MODCK determines the PCI clock frequency range. See Table 17 for higher range configurations.

[3] MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

[4] CPM multiplication factor = CPM clock/bus clock

[5] CPU multiplication factor = Core PLL multiplication factor

Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2] (continued)

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1000_000	Reserved										
1000_001	50.0	66.7	3	150.0	200.0	2.5	150.0	166.7	2.5	60.0	80.0
1000_010	50.0	66.7	3	150.0	200.0	3	180.0	240.0	2.5	60.0	80.0
1000_011	50.0	66.7	3	150.0	200.0	3.5	210.0	280.0	2.5	60.0	80.0
1000_100	50.0	66.7	3	150.0	200.0	4	240.0	320.0	2.5	60.0	80.0
1000_101	50.0	66.7	3	150.0	200.0	4.5	270.0	360.0	2.5	60.0	80.0
1001_000	Reserved										
1001_001	Reserved										
1001_010	Reserved										
1001_011	50.0	66.7	4	200.0	266.6	4	200.0	266.6	4	50.0	66.7
1001_100	50.0	66.7	4	200.0	266.6	4.5	225.0	300.0	4	50.0	66.7
1010_000	Reserved										
1010_001	50.0	66.7	4	200.0	266.6	3	200.0	266.6	3	66.7	88.9
1010_010	50.0	66.7	4	200.0	266.6	3.5	233.3	311.1	3	66.7	88.9
1010_011	50.0	66.7	4	200.0	266.6	4	266.7	355.5	3	66.7	88.9
1010_100	50.0	66.7	4	200.0	266.6	4.5	300.0	400.0	3	66.7	88.9
1011_000	Reserved										
1011_001	50.0	66.7	4	200.0	266.6	2.5	200.0	266.6	2.5	80.0	106.7
1011_010	50.0	66.7	4	200.0	266.6	3	240.0	320.0	2.5	80.0	106.7
1011_011	50.0	66.7	4	200.0	266.6	3.5	280.0	373.3	2.5	80.0	106.7
1011_100	50.0	66.7	4	200.0	266.6	4	320.0	426.6	2.5	80.0	106.7
1011_101	50.0	66.7	4	200.0	266.6	2.5	250.0	333.3	2	100.0	133.3
1011_110	50.0	66.7	4	200.0	266.6	3	300.0	400.0	2	100.0	133.3
1011_111	50.0	66.7	4	200.0	266.6	3.5	350.0	466.6	2	100.0	133.3

Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1001_010	Reserved										
1001_011	25.0	50.0	8	200.0	400.0	4	200.0	400.0	4	50.0	100.0
1001_100	25.0	50.0	8	200.0	400.0	4.5	225.0	450.0	4	50.0	100.0
1010_000	Reserved										
1010_001	25.0	50.0	8	200.0	400.0	3	200.0	400.0	3	66.7	133.3
1010_010	25.0	50.0	8	200.0	400.0	3.5	233.3	466.7	3	66.7	133.3
1010_011	25.0	50.0	8	200.0	400.0	4	266.7	533.3	3	66.7	133.3
1010_100	25.0	50.0	8	200.0	400.0	4.5	300.0	600.0	3	66.7	133.3
1011_000	Reserved										
1011_001	25.0	50.0	8	200.0	400.0	2.5	200.0	400.0	2.5	80.0	160.0
1011_010	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
1011_011	25.0	50.0	8	200.0	400.0	3.5	280.0	560.0	2.5	80.0	160.0
1011_100	25.0	50.0	8	200.0	400.0	4	320.0	640.0	2.5	80.0	160.0
1011_101	25.0	50.0	8	200.0	400.0	2.5	250.0	500.0	2	100.0	200.0
1011_110	25.0	50.0	8	200.0	400.0	3	300.0	600.0	2	100.0	200.0
1011_111	25.0	50.0	8	200.0	400.0	3.5	350.0	700.0	2	100.0	200.0
1100_101	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0
1100_110	25.0	50.0	6	150.0	300.0	4.5	225.0	450.0	3	50.0	100.0
1100_111	25.0	50.0	6	150.0	300.0	5	250.0	500.0	3	50.0	100.0
1101_000	25.0	50.0	6	150.0	300.0	5.5	275.0	550.0	3	50.0	100.0
1101_001	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
1101_010	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
1101_011	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
1101_100	25.0	50.0	6	150.0	300.0	5	300.0	600.0	2.5	60.0	120.0

Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)

Mode[3]	PCI Clock (MHz)		CPM Multiplication Factor[4]	CPM Clock (MHz)		CPU Multiplication Factor[5]	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1110_000	25.0	50.0	5	125.0	250.0	2.5	156.3	312.5	2	62.5	125.0
1110_001	25.0	50.0	5	125.0	250.0	3	187.5	375.0	2	62.5	125.0
1110_010	28.6	50.0	5	142.9	250.0	3.5	250.0	437.5	2	71.4	125.0
1110_011	25.0	50.0	5	125.0	250.0	4	250.0	500.0	2	62.5	125.0
1110_100	25.0	50.0	5	125.0	250.0	4	166.7	333.3	3	41.7	83.3
1110_101	25.0	50.0	5	125.0	250.0	4.5	187.5	375.0	3	41.7	83.3
1110_110	25.0	50.0	5	125.0	250.0	5	208.3	416.7	3	41.7	83.3
1110_111	25.0	50.0	5	125.0	250.0	5.5	229.2	458.3	3	41.7	83.3
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

[1] The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

[2] PCI_MODCK determines the PCI clock frequency range. See Table 19 for higher range configurations.

[3] MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

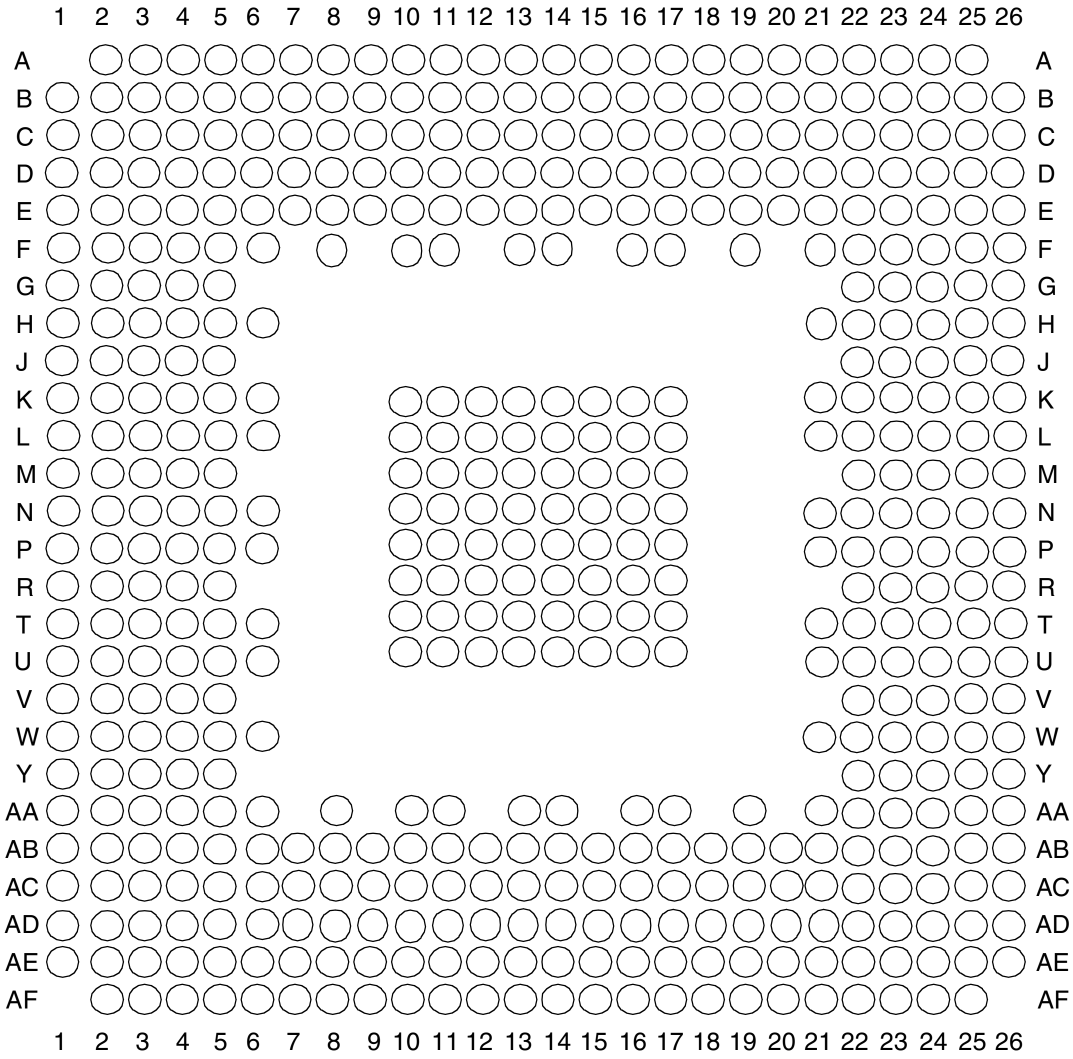
[4] CPM multiplication factor = CPM clock/bus clock

[5] CPU multiplication factor = Core PLL multiplication factor

8 Pinout

This figure and table show the pin assignments and pinout for the 516 PBGA package.

This figure shows the pinout of the 516 PBGA package as viewed from the top surface.



Not to Scale

Figure 12. Pinout of the 516 PBGA Package (View from Top)

This table lists the pins of the MPC8272. Note that the pins in the "MPC8272/8271 Only" column relate to Utopia functionality.

Table 21. Pinout

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
$\overline{\text{BR}}$		A19
$\overline{\text{BG}}$/$\overline{\text{IRQ6}}$		D2
$\overline{\text{ABB}}$/$\overline{\text{IRQ2}}$		C1

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
D15		G3
D16		AB3
D17		Y1
D18		T4
D19		T3
D20		P2
D21		M1
D22		J1
D23		G4
D24		AB2
D25		W4
D26		V2
D27		T1
D28		N5
D29		L1
D30		H1
D31		G5
D32		W5
D33		W2
D34		T5
D35		T2
D36		N1
D37		K3
D38		H2
D39		F1
D40		AA2
D41		W1
D42		U3
D43		R2
D44		N2
D45		L2

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
PCI_AD16		AE16
PCI_AD17		AF17
PCI_AD18		AD16
PCI_AD19		AC16
PCI_AD20		AF18
PCI_AD21		AB16
PCI_AD22		AD17
PCI_AD23		AF19
PCI_AD24		AB17
PCI_AD25		AF20
PCI_AD26		AE19
PCI_AD27		AC18
PCI_AD28		AB18
PCI_AD29		AD19
PCI_AD30		AD21
PCI_AD31		AC20
PCI_C0/BE0		AE12
PCI_C1/BE1		AF13
PCI_C2/BE2		AC15
PCI_C3/BE3		AE18
IRQ0/NMI_OUT		A17
TRST[2]		E21
TCK		B22
TMS		C23
TDI		B24
TDO		A22
TRIS		B23
PORESET[2]/PCI_RST		C24
HRESET		D22
SRESET		F22
RSTCONF		A24

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
PA31/FCC1_MII_COL	FCC1_UT_TXENB	G22[3]
PB18/FCC2_MII_HDLC_RXD3		T25[3]
PB19/FCC2_MII_HDLC_RXD2		P22[3]
PB20/FCC2_MII_HDLC_RMII_RXD1		L25[3]
PB21/FCC2_MII_HDLC_RMII_RXD0/FCC2_TRAN_RXD		J26[3]
PB22/FCC2_MII_HDLC_TXD0/FCC2_TRAN_TXD/ FCC2_RMII_TXD0		U23[3]
PB23/FCC2_MII_HDLC_TXD1/FCC2_RMII_TXD1		U26[3]
PB24/FCC2_MII_HDLC_TXD2/L1RSYNCB2		M24[3]
PB25/FCC2_MII_HDLC_TXD3/L1TSYNCB2		M23[3]
PB26/FCC2_MII_CRS/L1RXDB2		H24[3]
PB27/FCC2_MII_COL/L1TXDB2		E25[3]
PB28/FCC2_MII_RMII_RX_ER/FCC2_RTS/TXD1		D26[3]
PB29/FCC2_MII_RMII_TX_EN		K21[3]
PB30/FCC2_MII_RX_DV/FCC2_RMII_CRS_DV		D24[3]
PB31/FCC2_MII_TX_ER		E23[3]
PC0/DREQ3/BRGO7/SMSYN1/L1CLKOA2		AF23[3]
PC1/BRGO6/L1RQA2		AD23[3]
PC4/SMRXD1/SI2_L1ST4/FCC2_CD		AB22[3]
PC5/SMTXD1/SI2_L1ST3/FCC2_CTS		AE24[3]
PC6/FCC1_CD/SI2_L1ST2	FCC1_UT_RXADDR2	AF24[3]
PC7/FCC1_CTS	FCC1_UT_TXADDR2	AE26[3]
PC8/CD4/RTS1/SI2_L1ST2/CTS3		AC24[3]
PC9/CTS4/L1TSYNCA2		AA23[3]
PC10/CD3/USB_RN		AB25[3]
PC11/CTS3/USB_RP/L1TXD3A2		V22[3]
PC12	FCC1_UT_RXADDR1	AA26[3]
PC13/BRGO5	FCC1_UT_TXADDR1	V23[3]
PC14/CD1	FCC1_UT_RXADDR0	W24[3]
PC15/CTS1	FCC1_UT_TXADDR0	U24[3]
PC16/CLK16		T23[3]

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	**MPC8272/MPC8271 Only**	
PC17/CLK15/BRGO8/$\overline{\text{DONE2}}$		T26[3]
PC18/CLK14/$\overline{\text{TGATE2}}$		R26[3]
PC19/CLK13/BRGO7/$\overline{\text{TGATE1}}$		P24[3]
PC20/CLK12/$\overline{\text{USBOE}}$		L26[3]
PC21/CLK11/BRGO6/CP_INT		L24[3]
PC22/CLK10/$\overline{\text{DONE3}}$	FCC1_UT_TXPRTY	L23[3]
PC23/CLK9/BRGO5/$\overline{\text{DACK3}}$/$\overline{\text{CD1}}$		K24[3]
PC24/CLK8/TIN3/$\overline{\text{TOUT4}}$/DREQ2/BRGO1		K23[3]
PC25/CLK7/BRGO4/$\overline{\text{DACK2}}$/SPISEL		F26[3]
PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK		H23[3]
PC27/CLK5/BRGO3/$\overline{\text{TOUT1}}$	FCC1_UT_RXPRTY	K22[3]
PC28/CLK4/TIN1/$\overline{\text{TOUT2}}$/SPICLK		D25[3]
PC29/CLK3/TIN2/BRGO2/$\overline{\text{CTS1}}$		F24[3]
PD7/SMSYN2	FCC1_UT_TXADDR3	AB21[3]
PD14/I2CSCL		AC26[3]
PD15/I2CSDA		Y23[3]
PD16/SPIMISO	FCC1_UT_TXPRTY	AA25[3]
PD17/BRGO2/SPIMOSI	FCC1_UT_RXPRTY	Y26[3]
PD18/SPICLK	FCC1_UT_RXADDR4	W25[3]
PD19/SPISEL/BRGO1	FCC1_UT_TXADDR4	V25[3]
PD20/$\overline{\text{RTS4}}$/L1RSYNCA2		R24[3]
PD21/TXD4/L1RXD0A2		P23[3]
PD22/RXD4/L1TXD0A2		N25[3]
PD23/$\overline{\text{RTS3}}$/USB_TP		K26[3]
PD24/TXD3/USB_TN		K25[3]
PD25/RXD3/USB_RXD		J25[3]
PD29/$\overline{\text{RTS1}}$	FCC1_UT_RXADDR3	C26[3]
PD30/TXD1		E24[3]
PD31/RXD1		B25[3]
VCCSYN		C18
VCCSYN1		K6

10 Ordering Information

This figure provides an example of the Freescale part numbering nomenclature for the SoC. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

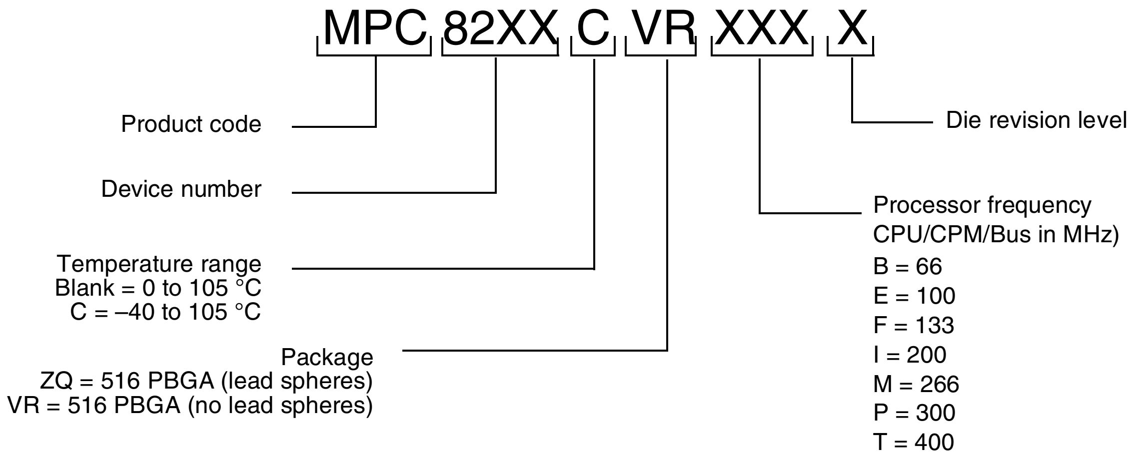


Figure 15. Freescale Part Number Key

11 Document Revision History

This table summarizes changes to this document.

Table 23. Document Revision History

Revision	Date	Substantive Changes
3	09/2011	In Figure 15, “Freescale Part Number Key,” added speed decoding information below processor frequency information.
2	12/2008	• Modified Figure 5, “SCC/SMC/SPI/I2C External Clock Diagram,” and added second section of figure notes. • In Table 12, modified “Data bus in pipeline mode” row and showed 66 MHz as “N/A.” • In Section 10, “Ordering Information,” added “F = 133” to CPU/CPM/Bus Frequency. • Added footnote concerning CPM_CLK/PCI_CLK ratio to column “PCI Division Factor” in Table 17, “Clock Configurations for PCI Host Mode (PCI_MODCK=0),” and Table 18, “Clock Configurations for PCI Host Mode (PCI_MODCK=1),.” • Removed overbar from DLL_ENABLE in Table 21, “Pinout.”
1.5	12/2006	• Section 6, “AC Electrical Characteristics,” removed deratings statement and clarified AC timing descriptions.
1.4	05/2006	• Added row for 133 MHz configurations to Table 8.
1.3	02/2006	• Inserted Section 6.3, “JTAG Timings.”

Table 23. Document Revision History (continued)

Revision	Date	Substantive Changes
0.2	12/2003	• Table 1: New • Table 2: New • Table 4: Modification of VDD and VCCSYN to 1.45–1.60 V • Table 8: Addition of note 2 regarding $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ (see V_{IH} row of Table 8) • Table 8 and Table 21: Addition of muxed signals CPCI_HS_ES to $\overline{\text{PCI\_REQ1}}$ (AF14) CPCI_HS_LED to $\overline{\text{PCI\_GNT1}}$ (AE13) $\overline{\text{CPCI\_HS\_ENUM}}$ to $\overline{\text{PCI\_GNT2}}$ (AF21) • Table 8 and Table 21: Modification of PCI signal names for consistency with PCI signal names on other PowerQUICC II devices: PCI_CFG0 ($\overline{\text{PCI\_HOST\_EN}}$) (AC21) PCI_CFG1 ($\overline{\text{PCI\_ARB\_EN}}$) (AE22) PCI_CFG2 (DLL_ENABLE) (AE23) PCI_PAR (AF12) $\overline{\text{PCI\_FRAME}}$ (AD15) $\overline{\text{PCI\_TRDY}}$(AF16) $\overline{\text{PCI\_IRDY}}$ (AF15) $\overline{\text{PCI\_STOP}}$ (AE15) $\overline{\text{DEVSEL}}$ (AE14) PCI_IDSEL (AC17) $\overline{\text{PCI\_PERR}}$ (AD14) $\overline{\text{PCI\_SERR}}$ (AD13) $\overline{\text{PCI\_REQ0–2}}$ (AAE20, AF14, AB14) $\overline{\text{PCI\_GNT0–2}}$ (AD20, AE13, AF21) $\overline{\text{PCI\_RST}}$ (AF22) $\overline{\text{PCI\_INTA}}$ (AE21) $\overline{\text{PCI\_C0-3}}$ (AE12, AF13, AC15, AE18) PCI_AD0-31 • Table 8 and Table 21: Corrected assertion level (added “‾“) $\overline{\text{PCI\_HOST\_EN}}$ (AC21) and $\overline{\text{PCI\_ARB\_EN}}$ (AE22) • Table 7: Addition of $R_{\theta JT}$ and note 4 • Sections 4.1–4.5 and 4.7 on thermal characteristics: New • Section 7, “Clock Configuration Modes”: Modification to first paragraph. Note that PCI_MODCK is a bit in the Hard Reset Configuration Word. It is not an input signal as it is in the MPC8280 Family and MPC8260 Family. • Addition of “Note: Temperature Reflow for the VR Package" on page 56 • Table 21: Addition of note 2 to $\overline{\text{TRST}}$ (E21) and $\overline{\text{PORESET}}$ (C24) • Table 21: Removal of Thermal0 (D19) and Thermal1(J3). These pins are now “No connects.” Note 4 unchanged. • Table 21: Removal of Spare0 (AD24). This pin is now a “No connect.” Note 5 unchanged. • Table 21: Addition of $\overline{\text{PCI\_MODE}}$ (AD22). This pin was previously listed as “Ground.” Addition of note 1.
0.1	9/2003	• Addition of the MPC8271 and the MPC8247 (these devices do not have a security engine) • Table 8: Addition of note 2 to V_{IH} • Table 8: Changed I_{OL} for 60x signals to 6.0 mA • Modification of note 1 for Table 17, Table 18, Table 19, and Table 20 • Table 21: Addition of ball AD9 to GND. In rev 0 of this document, AD8 was listed as assigned to both $\overline{\text{CS5}}$ and GND. AD8 is only assigned to $\overline{\text{CS5}}$. • Table 21: Addition of note 4 to Thermal0 (D19) and Thermal1(J3) • Addition of ZQ package code to Figure 15
0	5/2003	NDA release