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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	300MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8271vrpiea

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Overview

1 Overview

This table shows the functionality supported by each SoC in the MPC8272 family.

			SoCs					
Functionality		MPC8272	MPC8248	MPC8271	MPC8247			
	Package ¹	516 PBGA						
Serial communications controllers (SC	Cs)	3	3	3	3			
QUICC multi-channel controller (QMC)		Yes	Yes	Yes	Yes			
Fast communication controllers (FCCs))	2	2	2	2			
I-Cache (Kbyte)		16	16	16	16			
D-Cache (Kbyte)		16	16	16	16			
Ethernet (10/100)		2	2	2	2			
UTOPIA II Ports		1	0	1	0			
Multi-channel controllers (MCCs)		0	0	0	0			
PCI bridge		Yes	Yes	Yes	Yes			
Transmission convergence (TC) layer		_	—	_	—			
Inverse multiplexing for ATM (IMA)	lexing for ATM (IMA) — — — —							
Universal serial bus (USB) 2.0 full/low	rate	1	1	1	1			
Security engine (SEC)		Yes	Yes	—	—			

Table 1. MPC8272 PowerQUICC II Family Functionality

¹ See Table 2.

Devices in the MPC8272 family are available in two packages—the VR or ZQ package—as shown in . For package ordering information, see Section 10, "Ordering Information."

Code (Package)	VR (516 PBGA—Lead free)	ZQ (516 PBGA—Lead spheres)
	MPC8272VR	MPC8272ZQ
Device	MPC8248VR	MPC8248ZQ
Device	MPC8271VR	MPC8271ZQ
	MPC8247VR	MPC8247ZQ

Table 2. MPC8272 PowerQUICC II Device Packages



This figure shows the block diagram of the SoC.





1.1 Features

The major features of the SoC are as follows:

- Dual-issue integer (G2_LE) core
 - A core version of the MPC603e microprocessor
 - System core microprocessor supporting frequencies of 266–400 MHz
 - Separate 16 KB data and instruction caches:
 - Four-way set associative
 - Physically addressed
 - LRU replacement algorithm
 - Power Architecture®-compliant memory management unit (MMU)
 - Common on-chip processor (COP) test interface
 - Supports bus snooping for cache coherency



- PCI bridge
 - PCI Specification revision 2.2-compliant and supports frequencies up to 66 MHz
 - On-chip arbitration
 - Support for PCI to 60x memory and 60x memory to PCI streaming
 - PCI host bridge or peripheral capabilities
 - Includes four DMA channels for the following transfers:
 - PCI-to-60x to 60x-to-PCI
 - 60x-to-PCI to PCI-to-60x
 - PCI-to-60x to PCI-to-60x
 - 60x-to-PCI to 60x-to-PCI
 - Includes the configuration registers required by the PCI standard (which are automatically loaded from the EPROM to configure the MPC8272) and message and doorbell registers
 - Supports the I_2O standard
 - Hot-Swap friendly (supports the Hot Swap Specification as defined by PICMG 2.1 R1.0 August 3, 1998)
 - Support for 66 MHz, 3.3 V specification
 - 60x-PCI bus core logic, which uses a buffer pool to allocate buffers for each port

2 **Operating Conditions**

This table shows the maximum electrical ratings.

Table 3. Absolute Maximum Ratings¹

Rating	Symbol	Value	Unit
Core supply voltage ²	VDD	-0.3 - 2.25	V
PLL supply voltage ²	VCCSYN	-0.3 - 2.25	V
I/O supply voltage ³	VDDH	-0.3 - 4.0	V
Input voltage ⁴	VIN	GND(-0.3) - 3.6	V
Junction temperature	Тj	120	°C
Storage temperature range	T _{STG}	(–55) – (+150)	°C

¹ Absolute maximum ratings are stress ratings only; functional operation (see Table 4) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.

- ² Caution: VDD/VCCSYN must not exceed VDDH by more than 0.4 V during normal operation. It is recommended that VDD/VCCSYN should be raised before or simultaneous with VDDH during power-on reset. VDD/VCCSYN may exceed VDDH by more than 0.4 V during power-on reset for no more than 100 ms.
- ³ Caution: VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.5 V during normal operation.
- ⁴ Caution: VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.



DC Electrical Characteristics

⁵ MPC8272 and MPC8271 only.

Table 6.

Characteristic	Symbol	Min	Max	Unit
Input high voltage—all inputs except TCK, TRST and PORESET ¹	VIH	2.0	3.465	V
Input low voltage	V _{IL}	GND	0.8	V
CLKIN input high voltage	VIHC	2.4	3.465	V
CLKIN input low voltage	V _{ILC}	GND	0.4	V
Input leakage current, V _{IN} = VDDH ²	I _{IN}		10	μA
Hi-Z (off state) leakage current, V _{IN} = VDDH ²	I _{OZ}	_	10	μA
Signal low input current, V _{IL} = 0.8 V ³	١	_	1	μA
Signal high input current, V _{IH} = 2.0 V	Ι _Η	_	1	μA
Output high voltage, $I_{OH} = -2 \text{ mA}$ except UTOPIA mode, and open drain pins In UTOPIA mode ⁴ (UTOPIA pins only): $I_{OH} = -8.0 \text{mA}$	V _{OH}	2.4	_	V
In UTOPIA mode ⁴ (UTOPIA pins only): I _{OL} = 8.0mA	V _{OL}	_	0.5	V
I _{OL} = 6.0mA BR BG ABB/IRQ2 TS A[0-31] TT[0-4] TBST TSIZE[0-3] AACK ARTRY DBG DBB/IRQ3 D[0-63] //EXT_BR3 //EXT_BR3 //EXT_BG3	V _{OL}		0.4	V



Thermal Characteristics

⁴ MPC8280, MPC8275VR, MPC8275ZQ only.

4 Thermal Characteristics

This table describes thermal characteristics. See Table 2 for information on a given SoC's package. Discussions of each characteristic are provided in Section 4.1, "Estimation with Junction-to-Ambient Thermal Resistance," through Section 4.7, "References." For the these discussions, $P_D = (V_{DD} \times I_{DD}) + PI/O$, where PI/O is the power dissipation of the I/O drivers.

Characteristic	Symbol	Value	Unit	Air Flow
Junction-to-ambient—	P	27		Natural convection
single-layer board	R _θ JA	21	°C/W	1 m/s
Junction-to-ambient—	P	19		Natural convection
four-layer board	R _{θJA}	16	°C/W	1 m/s
Junction-to-board ²	$R_{ extsf{ heta}JB}$	11	°C/W	—
Junction-to-case ³	$R_{ extsf{ heta}JC}$	8	°C/W	_
Junction-to-package top ⁴	$R_{ extsf{ heta}JT}$	2	°C/W	—

Table 7. Thermal Characteristics

¹ Assumes no thermal vias

² Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

³ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

⁴ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, in C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

 T_A = ambient temperature (°C)

 $R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)

 P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_I - T_A$) are possible.



This figure shows the SCC/SMC/SPI/I²C internal clock.



Note: There are four possible timing conditions for SCC and SPI:

- 1. Input sampled on the rising edge and output driven on the rising edge (shown).
- 2. Input sampled on the rising edge and output driven on the falling edge.
- 3. Input sampled on the falling edge and output driven on the falling edge.
- 4. Input sampled on the falling edge and output driven on the rising edge.

Figure 6. SCC/SMC/SPI/I²C Internal Clock Diagram

This figure shows TDM input and output signals.



Note: There are four possible TDM timing conditions:

- 1. Input sampled on the rising edge and output driven on the rising edge (shown).
- 2. Input sampled on the rising edge and output driven on the falling edge.
- 3. Input sampled on the falling edge and output driven on the falling edge.
- 4. Input sampled on the falling edge and output driven on the rising edge.

Figure 7. TDM Signal Diagram



AC Electrical Characteristics

This figure shows PIO and timer signals.



Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

Figure 8. PIO and Timer Signal Diagram

6.2 SIU AC Characteristics

This table lists SIU input characteristics.

NOTE: CLKIN Jitter and Duty Cycle

The CLKIN input to the SoC should not exceed +/- 150 psec of jitter (peak-to-peak). This represents total input jitter—the combination of short term (peak-to-peak) and long term (cumulative). The duty cycle of CLKIN should not exceed the ratio of 40:60.

NOTE: Spread Spectrum Clocking

Spread spectrum clocking is allowed with 1% input frequency down-spread at maximum 60 KHz modulation rate regardless of input frequency.

NOTE: PCI AC Timing

The SoC meets the timing requirements of *PCI Specification Revision 2.2.* See Section 7, "Clock Configuration Modes," and "Note: Tval (Output Hold)" to determine if a specific clock configuration is compliant.



NOTE: Conditions

The following conditions must be met in order to operate the MPC8272 family devices with 133 MHz bus: single PowerQUICC II Bus mode must be used (no external master, BCR[EBM] = 0); data bus must be in Pipeline mode (BRx[DR] = 1); internal arbiter and memory controller must be used. For expected load of above 40 pF, it is recommended that data and address buses be configured to low (25 Ω) impedance (SIUMCR[HLBE0] = 1, SIUMCR[HLBE1] = 1).

Spec N	umber		Value (ns)										
	Characteristic		Se	tup		Hold							
Setup	Hold		66 MHz	83 MHz	100 MHz	133 MHz	66 MHz	83 MHz	Hold 83 100 13 MHz MHz MI 0.5 0.5 N 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5	133 MHz			
sp11	sp10	AACK/TA/TS/DBG/BG/BR/ARTRY/TEA	6	5	3.5	N/A	0.5	0.5	0.5	N/A			
sp12	sp10	Data bus in normal mode	5	4	3.5	N/A	0.5	0.5	0.5	N/A			
sp13	sp10	Data bus in pipeline mode (without ECC and PARITY)	N/A	4	2.5	1.5	N/A	0.5	0.5	0.5			
sp15	sp10	All other pins	5	4	3.5	N/A	0.5	0.5	0.5	N/A			

Table 12. AC Characteristics for SIU Inputs¹

¹ Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

This table lists SIU output characteristics.

Table 13. AC Characteristics for SIU Outputs¹

Spec N	lumber		Value (ns)									
	Characteristic	I	Maximu	m Delay	/	Minimum Delay						
Мах	Min		66 MHz	83 MHz	100 MHz	133 MHz	66 MHz	83 100 133 MHz MHz MHz MHz 1 1 N/A 1 1 1 ² 0.8 0.8 1	133 MHz			
sp31	sp30	PSDVAL/TEA/TA	7	6	5.5	N/A	1	1	1	N/A		
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	5.5	4.5 ²	1	1	1	1 ²		
sp33	sp30	Data bus ³	6.5	6.5	5.5	4.5	0.8	0.8	0.8	1		
sp34	sp30	Memory controller signals/ALE	6	5.5	5.5	4.5	1	1	1	1		
sp35	sp30	All other signals	6	5.5	5.5	N/A	1	1	1	N/A		

¹ Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

² Value is for ADD only; other sp32/sp30 signals are not applicable.

³ To achieve 1 ns of hold time at 66.67/83.33/100 MHZ, a minimum loading of 20 pF is required.



Mode ³	Bus ((M	Clock Hz)	CPM Multiplication	CPM (M	Clock Hz)	CPU	CPU (M	Clock Hz)	PCI	PCI ((M	Clock Hz)
MODCK_H- MODCK[1-3]	Low	High	Factor ⁴	Low	High	Factor ⁵	Low	High	Factor ⁶	Low	High
0100_001	25.0	50.0	6	150.0	300.0	6	150.0	300.0	6	25.0	50.0
0100_010	25.0	50.0	6	150.0	300.0	7	175.0	350.0	6	25.0	50.0
0100_011	25.0	50.0	6	150.0	300.0	8	200.0	400.0	6	25.0	50.0
0101_000	60.0	100.0	2	120.0	200.0	2.5	150.0	250.0	4	30.0	50.0
0101_001	50.0	100.0	2	100.0	200.0	3	150.0	300.0	4	25.0	50.0
0101_010	50.0	100.0	2	100.0	200.0	3.5	175.0	350.0	4	25.0	50.0
0101_011	50.0	100.0	2	100.0	200.0	4	200.0	400.0	4	25.0	50.0
0101_100	50.0	100.0	2	100.0	200.0	4.5	225.0	450.0	4	25.0	50.0
					•						
0101_101	42.9	83.3	3	128.6	250.0	3.5	150.0	291.7	5	25.7	50.0
0101_110	41.7	83.3	3	125.0	250.0	4	166.7	333.3	5	25.0	50.0
0101_111	41.7	83.3	3	125.0	250.0	4.5	187.5	375.0	5	25.0	50.0
0110_000	60.0	120.0	2.5	150.0	300.0	2.5	150.0	300.0	6	25.0	50.0
0110_001	60.0	120.0	2.5	150.0	300.0	3	180.0	360.0	6	25.0	50.0
0110_010	60.0	120.0	2.5	150.0	300.0	3.5	210.0	420.0	6	25.0	50.0
0110_011	60.0	120.0	2.5	150.0	300.0	4	240.0	480.0	6	25.0	50.0
0110_100	60.0	120.0	2.5	150.0	300.0	4.5	270.0	540.0	6	25.0	50.0
0110_101	60.0	120.0	2.5	150.0	300.0	5	300.0	600.0	6	25.0	50.0
0110_110	60.0	120.0	2.5	150.0	300.0	6	360.0	720.0	6	25.0	50.0
0111_000						Reserved					
0111_001	50.0	100.0	3	150.0	300.0	3	150.0	300.0	6	25.0	50.0
0111_010	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
0111_011	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
0111_100	50.0	100.0	3	150.0	300.0	4.5	225.0	450.0	6	25.0	50.0
	-			-	•		-				
1000_000						Reserved					
1000_001	66.7	133.3	3	200.0	400.0	3	200.0	400.0	8	25.0	50.0

Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)^{1,2} (continued)



Clock Configuration Modes

- ⁶ CPM_CLK/PCI_CLK ratio. When PCI_MODCK = 1, the ratio of CPM_CLK/PCI_CLK should be calculated from PCIDF as follows: PCIDF = 3 > CPM_CLK/PCI_CLK = 4 PCIDF = 5 > CPM_CLK/PCI_CLK = 6 PCIDF = 7 > CPM_CLK/PCI_CLK = 8
 - PCIDF = 9 > CPM_CLK/PCI_CLK = 5
 - PCIDF = B > CPM_CLK/PCI_CLK = 6

7.2 PCI Agent Mode

These tables show configurations for PCI agent mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device. Note that in PCI agent mode the input clock is PCI clock.

Mode ³	PCI ((Mi	Clock Hz)	CPM Multiplication	CPM Clock (MHz)		CPM Clock (MHz)		M Clock (MHz) CPU (MHz) Bus Multiplication Divisio		Bus	Bus Clock (MHz)	
MODCK_H- MODCK[1-3]	Low	High	Factor ⁴	Low	High	Factor ⁵	Low	High	Factor	Low	High	
Default Modes (MODCK_H=0000)												
0000_000	60.0	66.7	2	120.0	133.3	2.5	150.0	166.7	2	60.0	66.7	
0000_001	50.0	66.7	2	100.0	133.3	3	150.0	200.0	2	50.0	66.7	
0000_010	50.0	66.7	3	150.0	200.0	3	150.0	200.0	3	50.0	66.7	
0000_011	50.0	66.7	3	150.0	200.0	4	200.0	266.6	3	50.0	66.7	
0000_100	50.0	66.7	3	150.0	200.0	3	180.0	240.0	2.5	60.0	80.0	
0000_101	50.0	66.7	3	150.0	200.0	3.5	210.0	280.0	2.5	60.0	80.0	
0000_110	50.0	66.7	4	200.0	266.6	3.5	233.3	311.1	3	66.7	88.9	
0000_111	50.0	66.7	4	200.0	266.6	3	240.0	320.0	2.5	80.0	106.7	
			F	ull Con	figurati	ion Modes						
0001_001	60.0	66.7	2	120.0	133.3	5	150.0	166.7	4	30.0	33.3	
0001_010	50.0	66.7	2	100.0	133.3	6	150.0	200.0	4	25.0	33.3	
0001_011	50.0	66.7	2	100.0	133.3	7	175.0	233.3	4	25.0	33.3	
0001_100	50.0	66.7	2	100.0	133.3	8	200.0	266.6	4	25.0	33.3	
0010_001	50.0	66.7	3	150.0	200.0	3	180.0	240.0	2.5	60.0	80.0	
0010_010	50.0	66.7	3	150.0	200.0	3.5	210.0	280.0	2.5	60.0	80.0	
0010_011	50.0	66.7	3	150.0	200.0	4	240.0	320.0	2.5	60.0	80.0	
0010_100	50.0	66.7	3	150.0	200.0	4.5	270.0	360.0	2.5	60.0	80.0	

Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)^{1,2}



Mode ³	PCI ((MI	Clock Hz)	CPM Multiplication	CPM (M	Clock Hz)	CPU Multiplication	CPU (M	Clock Hz)	Bus	Bus Clock (MHz)	
MODCK_H- MODCK[1-3]	Low	High	Factor ⁴	Low	High	Factor ⁵	Low	High	Factor	Low	High
1110_000	25.0	50.0	5	125.0	250.0	2.5	156.3	312.5	2	62.5	125.0
1110_001	25.0	50.0	5	125.0	250.0	3	187.5	375.0	2	62.5	125.0
1110_010	28.6	50.0	5	142.9	250.0	3.5	250.0	437.5	2	71.4	125.0
1110_011	25.0	50.0	5	125.0	250.0	4	250.0	500.0	2	62.5	125.0
1110_100	25.0	50.0	5	125.0	250.0	4	166.7	333.3	3	41.7	83.3
1110_101	25.0	50.0	5	125.0	250.0	4.5	187.5	375.0	3	41.7	83.3
1110_110	25.0	50.0	5	125.0	250.0	5	208.3	416.7	3	41.7	83.3
1110_111	25.0	50.0	5	125.0	250.0	5.5	229.2	458.3	3	41.7	83.3
1100_000						Reserved					
1100_001						Reserved					
1100_010						Reserved					

Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)^{1,2} (continued)

¹ The "low" values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The "high" values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

² PCI_MODCK determines the PCI clock frequency range. See Table 19 for higher range configurations.

³ MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

⁴ CPM multiplication factor = CPM clock/bus clock

⁵ CPU multiplication factor = Core PLL multiplication factor

8 Pinout

This figure and table show the pin assignments and pinout for the 516 PBGA package.



This figure shows the pinout of the 516 PBGA package as viewed from the top surface.



Not to Scale

Figure 12. Pinout of the 516 PBGA Package (View from Top)

This table lists the pins of the MPC8272. Note that the pins in the "MPC8272/8271 Only" column relate to Utopia functionality.

Pin Name			
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	Ball	
BR		A19	
BG/IRQ6		D2	
ABB/IRQ2		C1	



Pinout

Table 21. Pinout (continued)

Pin Name		
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	Ball
PCI_IRDY		AF15
PCI_S	STOP	AE15
PCI_D	EVSEL	AE14
PCI_I	DSEL	AC17
PCI_I	PERR	AD14
PCI_S	SERR	AD13
PCI_I	REQ0	AE20
PCI_REQ1/C	PCI_HS_ES	AF14
PCI_0	GNTO	AD20
PCI_GNT1/C	PCI_HS_LED	AE13
PCI_GNT2/CP	CI_HS_ENUM	AF21
PCI_RST		AF22
PCI_	INTA	AE21
PCI_I	REQ2	AB14
DLLOUT		AC22
PCI_AD0		AF7
PCI_AD1		AE10
PCI_AD2		AB10
PCI_AD3		AD10
PCI_AD4		AE9
PCI_AD5		AF8
PCI_	_AD6	AC10
PCI_AD7		AE11
PCI_AD8		AB11
PCI_AD9		AF10
PCI_AD10		AF9
PCI_AD11		AB12
PCI_	AD12	AC12
PCI_/	AD13	AD12
PCI	AD14	AF11
PCI_AD15		AB13



Table 21. Pinout (continued)
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Pin Name		
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	Ball
PCI_AD16		AE16
PCI_/	AD17	AF17
PCI	AD18	AD16
PCI	AD19	AC16
PCI	AD20	AF18
PCI_/	AD21	AB16
PCI_/	AD22	AD17
PCI_/	AD23	AF19
PCI_/	AD24	AB17
PCI_/	AD25	AF20
PCI_/	AD26	AE19
PCI_/	AD27	AC18
PCI_AD28		AB18
PCI_/	PCI_AD29	
PCI_AD30		AD21
PCI_/	AD31	AC20
PCI_C0/BE0		AE12
PCI_C1/BE1		AF13
PCI_C	2/BE2	AC15
PCI_C	3/BE3	AE18
IRQ0/NMI_OUT		A17
TRST ²		E21
тск		B22
TMS		C23
TDI		B24
TDO		A22
TRIS		B23
PORESET	² /PCI_RST	C24
HRE	SET	D22
SRE	SET	F22
RSTCONF		A24



Pinout

Table 21. Pinout (continued)

Pin Name		
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	Ball
PC17/CLK15/B	RG08/DONE2	T26 ³
PC18/CLK	14/TGATE2	R26 ³
PC19/CLK13/B	RG07/TGATE1	P24 ³
PC20/CLK	12/USBOE	L26 ³
PC21/CLK11/B	RGO6/CP_INT	L24 ³
PC22/CLK10/DONE3	FCC1_UT_TXPRTY	L23 ³
PC23/CLK9/BRG	GO5/DACK3/CD1	K24 ³
PC24/CLK8/TIN3/TO	UT4/DREQ2/BRGO1	K23 ³
PC25/CLK7/BRGC	04/DACK2/SPISEL	F26 ³
PC26/CLK6/T	OUT3/TMCLK	H23 ³
PC27/CLK5/BRGO3/TOUT1	FCC1_UT_RXPRTY	K22 ³
PC28/CLK4/TIN1	/TOUT2/SPICLK	D25 ³
PC29/CLK3/TIN	2/BRGO2/CTS1	F24 ³
PD7/SMSYN2	FCC1_UT_TXADDR3	AB21 ³
PD14/I	PD14/I2CSCL	
PD15/I	PD15/I2CSDA	
PD16/SPIMISO	FCC1_UT_TXPRTY	AA25 ³
PD17/BRGO2/SPIMOSI	FCC1_UT_RXPRTY	Y26 ³
PD18/SPICLK	FCC1_UT_RXADDR4	W25 ³
PD19/SPISEL/BRGO1	FCC1_UT_TXADDR4	V25 ³
PD20/RTS4/	L1RSYNCA2	R24 ³
PD21/TXD4	PD21/TXD4/L1RXD0A2	
PD22/RXD4	/L1TXD0A2	N25 ³
PD23/RTS3/USB_TP		K26 ³
PD24/TXD	PD24/TXD3/USB_TN	
PD25/RXD3/USB_RXD		J25 ³
PD29/RTS1 FCC1_UT_RXADDR		C26 ³
PD30/	TXD1	E24 ³
PD31/	/RXD1	B25 ³
VCC	VCCSYN	
VCCSYN1		К6



Pin Name			
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	Ball	
CLK	IN2	C21	
No cor	nnect ⁴	D19 ⁴ , J3 ⁴ , AD24 ⁵	
I/O po	ower	B4, F3, J2, N4, AD1, AD5, AE8, AC13, AD18, AB24, AB26, W23, R25, M25, F25, C25, C22, B17, B12, B8, E6, F6, H6, L5, L6, P6, T6, U6, V5, Y5, AA6, AA8, AA10, AA11, AA14, AA16, AA17, AB19, AB20, W21, U21, T21, P21, N21, M22, J22, H21, F21, F19, F17, E16, F14, E13, E12, F10, E10, E9	
Core F	Power	F5, K5, M5, AA5, AB7, AA13, AA19, AA21, Y22, AC25, U22, R22, L21, H22, E22, E20, E15, F13, F11, F8, L3, V4, W3, AC11, AD11, AB15, U25, T24, J24, H25, F23, B19, D17, C17, D10, C10	
Gro	und	E19, E2, K1, Y2, AE1, AE4, AD9, AC14, AE17, AC19, AE25, V24, P26, M26, G26, E26, B21, C12, C11, C8, A8, B18, A18, A2, B1, B2, A5, C5, D4, D6, G2, L4, P1, R1, R4, AC4, AE7, AC23, Y25, N24, J23, A23, D23, D20, E18, A13, A16, K10, K11, K12, K13, K14, K15, K16, K17, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, R10, R11, R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17	

Table 21. Pinout (continued)

¹ Must be tied to ground.

 2 Should be tied to VDDH via a 2K Ω external pull-up resistor.

³ The default configuration of the CPM pins (PA[8–31], PB[18–31], PC[0–1,4–29], PD[7–25, 29–31]) is input. To prevent excessive DC current, it is recommended either to pull unused pins to GND or VDDH, or to configure them as outputs.

⁴ This pin is not connected. It should be left floating.

⁵ Must be pulled down or left floating



9.2 Mechanical Dimensions

This figure provides the mechanical dimensions and bottom surface nomenclature of the 516 PBGA package.



Figure 14. Mechanical Dimensions and Bottom Surface Nomenclature—516 PBGA



Ordering Information

10 Ordering Information

This figure provides an example of the Freescale part numbering nomenclature for the SoC. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.



Figure 15. Freescale Part Number Key

11 Document Revision History

This table summarizes changes to this document.

Table 23.	Document	Revision	History
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Revision	Date	Substantive Changes
3	09/2011	In Figure 15, "Freescale Part Number Key," added speed decoding information below processor frequency information.
2	12/2008	 Modified Figure 5, "SCC/SMC/SPI/I2C External Clock Diagram," and added second section of figure notes. In Table 12, modified "Data bus in pipeline mode" row and showed 66 MHz as "N/A." In Section 10, "Ordering Information," added "F = 133" to CPU/CPM/Bus Frequency. Added footnote concerning CPM_CLK/PCI_CLK ratio to column "PCI Division Factor" in Table 17, "Clock Configurations for PCI Host Mode (PCI_MODCK=0)," and Table 18, "Clock Configurations for PCI Host Mode (PCI_MODCK=1),." Removed overbar from DLL_ENABLE in Table 21, "Pinout."
1.5	12/2006	• Section 6, "AC Electrical Characteristics," removed deratings statement and clarified AC timing descriptions.
1.4	05/2006	Added row for 133 MHz configurations to Table 8.
1.3	02/2006	Inserted Section 6.3, "JTAG Timings."



Document Revision History

Revision	Date	Substantive Changes
0.2	12/2003	 Table 1: New Table 2: New Table 4: Modification of VDD and VCCSYN to 1.45–1.60 V Table 8: Addition of note 2 regarding TRST and PORESET (see V_{IH} row of Table 8) Table 8: Addition of note 2 regarding TRST and PORESET (see V_{IH} row of Table 8) Table 8: Addition of note 2 regarding TRST and PORESET (see V_{IH} row of Table 8) Table 8: Addition of note 2 regarding TRST and PORESET (see V_{IH} row of Table 8) Table 8: Addition of note 2 regarding TRST and PORESET (see V_{IH} row of Table 8) Table 8: Addition of note 2 regarding TRST and PORESET (see V_{IH} row of Table 8) Table 8: Addition of POL_GNT1 (AE13) CPCI_HS_ENUM to POL_GNT2 (AF21) Table 8: Addition of POL_GNT2 (AF21) Table 8: Addition of POWerQUICO II devices: PCI_CFG0 (PCI_HOST_EN) (AC21) PCI_CFG2 (DLL_ENABLE) (AE22) PCI_CCG2 (DLL_ENABLE) (AE23) PCI_RD7 (AF16) PCI_TRD7 (AF16) PCI_TRD7 (AF16) PCI_TRD7 (AF16) PCI_DEV (AF15) PCI_COSTOP (AE15) DEVSEL (AC17) PCI_DERE (AD13) PCI_REQO-2 (AAE20, AF14, AB14) PCI_GINT0-2 (AD20, AE13, AF21) PCI_CO-3 (AE12, AF13, AC15, AE18) PCI_CABD-31 Table 8: Addition of R_{0,IT} and note 4 Sections 4: 1-4.5 and 4.7 on thermal characteristics: New Section 7, "Clock Configuration Modes": Modification to first paragraph. Note that PCI_MODCK is a bit in the Hard Reset Configuration Word. It is not an input signal as it is in the MPCR280 Family. Addition of These 1 to TRST (E21) and PORESET (C24) Table 21: Addition of These (AD24). This pin is now a "No connect." Note 5 unchanged. Table 21: Removal of Thermal0 (D19) and Thermal1(J3). These pins are now "No connects." Note 4 unchanged. Table 21: Removal of Spare0 (AD24). This pin is now a "No connect." Note 5 unchanged.
0.1	9/2003	 Addition of the MPC8271 and the MPC8247 (these devices do not have a security engine) Table 8: Addition of note 2 to V_{IH} Table 8: Changed I_{OL} for 60x signals to 6.0 mA Modification of note 1 for Table 17, Table 18, Table 19, and Table 20 Table 21: Addition of ball AD9 to GND. In rev 0 of this document, AD8 was listed as assigned to both CS5 and GND. AD8 is only assigned to CS5. Table 21: Addition of note 4 to Thermal0 (D19) and Thermal1(J3) Addition of ZQ package code to Figure 15
0	5/2003	NDA release

Table 23. Document Revision History (continued)

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