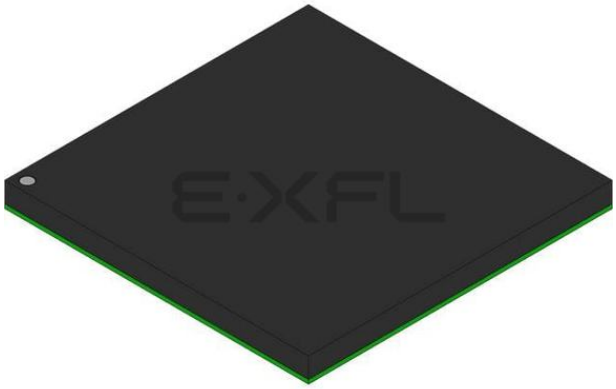

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PowerPC G2_LE |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 400MHz |
| Co-Processors/DSP | Communications; RISC CPM, Security; SEC |
| RAM Controllers | DRAM, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100Mbps (2) |
| SATA | - |
| USB | USB 2.0 (1) |
| Voltage - I/O | 3.3V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 516-BBGA |
| Supplier Device Package | 516-PBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8272cvrtiea |

# 1 Overview

This table shows the functionality supported by each SoC in the MPC8272 family.

**Table 1. MPC8272 PowerQUICC II Family Functionality**

| Functionality | SoCs | | | |
|---|---|---|---|---|
| | MPC8272 | MPC8248 | MPC8271 | MPC8247 |
| Package[1] | 516 PBGA | | | |
| Serial communications controllers (SCCs) | 3 | 3 | 3 | 3 |
| QUICC multi-channel controller (QMC) | Yes | Yes | Yes | Yes |
| Fast communication controllers (FCCs) | 2 | 2 | 2 | 2 |
| I-Cache (Kbyte) | 16 | 16 | 16 | 16 |
| D-Cache (Kbyte) | 16 | 16 | 16 | 16 |
| Ethernet (10/100) | 2 | 2 | 2 | 2 |
| UTOPIA II Ports | 1 | 0 | 1 | 0 |
| Multi-channel controllers (MCCs) | 0 | 0 | 0 | 0 |
| PCI bridge | Yes | Yes | Yes | Yes |
| Transmission convergence (TC) layer | — | — | — | — |
| Inverse multiplexing for ATM (IMA) | — | — | — | — |
| Universal serial bus (USB) 2.0 full/low rate | 1 | 1 | 1 | 1 |
| Security engine (SEC) | Yes | Yes | — | — |

[1] See Table 2.

Devices in the MPC8272 family are available in two packages—the VR or ZQ package—as shown in . For package ordering information, see Section 10, “Ordering Information.”

**Table 2. MPC8272 PowerQUICC II Device Packages**

| Code (Package) | VR (516 PBGA—Lead free) | ZQ (516 PBGA—Lead spheres) |
|---|---|---|
| Device | MPC8272VR | MPC8272ZQ |
| | MPC8248VR | MPC8248ZQ |
| | MPC8271VR | MPC8271ZQ |
| | MPC8247VR | MPC8247ZQ |

This figure shows the block diagram of the SoC.

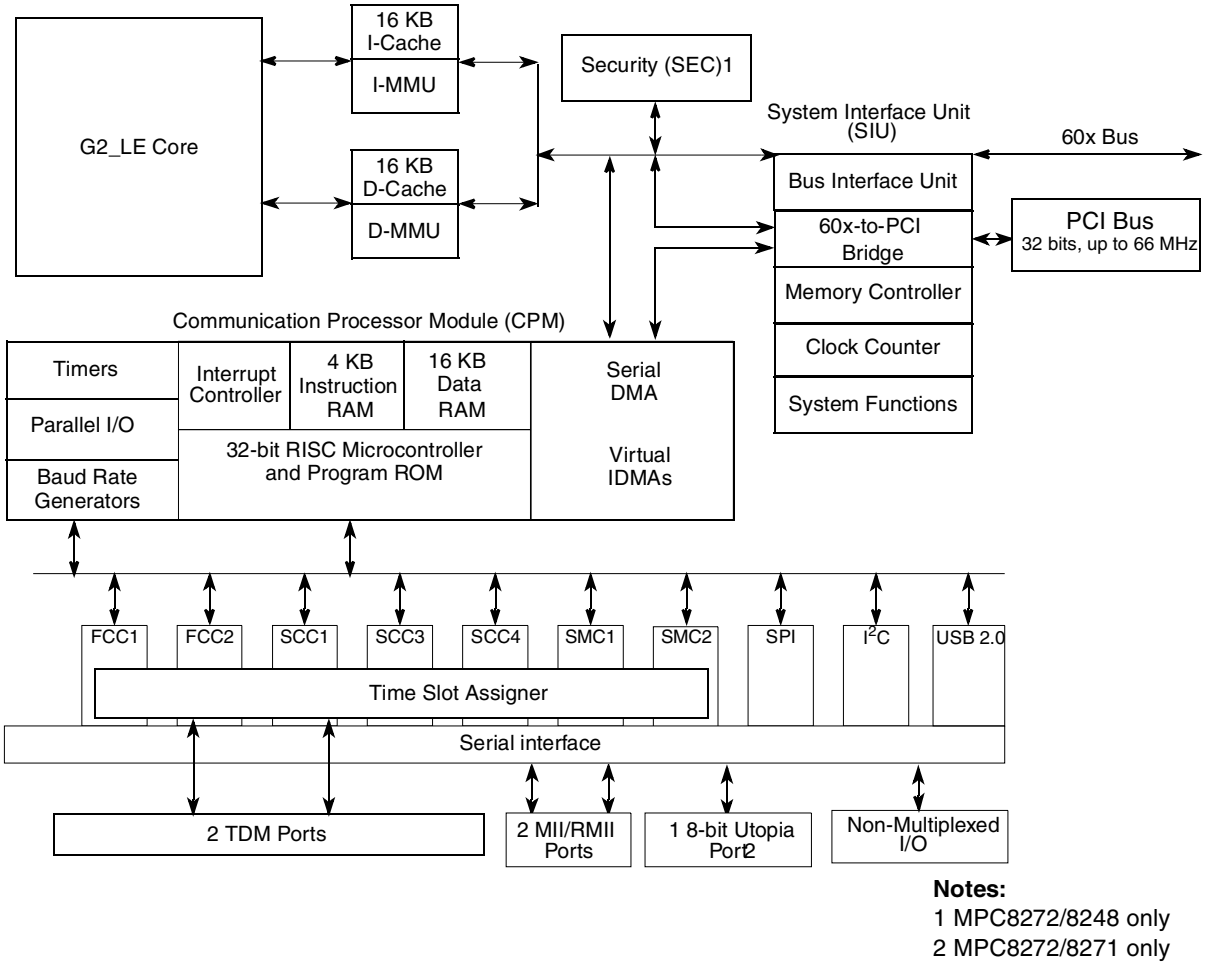



**Figure 1. SoC Block Diagram**

## 1.1 Features

The major features of the SoC are as follows:

- Dual-issue integer (G2_LE) core
  - A core version of the MPC603e microprocessor
  - System core microprocessor supporting frequencies of 266–400 MHz
  - Separate 16 KB data and instruction caches:
    - Four-way set associative
    - Physically addressed
    - LRU replacement algorithm
  - Power Architecture®-compliant memory management unit (MMU)
  - Common on-chip processor (COP) test interface
  - Supports bus snooping for cache coherency

This table lists recommended operational voltage conditions.

**Table 4. Recommended Operating Conditions[1]**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Core supply voltage | VDD | 1.425 – 575 | V |
| PLL supply voltage | VCCSYN | 1.425 – 575 | V |
| I/O supply voltage | VDDH | 3.135 – 3.465 | V |
| Input voltage | VIN | GND (–0.3) – 3.465 | V |
| Junction temperature (maximum) | $T_j$ | 105[2] | °C |
| Ambient temperature | $T_A$ | 0–70[2] | °C |

1 **Caution:** These are the recommended and tested operating conditions. Proper operation outside of these conditions is not guaranteed.

2 Note that for extended temperature parts the range is $(-40)_{T_A}$ – $105_{T_j}$.

This SoC contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or $V_{CC}$).

This figure shows the undershoot and overshoot voltage of the 60x bus memory interface of the SoC. Note that in PCI mode the I/O interface is different.

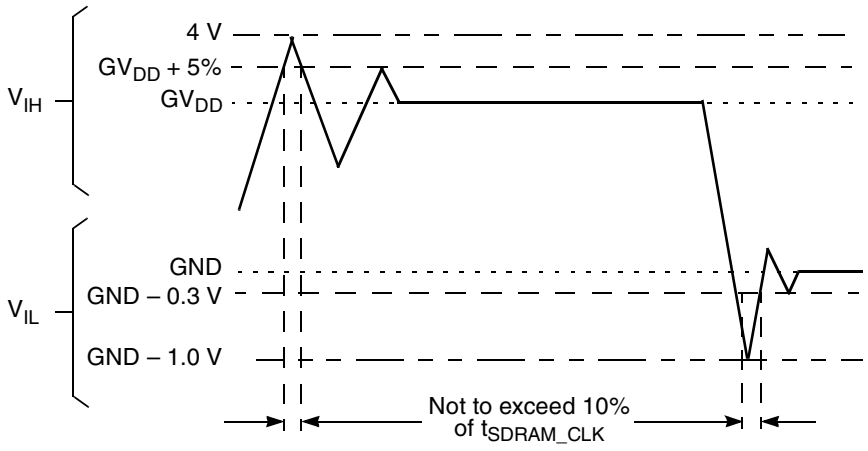



**Figure 2. Overshoot/Undershoot Voltage**

# 3 DC Electrical Characteristics

This table shows DC electrical characteristics.

**Table 5. DC Electrical Characteristics[1]**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input high voltage—all inputs except TCK, $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$[2] | $V_{IH}$ | 2.0 | 3.465 | V |
| Input low voltage[3] | $V_{IL}$ | GND | 0.8 | V |
| CLKIN input high voltage | $V_{IHC}$ | 2.4 | 3.465 | V |
| CLKIN input low voltage | $V_{ILC}$ | GND | 0.4 | V |
| Input leakage current, $V_{IN}$ = VDDH[4] | $I_{IN}$ | — | 10 | μA |
| Hi-Z (off state) leakage current, $V_{IN}$ = VDDH[2] | $I_{OZ}$ | — | 10 | μA |
| Signal low input current, $V_{IL}$ = 0.8 V | $I_L$ | — | 1 | μA |
| Signal high input current, $V_{IH}$ = 2.0 V | $I_H$ | — | 1 | μA |
| Output high voltage, $I_{OH}$ = –2 mA<br>except UTOPIA mode, and open drain pins<br><br>In UTOPIA mode[5] (UTOPIA pins only): $I_{OH}$ = -8.0mA<br>PA[8–31]<br>PB[18–31]<br>PC[0–1,4–29]<br>PD[7–25, 29–31] | $V_{OH}$ | 2.4 | — | V |
| In UTOPIA mode[5] (UTOPIA pins only): $I_{OL}$ = 8.0mA<br>PA[8–31]<br>PB[18–31]<br>PC[0–1,4–29]<br>PD[7–25, 29–31] | $V_{OL}$ | — | 0.5 | V |

**Table 5. DC Electrical Characteristics[1] (continued)**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| $I_{OL}$ = 5.3mA<br>CS[0–5]<br>CS6/BCTL1/SMI<br>CS7/TLBSYNC<br>BADDR27/ IRQ1<br>BADDR28/ IRQ2<br>ALE/ IRQ4<br>BCTL0<br>PWE[0–7]/PSDDQM[0–7]/PBS[0–7]<br>PSDA10/PGPL0<br>PSDWE/PGPL1<br>POE/PSDRAS/PGPL2<br>PSDCAS/PGPL3<br>PGTA/PUPMWAIT/PGPL4<br>PSDAMUX/PGPL5<br>PCI_CFG0 (PCI_HOST_EN)<br>PCI_CFG1 (PCI_ARB_EN)<br>PCI_CFG2 (DLL_ENABLE)<br>MODCK1/RSRV/TC(0)/BNKSEL(0)<br>MODCK2/CSE0/TC(1)/BNKSEL(1)<br>MODCK3CSE1/TC(2)/BNKSEL(2) | $V_{OL}$ | — | 0.4 | V |
| $I_{OL}$ = 3.2mA<br>PCI_PAR<br>PCI_FRAME<br>PCI_TRDY<br>PCI_IRDY<br>PCI_STOP<br>PCI_DEVSEL<br>PCI_IDSEL<br>PCI_PERR<br>PCI_SERR<br>PCI_REQ0<br>PCI_REQ1/ CPI_HS_ES<br>PCI_GNT0<br>PCI_GNT1/ CPI_HS_LES<br>PCI_GNT2/ CPI_HS_ENUM<br>PCI_RST<br>PCI_INTA<br>PCI_REQ2<br>DLLOUT<br>PCI_AD(0-31)<br>PCI_C(0–3)/BE(0-3)<br>PA[8–31]<br>PB[18–31]<br>PC[0–1,4–29]<br>PD[7–25, 29–31]<br>TDO | | | | |

1 The default configuration of the CPM pins (PA[8–31], PB[18–31], PC[0–1,4–29], PD[7–25, 29–31]) is input. To prevent excessive DC current, it is recommended either to pull unused pins to GND or VDDH, or to configure them as outputs.

2 TCK, TRST and PORESET have min VIH = 2.5V.

3 $V_{IL}$ for IIC interface does not match IIC standard, but does meet IIC standard for $V_{OL}$ and should not cause any compatibility issue.

4 The leakage current is measured for nominal VDDH,VCCSYN, and VDD.

This table lists CPM input characteristics.

**NOTE: Rise/Fall Time on CPM Input Pins**

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

**Table 11. AC Characteristics for CPM Inputs[1]**

| Spec Number | | Characteristic | Value (ns) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Setup | | | | Hold | | | |
| Setup | Hold | | 66 MHz | 83 MHz | 100 MHz | 133 MHz | 66 MHz | 83 MHz | 100 MHz | 133 MHz |
| sp16a | sp17a | FCC inputs—internal clock (NMSI) | 6 | 6 | 6 | 6 | 0 | 0 | 0 | 0 |
| sp16b | sp17b | FCC inputs—external clock (NMSI) | 2.5 | 2.5 | 2.5 | 2.5 | 2 | 2 | 2 | 2 |
| sp18a | sp19a | SCC/SMC/SPI/I2C inputs—internal clock (NMSI) | 6 | 6 | 6 | 6 | 0 | 0 | 0 | 0 |
| sp18b | sp19b | SCC/SMC/SPI/I2C inputs—external clock (NMSI) | 4 | 4 | 4 | 4 | 2 | 2 | 2 | 2 |
| sp20 | sp21 | TDM inputs/SI | 3 | 3 | 3 | 3 | 2.5 | 2.5 | 2.5 | 2.5 |
| sp22 | sp23 | PIO/TIMER/IDMA inputs | 8 | 8 | 8 | 8 | 0.5 | 0.5 | 0.5 | 0.5 |

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

**NOTE**

Although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the FCC internal clock.

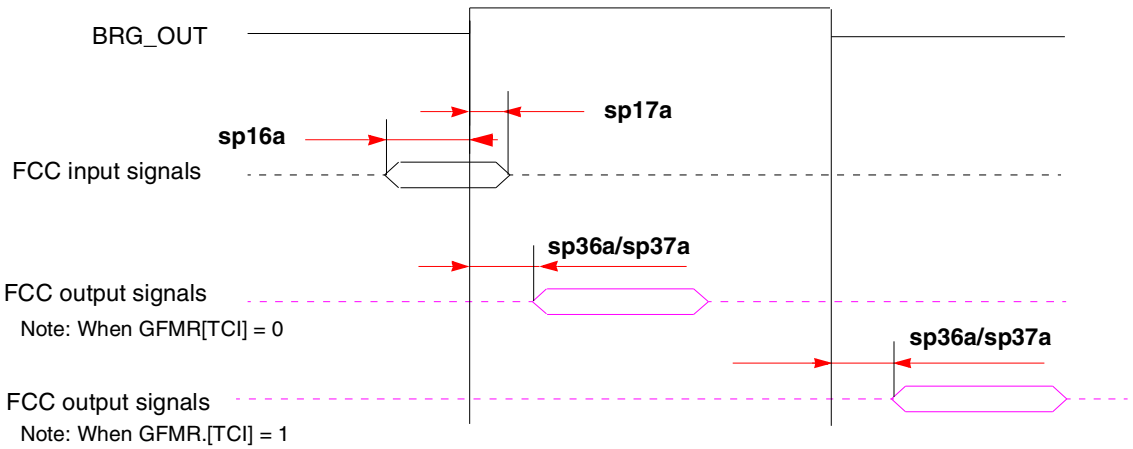



**Figure 3. FCC Internal Clock Diagram**

This figure shows the FCC external clock.

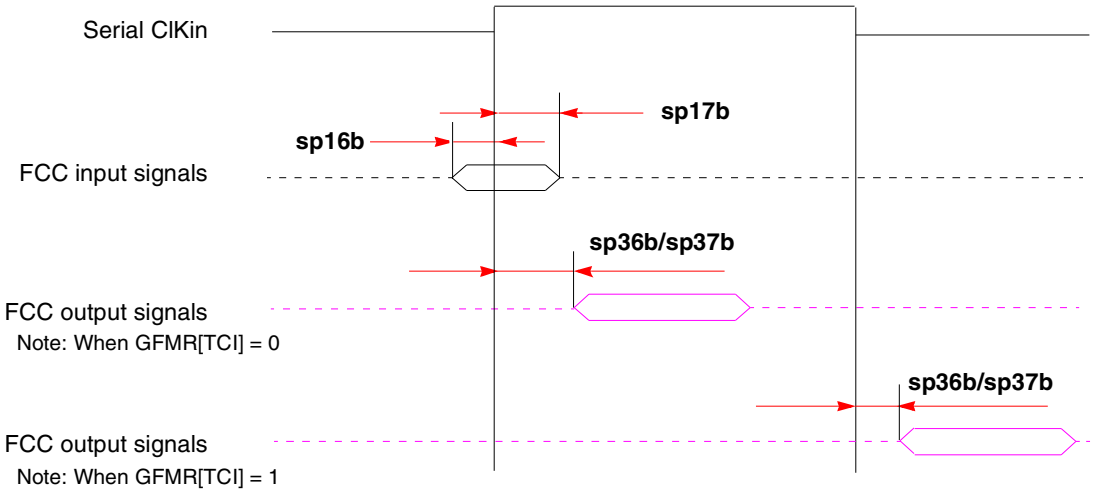
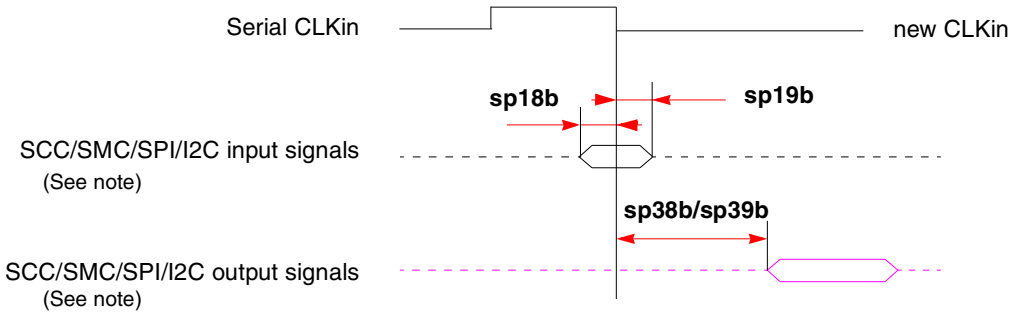



**Figure 4. FCC External Clock Diagram**

This figure shows the SCC/SMC/SPI/$I^2C$ external clock.




**Note:** There are four possible timing conditions for SPI:
1. Input sampled on the rising edge and output driven on the rising edge.
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge (shown).
4. Input sampled on the falling edge and output driven on the rising edge.

**Note:** There are two possible timing conditions for SCC/SMC/$I^2C$:
1. Input sampled on the falling edge and output driven on the falling edge (shown).
2. Input sampled on the falling edge and output driven on the rising edge.

**Figure 5. SCC/SMC/SPI/$I^2C$ External Clock Diagram**

**NOTE**

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin's rising edge.

## 6.3 JTAG Timings

This table lists the JTAG timings.

**Table 15. JTAG Timings[1]**

| Parameter | Symbol[2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| JTAG external clock frequency of operation | $f_{JTG}$ | 0 | 33.3 | MHz | — |
| JTAG external clock cycle time | $t_{JTG}$ | 30 | — | ns | — |
| JTAG external clock pulse width measured at 1.4V | $t_{JTKHKL}$ | 15 | — | ns | — |
| JTAG external clock rise and fall times | $t_{JTGR}$ and $t_{JTGF}$ | 0 | 5 | ns | 6 |
| TRST assert time | $t_{TRST}$ | 25 | — | ns | 3, 6 |
| Input setup times<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDVKH}$<br>$t_{JTIVKH}$ | <br>4<br>4 | <br>—<br>— | <br>ns<br>ns | <br>4, 7<br>4, 7 |
| Input hold times<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDXKH}$<br>$t_{JTIXKH}$ | <br>10<br>10 | <br>—<br>— | <br>ns<br>ns | <br>4, 7<br>4, 7 |
| Output valid times<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDV}$<br>$t_{JTKLOV}$ | <br>—<br>— | <br>10<br>10 | <br>ns<br>ns | <br>5, 7<br>5, 7 |
| Output hold times<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDX}$<br>$t_{JTKLOX}$ | <br>1<br>1 | <br>—<br>— | <br>ns<br>ns | <br>5, 7<br>5, 7 |
| JTAG external clock to output high impedance<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDZ}$<br>$t_{JTKLOZ}$ | <br>1<br>1 | <br>10<br>10 | <br>ns<br>ns | <br>5, 6<br>5, 6 |

1 All outputs are measured from the midpoint voltage of the falling/rising edge of $t_{TCLK}$ to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2 The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{JTDVKH}$ symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{JTDXKH}$ symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

3 TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

4 Non-JTAG signal input timing with respect to $t_{TCLK}$.

5 Non-JTAG signal output timing with respect to $t_{TCLK}$.

6 Guaranteed by design.

7 Guaranteed by design and device characterization.

**Table 17. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 0100_001 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 6 | 300.0 | 400.0 | 6 | 50.0 | 66.7 |
| 0100_010 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 7 | 350.0 | 466.6 | 6 | 50.0 | 66.7 |
| 0100_011 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 8 | 400.0 | 533.3 | 6 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0101_000 | 60.0 | 66.7 | 2 | 120.0 | 133.3 | 2.5 | 150.0 | 166.7 | 2 | 60.0 | 66.7 |
| 0101_001 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 3 | 150.0 | 200.0 | 2 | 50.0 | 66.7 |
| 0101_010 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 3.5 | 175.0 | 233.3 | 2 | 50.0 | 66.7 |
| 0101_011 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 4 | 200.0 | 266.6 | 2 | 50.0 | 66.7 |
| 0101_100 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 4.5 | 225.0 | 300.0 | 2 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0101_101 | 83.3 | 111.1 | 3 | 250.0 | 333.3 | 3.5 | 291.7 | 388.9 | 5 | 50.0 | 66.7 |
| 0101_110 | 83.3 | 111.1 | 3 | 250.0 | 333.3 | 4 | 333.3 | 444.4 | 5 | 50.0 | 66.7 |
| 0101_111 | 83.3 | 111.1 | 3 | 250.0 | 333.3 | 4.5 | 375.0 | 500.0 | 5 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0110_000 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 2.5 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0110_001 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 3 | 50.0 | 66.7 |
| 0110_010 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 3 | 50.0 | 66.7 |
| 0110_011 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 4 | 240.0 | 320.0 | 3 | 50.0 | 66.7 |
| 0110_100 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 4.5 | 270.0 | 360.0 | 3 | 50.0 | 66.7 |
| 0110_101 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 5 | 300.0 | 400.0 | 3 | 50.0 | 66.7 |
| 0110_110 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 6 | 360.0 | 480.0 | 3 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0111_000 | Reserved | | | | | | | | | | |
| 0111_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0111_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 175.0 | 233.3 | 3 | 50.0 | 66.7 |
| 0111_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 200.0 | 266.6 | 3 | 50.0 | 66.7 |
| 0111_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4.5 | 225.0 | 300.0 | 3 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1000_000 | Reserved | | | | | | | | | | |
| 1000_001 | 66.7 | 88.9 | 3 | 200.0 | 266.6 | 3 | 200.0 | 266.6 | 4 | 50.0 | 66.7 |

**Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 0100_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 6 | 150.0 | 300.0 | 6 | 25.0 | 50.0 |
| 0100_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 7 | 175.0 | 350.0 | 6 | 25.0 | 50.0 |
| 0100_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 8 | 200.0 | 400.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0101_000 | 60.0 | 100.0 | 2 | 120.0 | 200.0 | 2.5 | 150.0 | 250.0 | 4 | 30.0 | 50.0 |
| 0101_001 | 50.0 | 100.0 | 2 | 100.0 | 200.0 | 3 | 150.0 | 300.0 | 4 | 25.0 | 50.0 |
| 0101_010 | 50.0 | 100.0 | 2 | 100.0 | 200.0 | 3.5 | 175.0 | 350.0 | 4 | 25.0 | 50.0 |
| 0101_011 | 50.0 | 100.0 | 2 | 100.0 | 200.0 | 4 | 200.0 | 400.0 | 4 | 25.0 | 50.0 |
| 0101_100 | 50.0 | 100.0 | 2 | 100.0 | 200.0 | 4.5 | 225.0 | 450.0 | 4 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0101_101 | 42.9 | 83.3 | 3 | 128.6 | 250.0 | 3.5 | 150.0 | 291.7 | 5 | 25.7 | 50.0 |
| 0101_110 | 41.7 | 83.3 | 3 | 125.0 | 250.0 | 4 | 166.7 | 333.3 | 5 | 25.0 | 50.0 |
| 0101_111 | 41.7 | 83.3 | 3 | 125.0 | 250.0 | 4.5 | 187.5 | 375.0 | 5 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0110_000 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 2.5 | 150.0 | 300.0 | 6 | 25.0 | 50.0 |
| 0110_001 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 3 | 180.0 | 360.0 | 6 | 25.0 | 50.0 |
| 0110_010 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 6 | 25.0 | 50.0 |
| 0110_011 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 4 | 240.0 | 480.0 | 6 | 25.0 | 50.0 |
| 0110_100 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 4.5 | 270.0 | 540.0 | 6 | 25.0 | 50.0 |
| 0110_101 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 5 | 300.0 | 600.0 | 6 | 25.0 | 50.0 |
| 0110_110 | 60.0 | 120.0 | 2.5 | 150.0 | 300.0 | 6 | 360.0 | 720.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0111_000 | Reserved | | | | | | | | | | |
| 0111_001 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 3 | 150.0 | 300.0 | 6 | 25.0 | 50.0 |
| 0111_010 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 3.5 | 175.0 | 350.0 | 6 | 25.0 | 50.0 |
| 0111_011 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 6 | 25.0 | 50.0 |
| 0111_100 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 4.5 | 225.0 | 450.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1000_000 | Reserved | | | | | | | | | | |
| 1000_001 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 3 | 200.0 | 400.0 | 8 | 25.0 | 50.0 |

**Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1000_010 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 3.5 | 233.3 | 466.7 | 8 | 25.0 | 50.0 |
| 1000_011 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 4 | 266.7 | 533.3 | 8 | 25.0 | 50.0 |
| 1000_100 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 4.5 | 300.0 | 600.0 | 8 | 25.0 | 50.0 |
| 1000_101 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 6 | 400.0 | 800.0 | 8 | 25.0 | 50.0 |
| 1000_110 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 6.5 | 433.3 | 866.7 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1001_000 | Reserved | | | | | | | | | | |
| 1001_001 | Reserved | | | | | | | | | | |
| 1001_010 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 3.5 | 200.0 | 400.0 | 8 | 25.0 | 50.0 |
| 1001_011 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 4 | 228.6 | 457.1 | 8 | 25.0 | 50.0 |
| 1001_100 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 4.5 | 257.1 | 514.3 | 8 | 25.0 | 50.0 |
| 1001_101 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 5 | 214.3 | 428.6 | 6 | 25.0 | 50.0 |
| 1001_110 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 5.5 | 235.7 | 471.4 | 6 | 25.0 | 50.0 |
| 1001_111 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 6 | 257.1 | 514.3 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1010_000 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 2 | 150.0 | 300.0 | 6 | 25.0 | 50.0 |
| 1010_001 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 2.5 | 187.5 | 375.0 | 6 | 25.0 | 50.0 |
| 1010_010 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 3 | 225.0 | 450.0 | 6 | 25.0 | 50.0 |
| 1010_011 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 3.5 | 262.5 | 525.0 | 6 | 25.0 | 50.0 |
| 1010_100 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 4 | 300.0 | 600.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1010_101 | 100.0 | 200.0 | 2 | 200.0 | 400.0 | 2.5 | 250.0 | 500.0 | 8 | 25.0 | 50.0 |
| 1010_110 | 100.0 | 200.0 | 2 | 200.0 | 400.0 | 3 | 300.0 | 600.0 | 8 | 25.0 | 50.0 |
| 1010_111 | 100.0 | 200.0 | 2 | 200.0 | 400.0 | 3.5 | 350.0 | 700.0 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1011_000 | Reserved | | | | | | | | | | |
| 1011_001 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 2.5 | 200.0 | 400.0 | 8 | 25.0 | 50.0 |
| 1011_010 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 3 | 240.0 | 480.0 | 8 | 25.0 | 50.0 |
| 1011_011 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 3.5 | 280.0 | 560.0 | 8 | 25.0 | 50.0 |
| 1011_100 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 4 | 320.0 | 640.0 | 8 | 25.0 | 50.0 |

6 CPM_CLK/PCI_CLK ratio. When PCI_MODCK = 1, the ratio of CPM_CLK/PCI_CLK should be calculated from PCIDF as follows:
PCIDF = 3 > CPM_CLK/PCI_CLK = 4
PCIDF = 5 > CPM_CLK/PCI_CLK = 6
PCIDF = 7 > CPM_CLK/PCI_CLK = 8
PCIDF = 9 > CPM_CLK/PCI_CLK = 5
PCIDF = B > CPM_CLK/PCI_CLK = 6

## 7.2 PCI Agent Mode

These tables show configurations for PCI agent mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device. Note that in PCI agent mode the input clock is PCI clock.

**Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2]**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| **Default Modes (MODCK_H=0000)** | | | | | | | | | | | |
| 0000_000 | 60.0 | 66.7 | 2 | 120.0 | 133.3 | 2.5 | 150.0 | 166.7 | 2 | 60.0 | 66.7 |
| 0000_001 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 3 | 150.0 | 200.0 | 2 | 50.0 | 66.7 |
| 0000_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0000_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 200.0 | 266.6 | 3 | 50.0 | 66.7 |
| 0000_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 2.5 | 60.0 | 80.0 |
| 0000_101 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 2.5 | 60.0 | 80.0 |
| 0000_110 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 233.3 | 311.1 | 3 | 66.7 | 88.9 |
| 0000_111 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 240.0 | 320.0 | 2.5 | 80.0 | 106.7 |
| **Full Configuration Modes** | | | | | | | | | | | |
| 0001_001 | 60.0 | 66.7 | 2 | 120.0 | 133.3 | 5 | 150.0 | 166.7 | 4 | 30.0 | 33.3 |
| 0001_010 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 6 | 150.0 | 200.0 | 4 | 25.0 | 33.3 |
| 0001_011 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 7 | 175.0 | 233.3 | 4 | 25.0 | 33.3 |
| 0001_100 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 8 | 200.0 | 266.6 | 4 | 25.0 | 33.3 |
| | | | | | | | | | | | |
| 0010_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 2.5 | 60.0 | 80.0 |
| 0010_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 2.5 | 60.0 | 80.0 |
| 0010_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 240.0 | 320.0 | 2.5 | 60.0 | 80.0 |
| 0010_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4.5 | 270.0 | 360.0 | 2.5 | 60.0 | 80.0 |
| | | | | | | | | | | | |

**Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 0100_100 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4.5 | 225.0 | 450.0 | 3 | 50.0 | 100.0 |
| | | | | | | | | | | | |
| 0101_000 | 30.0 | 50.0 | 5 | 150.0 | 250.0 | 2.5 | 150.0 | 250.0 | 2.5 | 60.0 | 100.0 |
| 0101_001 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 3 | 150.0 | 300.0 | 2.5 | 50.0 | 100.0 |
| 0101_010 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 3.5 | 175.0 | 350.0 | 2.5 | 50.0 | 100.0 |
| 0101_011 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 4 | 200.0 | 400.0 | 2.5 | 50.0 | 100.0 |
| 0101_100 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 4.5 | 225.0 | 450.0 | 2.5 | 50.0 | 100.0 |
| 0101_101 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 5 | 250.0 | 500.0 | 2.5 | 50.0 | 100.0 |
| 0101_110 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 5.5 | 275.0 | 550.0 | 2.5 | 50.0 | 100.0 |
| | | | | | | | | | | | |
| 0110_000 | Reserved | | | | | | | | | | |
| 0110_001 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3 | 200.0 | 400.0 | 3 | 66.7 | 133.3 |
| 0110_010 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3.5 | 233.3 | 466.7 | 3 | 66.7 | 133.3 |
| 0110_011 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4 | 266.7 | 533.3 | 3 | 66.7 | 133.3 |
| 0110_100 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4.5 | 300.0 | 600.0 | 3 | 66.7 | 133.3 |
| | | | | | | | | | | | |
| 0111_000 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 2 | 150.0 | 300.0 | 2 | 75.0 | 150.0 |
| 0111_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 2.5 | 187.5 | 375.0 | 2 | 75.0 | 150.0 |
| 0111_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 225.0 | 450.0 | 2 | 75.0 | 150.0 |
| 0111_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 262.5 | 525.0 | 2 | 75.0 | 150.0 |
| | | | | | | | | | | | |
| 1000_000 | Reserved | | | | | | | | | | |
| 1000_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 2.5 | 150.0 | 300.0 | 2.5 | 60.0 | 120.0 |
| 1000_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 180.0 | 360.0 | 2.5 | 60.0 | 120.0 |
| 1000_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 2.5 | 60.0 | 120.0 |
| 1000_100 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 240.0 | 480.0 | 2.5 | 60.0 | 120.0 |
| 1000_101 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4.5 | 270.0 | 540.0 | 2.5 | 60.0 | 120.0 |
| | | | | | | | | | | | |
| 1001_000 | Reserved | | | | | | | | | | |
| 1001_001 | Reserved | | | | | | | | | | |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| A30 | | B15 |
| A31 | | A15 |
| TT0 | | B3 |
| TT1 | | E8 |
| TT2 | | D7 |
| TT3 | | C4 |
| TT4 | | E7 |
| $\overline{\text{TBST}}$ | | E3 |
| TSIZ0 | | E4 |
| TSIZ1 | | E5 |
| TSIZ2 | | C3 |
| TSIZ3 | | D5 |
| $\overline{\text{AACK}}$ | | D3 |
| $\overline{\text{ARTRY}}$ | | C2 |
| $\overline{\text{DBG}}$/$\overline{\text{IRQ7}}$ | | F16 |
| $\overline{\text{DBB}}$/$\overline{\text{IRQ3}}$ | | D18 |
| D0 | | AC1 |
| D1 | | AA1 |
| D2 | | V3 |
| D3 | | R5 |
| D4 | | P4 |
| D5 | | M4 |
| D6 | | J4 |
| D7 | | G1 |
| D8 | | W6 |
| D9 | | Y3 |
| D10 | | V1 |
| D11 | | N6 |
| D12 | | P3 |
| D13 | | M2 |
| D14 | | J5 |

Table 21. Pinout (continued)

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| D15 | | G3 |
| D16 | | AB3 |
| D17 | | Y1 |
| D18 | | T4 |
| D19 | | T3 |
| D20 | | P2 |
| D21 | | M1 |
| D22 | | J1 |
| D23 | | G4 |
| D24 | | AB2 |
| D25 | | W4 |
| D26 | | V2 |
| D27 | | T1 |
| D28 | | N5 |
| D29 | | L1 |
| D30 | | H1 |
| D31 | | G5 |
| D32 | | W5 |
| D33 | | W2 |
| D34 | | T5 |
| D35 | | T2 |
| D36 | | N1 |
| D37 | | K3 |
| D38 | | H2 |
| D39 | | F1 |
| D40 | | AA2 |
| D41 | | W1 |
| D42 | | U3 |
| D43 | | R2 |
| D44 | | N2 |
| D45 | | L2 |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| $\overline{\text{CS2}}$ | | AF5 |
| $\overline{\text{CS3}}$ | | AC8 |
| $\overline{\text{CS4}}$ | | AF6 |
| $\overline{\text{CS5}}$ | | AD8 |
| $\overline{\text{CS6}}$/BCTL1/$\overline{\text{SMI}}$ | | AC9 |
| $\overline{\text{CS7}}$/TLBISYNC | | AB9 |
| BADDR27/$\overline{\text{IRQ1}}$ | | AB8 |
| BADDR28/$\overline{\text{IRQ2}}$ | | AC7 |
| ALE/$\overline{\text{IRQ4}}$ | | AF4 |
| $\overline{\text{BCTL0}}$ | | AF3 |
| $\overline{\text{PWE0}}$/$\overline{\text{PSDDQM0}}$/$\overline{\text{PBS0}}$ | | AD6 |
| $\overline{\text{PWE1}}$/$\overline{\text{PSDDQM1}}$/$\overline{\text{PBS1}}$ | | AE5 |
| $\overline{\text{PWE2}}$/$\overline{\text{PSDDQM2}}$/$\overline{\text{PBS2}}$ | | AE3 |
| $\overline{\text{PWE3}}$/$\overline{\text{PSDDQM3}}$/$\overline{\text{PBS3}}$ | | AF2 |
| $\overline{\text{PWE4}}$/$\overline{\text{PSDDQM4}}$/$\overline{\text{PBS4}}$ | | AC6 |
| $\overline{\text{PWE5}}$/$\overline{\text{PSDDQM5}}$/$\overline{\text{PBS5}}$ | | AC5 |
| $\overline{\text{PWE6}}$/$\overline{\text{PSDDQM6}}$/$\overline{\text{PBS6}}$ | | AD4 |
| $\overline{\text{PWE7}}$/$\overline{\text{PSDDQM7}}$/$\overline{\text{PBS7}}$ | | AB5 |
| PSDA10/PGPL0 | | AE2 |
| $\overline{\text{PSDWE}}$/PGPL1 | | AD3 |
| $\overline{\text{POE}}$/$\overline{\text{PSDRAS}}$/PGPL2 | | AB4 |
| $\overline{\text{PSDCAS}}$/PGPL3 | | AC3 |
| $\overline{\text{PGTA}}$/PUPMWAIT/PGPL4 | | AD2 |
| PSDAMUX/PGPL5 | | AC2 |
| $\overline{\text{PCI\_MODE}}$[1] | | AD22 |
| PCI_CFG0 ($\overline{\text{PCI\_HOST\_EN}}$) | | AC21 |
| PCI_CFG1 ($\overline{\text{PCI\_ARB\_EN}}$) | | AE22 |
| PCI_CFG2 (DLL_ENABLE) | | AE23 |
| PCI_ PAR | | AF12 |
| $\overline{\text{PCI\_FRAME}}$ | | AD15 |
| $\overline{\text{PCI\_TRDY}}$ | | AF16 |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| PCI_AD16 | | AE16 |
| PCI_AD17 | | AF17 |
| PCI_AD18 | | AD16 |
| PCI_AD19 | | AC16 |
| PCI_AD20 | | AF18 |
| PCI_AD21 | | AB16 |
| PCI_AD22 | | AD17 |
| PCI_AD23 | | AF19 |
| PCI_AD24 | | AB17 |
| PCI_AD25 | | AF20 |
| PCI_AD26 | | AE19 |
| PCI_AD27 | | AC18 |
| PCI_AD28 | | AB18 |
| PCI_AD29 | | AD19 |
| PCI_AD30 | | AD21 |
| PCI_AD31 | | AC20 |
| $\overline{\text{PCI\_C0}}/\overline{\text{BE0}}$ | | AE12 |
| $\overline{\text{PCI\_C1}}/\overline{\text{BE1}}$ | | AF13 |
| $\overline{\text{PCI\_C2}}/\overline{\text{BE2}}$ | | AC15 |
| $\overline{\text{PCI\_C3}}/\overline{\text{BE3}}$ | | AE18 |
| $\overline{\text{IRQ0}}/\overline{\text{NMI\_OUT}}$ | | A17 |
| $\overline{\text{TRST}}$[2] | | E21 |
| TCK | | B22 |
| TMS | | C23 |
| TDI | | B24 |
| TDO | | A22 |
| $\overline{\text{TRIS}}$ | | B23 |
| $\overline{\text{PORESET}}$[2]/$\overline{\text{PCI\_RST}}$ | | C24 |
| $\overline{\text{HRESET}}$ | | D22 |
| $\overline{\text{SRESET}}$ | | F22 |
| $\overline{\text{RSTCONF}}$ | | A24 |

# 9 Package Description

This figure shows the side profile of the PBGA package to indicate the direction of the top surface view.

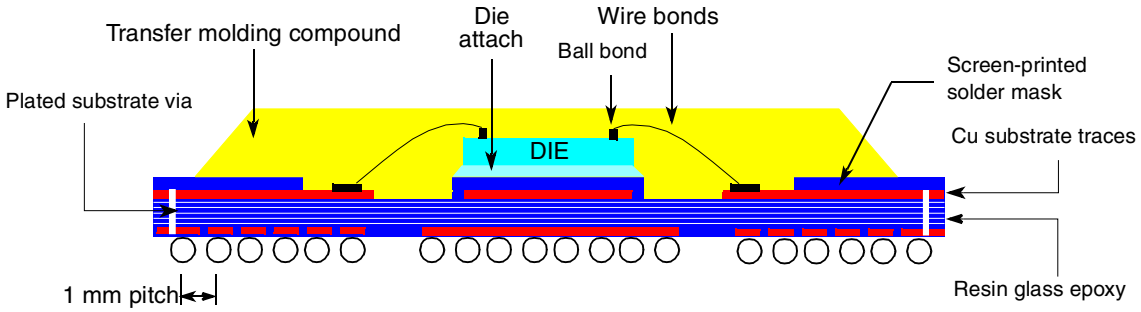



**Figure 13. Side View of the PBGA Package Remove**

## 9.1 Package Parameters

This table provides package parameters.

**Table 22. Package Parameters**

| Code | Type | Outline (mm) | Interconnects | Pitch (mm) | Nominal Unmounted Height (mm) |
|---|---|---|---|---|---|
| VR, ZQ | PBGA | 27 x 27 | 516 | 1 | 2.25 |

**NOTE: Temperature Reflow for the VR Package**

In the VR package, sphere composition is lead-free (see Table 2). This requires higher temperature reflow than what is required for other PowerQUICC II packages. Consult “Freescale PowerQUICC II Pb-Free Packaging Information” (MPC8250PBFREEPKG) available on www.freescale.com.

## 9.2 Mechanical Dimensions

This figure provides the mechanical dimensions and bottom surface nomenclature of the 516 PBGA package.

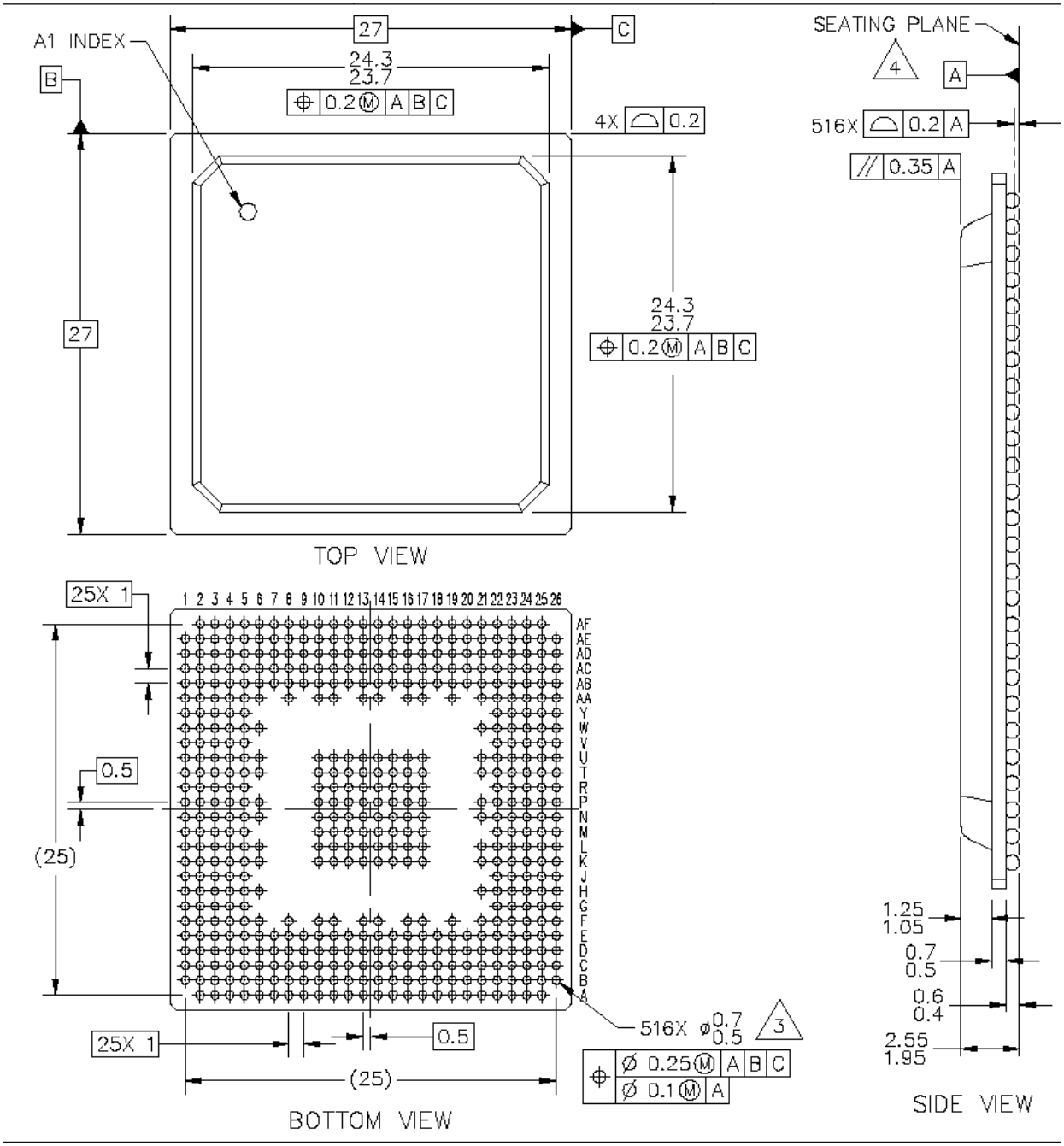



**Figure 14. Mechanical Dimensions and Bottom Surface Nomenclature—516 PBGA**

**Table 23. Document Revision History (continued)**

| Revision | Date | Substantive Changes |
|---|---|---|
| 1.2 | 09/2005 | • Added 133-MHz to the list of frequencies in the opening sentence of Section 6, "AC Electrical Characteristics".<br>• Added 133 MHz columns to Table 9, Table 11, Table 12, and Table 13.<br>• Added footnote 2 to Table 13.<br>• Added the conditions note directly above Table 12. |
| 1.1 | 01/2005 | • Modification for correct display of assertion level ("overbar") for some signals |
| 1.0 | 12/2004 | • Section 1.1: Added 8:1 ratio to Internal CPM/bus clock multiplier values<br>• Section 2: removed voltage tracking note<br>• Table 3: Note 2 updated regarding VDD/VCCSYN relationship to VDDH during power-on reset<br>• Table 4: Updated VDD and VCCSYN to 1.425 V - 1.575 V<br>• Table 8: Note 2 updated to reflect VIH=2.5 for TCK, TRST, PORESET; request for external pull-up removed.<br>• Section 4.6: Updated description of layout practices<br>• Table 8: Note 3 added regarding IIC compatibility<br>• Table 8: Updated nominal and maximum power dissipation values<br>• Table 9: updated PCI impedance to 27Ω, updated 60x and MEMC values and added note to reflect configurable impedance<br>• Section 6: Added sentence providing derating factor<br>• Section 6.1: added Note: Rise/Fall Time on CPM Input Pins<br>• Table 9: updated values for following specs: sp36b, sp37a, sp38a, sp39a, sp38b, sp40, sp41, sp42, sp43, sp42a<br>• Table 11: updated values for following specs: sp16a, sp16b, sp18a, sp18b, sp20, sp21, sp22<br>• Section 6.2: added spread spectrum clocking note<br>• Section 6.2: added CLKIN jitter note<br>• Table 12: combined specs sp11 and sp11a<br>• Table 13: sp30 Data Bus minimum delay values changed to 0.8<br>• Section 7: unit of ns added to Tval notes<br>• Section 7: Updated all notes to reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz.<br>• Section 7, "Clock Configuration Modes": Updated all table footnotes reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz.<br>• Table 21: correct superscript of footnote number after pin AD22<br>• Table 21: remove DONE3 from PC12<br>• Table 21: signals referring to TDMs C2 and D2 removed |