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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC G2_LE |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 300MHz |
| Co-Processors/DSP | Communications; RISC CPM, Security; SEC |
| RAM Controllers | DRAM, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100Mbps (2) |
| SATA | - |
| USB | USB 2.0 (1) |
| Voltage - I/O | 3.3V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 516-BBGA |
| Supplier Device Package | 516-PBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8272czqpiea |

# 1 Overview

This table shows the functionality supported by each SoC in the MPC8272 family.

**Table 1. MPC8272 PowerQUICC II Family Functionality**

| Functionality | SoCs | | | |
|---|---|---|---|---|
| | MPC8272 | MPC8248 | MPC8271 | MPC8247 |
| Package[1] | 516 PBGA | | | |
| Serial communications controllers (SCCs) | 3 | 3 | 3 | 3 |
| QUICC multi-channel controller (QMC) | Yes | Yes | Yes | Yes |
| Fast communication controllers (FCCs) | 2 | 2 | 2 | 2 |
| I-Cache (Kbyte) | 16 | 16 | 16 | 16 |
| D-Cache (Kbyte) | 16 | 16 | 16 | 16 |
| Ethernet (10/100) | 2 | 2 | 2 | 2 |
| UTOPIA II Ports | 1 | 0 | 1 | 0 |
| Multi-channel controllers (MCCs) | 0 | 0 | 0 | 0 |
| PCI bridge | Yes | Yes | Yes | Yes |
| Transmission convergence (TC) layer | — | — | — | — |
| Inverse multiplexing for ATM (IMA) | — | — | — | — |
| Universal serial bus (USB) 2.0 full/low rate | 1 | 1 | 1 | 1 |
| Security engine (SEC) | Yes | Yes | — | — |

[1] See Table 2.

Devices in the MPC8272 family are available in two packages—the VR or ZQ package—as shown in . For package ordering information, see Section 10, “Ordering Information.”

**Table 2. MPC8272 PowerQUICC II Device Packages**

| Code (Package) | VR (516 PBGA—Lead free) | ZQ (516 PBGA—Lead spheres) |
|---|---|---|
| Device | MPC8272VR | MPC8272ZQ |
| | MPC8248VR | MPC8248ZQ |
| | MPC8271VR | MPC8271ZQ |
| | MPC8247VR | MPC8247ZQ |

  - One of the FCCs supports ATM (MPC8272 and MPC8271 only)—full-duplex SAR at 155 Mbps, 8-bit UTOPIA interface 31 Mphys, AAL5, AAL1, AAL2, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 64-K external connections

— Three serial communications controllers (SCCs) identical to those on the MPC860 supporting the digital portions of the following protocols:
  - Ethernet/IEEE 802.3 CDMA/CS
  - HDLC/SDLC and HDLC bus
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Binary synchronous (BiSync) communications
  - Transparent
  - QUICC multichannel controller (QMC) up to 64 channels
    - Independent transmit and receive routing, frame synchronization.
    - Serial-multiplexed (full-duplex) input/output 2048, 1544, and 1536 Kbps PCM highways
    - Compatible with T1/DS1 24-channel and CEPT E1 32-channel PCM highway, ISDN basic rate, ISDN primary rate, and user defined.
    - Subchanneling on each time slot.
    - Independent transmit and receive routing, frame synchronization and clocking
    - Concatenation of any not necessarily consecutive time slots to channels independently for receiver/transmitter
    - Supports H1,H11, and H12 channels
    - Allows dynamic allocation of channels
  - SCC3 in NMSI mode is not usable when USB is enabled.
— Two serial management controllers (SMCs), identical to those of the MPC860
  - Provides management for BRI devices as general-circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
  - Transparent
  - UART (low-speed operation)
— One serial peripheral interface identical to the MPC860 SPI
— One $I^2C$ controller (identical to the MPC860 $I^2C$ controller)
  - Microwire compatible
  - Multiple-master, single-master, and slave modes
— Up to two TDM interfaces
  - Supports one groups of two TDM channels
  - 1024 bytes of SI RAM
— Eight independent baud rate generators and 14 input clock pins for supplying clocks to FCC, SCC, SMC, and USB serial channels
— Four independent 16-bit timers that can be interconnected as two 32-bit timers

**Table 5. DC Electrical Characteristics[1] (continued)**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| $I_{OL}$ = 5.3mA<br>CS[0–5]<br>CS6/BCTL1/SMI<br>CS7/TLBSYNC<br>BADDR27/ IRQ1<br>BADDR28/ IRQ2<br>ALE/ IRQ4<br>BCTL0<br>PWE[0–7]/PSDDQM[0–7]/PBS[0–7]<br>PSDA10/PGPL0<br>PSDWE/PGPL1<br>POE/PSDRAS/PGPL2<br>PSDCAS/PGPL3<br>PGTA/PUPMWAIT/PGPL4<br>PSDAMUX/PGPL5<br>PCI_CFG0 (PCI_HOST_EN)<br>PCI_CFG1 (PCI_ARB_EN)<br>PCI_CFG2 (DLL_ENABLE)<br>MODCK1/RSRV/TC(0)/BNKSEL(0)<br>MODCK2/CSE0/TC(1)/BNKSEL(1)<br>MODCK3CSE1/TC(2)/BNKSEL(2) | $V_{OL}$ | — | 0.4 | V |
| $I_{OL}$ = 3.2mA<br>PCI_PAR<br>PCI_FRAME<br>PCI_TRDY<br>PCI_IRDY<br>PCI_STOP<br>PCI_DEVSEL<br>PCI_IDSEL<br>PCI_PERR<br>PCI_SERR<br>PCI_REQ0<br>PCI_REQ1/ CPI_HS_ES<br>PCI_GNT0<br>PCI_GNT1/ CPI_HS_LES<br>PCI_GNT2/ CPI_HS_ENUM<br>PCI_RST<br>PCI_INTA<br>PCI_REQ2<br>DLLOUT<br>PCI_AD(0-31)<br>PCI_C(0–3)/BE(0-3)<br>PA[8–31]<br>PB[18–31]<br>PC[0–1,4–29]<br>PD[7–25, 29–31]<br>TDO | | | | |

1 The default configuration of the CPM pins (PA[8–31], PB[18–31], PC[0–1,4–29], PD[7–25, 29–31]) is input. To prevent excessive DC current, it is recommended either to pull unused pins to GND or VDDH, or to configure them as outputs.

2 TCK, TRST and PORESET have min VIH = 2.5V.

3 $V_{IL}$ for IIC interface does not match IIC standard, but does meet IIC standard for $V_{OL}$ and should not cause any compatibility issue.

4 The leakage current is measured for nominal VDDH,VCCSYN, and VDD.

[4] MPC8280, MPC8275VR, MPC8275ZQ only.

# 4 Thermal Characteristics

This table describes thermal characteristics. See Table 2 for information on a given SoC's package. Discussions of each characteristic are provided in Section 4.1, "Estimation with Junction-to-Ambient Thermal Resistance," through Section 4.7, "References." For the these discussions, $P_D = (V_{DD} \times I_{DD}) +$ PI/O, where PI/O is the power dissipation of the I/O drivers.

**Table 7. Thermal Characteristics**

| Characteristic | Symbol | Value | Unit | Air Flow |
|---|---|---|---|---|
| Junction-to-ambient—single-layer board[1] | $R_{\theta JA}$ | 27 | °C/W | Natural convection |
| | | 21 | | 1 m/s |
| Junction-to-ambient—four-layer board | $R_{\theta JA}$ | 19 | °C/W | Natural convection |
| | | 16 | | 1 m/s |
| Junction-to-board[2] | $R_{\theta JB}$ | 11 | °C/W | — |
| Junction-to-case[3] | $R_{\theta JC}$ | 8 | °C/W | — |
| Junction-to-package top[4] | $R_{\theta JT}$ | 2 | °C/W | — |

1 Assumes no thermal vias
2 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
3 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
4 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

## 4.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, $T_J$, in  C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

$T_A$ = ambient temperature (ºC)
$R_{\theta JA}$ = package junction-to-ambient thermal resistance (ºC/W)
$P_D$ = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

## 4.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

## 4.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages, especially PBGA packages, is strongly dependent on the board temperature.

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)

$T_B$ = board temperature (ºC)

$P_D$ = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

This table lists CPM input characteristics.

**NOTE: Rise/Fall Time on CPM Input Pins**

It is recommended that the rise/fall time on CPM input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

**Table 11. AC Characteristics for CPM Inputs[1]**

| Spec Number | | Characteristic | Value (ns) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Setup | | | | Hold | | | |
| Setup | Hold | | 66 MHz | 83 MHz | 100 MHz | 133 MHz | 66 MHz | 83 MHz | 100 MHz | 133 MHz |
| sp16a | sp17a | FCC inputs—internal clock (NMSI) | 6 | 6 | 6 | 6 | 0 | 0 | 0 | 0 |
| sp16b | sp17b | FCC inputs—external clock (NMSI) | 2.5 | 2.5 | 2.5 | 2.5 | 2 | 2 | 2 | 2 |
| sp18a | sp19a | SCC/SMC/SPI/I2C inputs—internal clock (NMSI) | 6 | 6 | 6 | 6 | 0 | 0 | 0 | 0 |
| sp18b | sp19b | SCC/SMC/SPI/I2C inputs—external clock (NMSI) | 4 | 4 | 4 | 4 | 2 | 2 | 2 | 2 |
| sp20 | sp21 | TDM inputs/SI | 3 | 3 | 3 | 3 | 2.5 | 2.5 | 2.5 | 2.5 |
| sp22 | sp23 | PIO/TIMER/IDMA inputs | 8 | 8 | 8 | 8 | 0.5 | 0.5 | 0.5 | 0.5 |

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

**NOTE**

Although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the FCC internal clock.

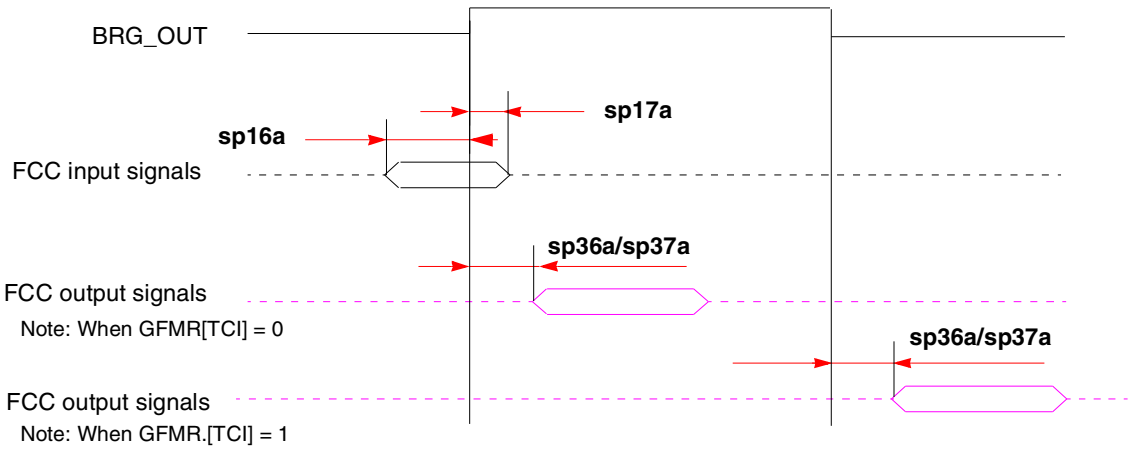
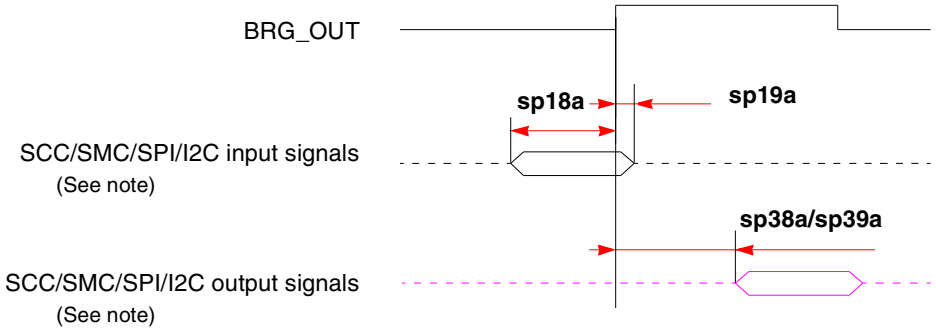



**Figure 3. FCC Internal Clock Diagram**

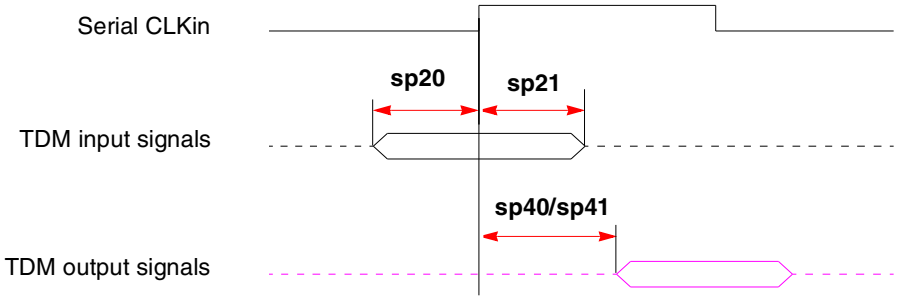
This figure shows the SCC/SMC/SPI/I$^2$C internal clock.




**Note:** There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

**Figure 6. SCC/SMC/SPI/I$^2$C Internal Clock Diagram**

This figure shows TDM input and output signals.




**Note:** There are four possible TDM timing conditions:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

**Figure 7. TDM Signal Diagram**

This figure shows signal behavior in MEMC mode.

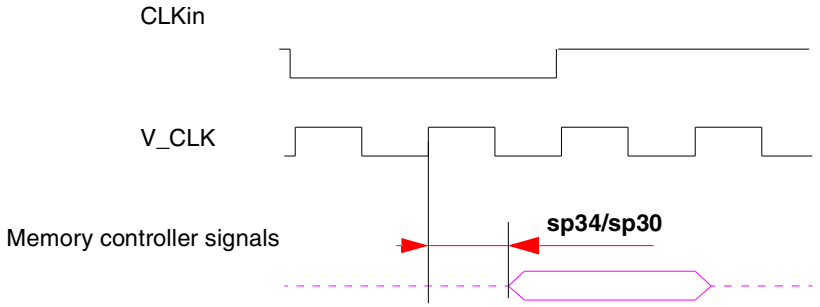



**Figure 10. MEMC Mode Diagram**

**NOTE**

Generally, all SoC bus and system output signals are driven from the rising edge of the input clock (CLKin). Memory controller signals, however, trigger on four points within a CLKin cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKin. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 14.

**Table 14. Tick Spacing for Memory Controller Signals**

| PLL Clock Ratio | Tick Spacing (T1 Occurs at the Rising Edge of CLKin) | | |
|---|---|---|---|
| | T2 | T3 | T4 |
| 1:2, 1:3, 1:4, 1:5, 1:6 | 1/4 CLKin | 1/2 CLKin | 3/4 CLKin |
| 1:2.5 | 3/10 CLKin | 1/2 CLKin | 8/10 CLKin |
| 1:3.5 | 4/14 CLKin | 1/2 CLKin | 11/14 CLKin |

This table is a representation of the information in Table 14.

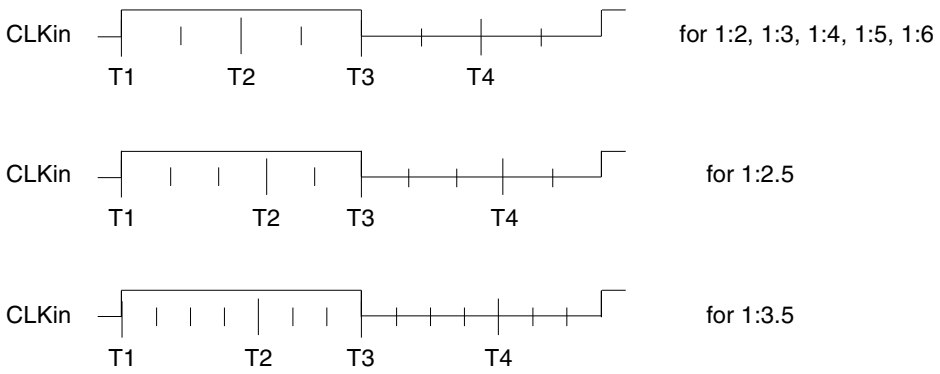



**Figure 11. Internal Tick Spacing for Memory Controller Signals**

**Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1000_010 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 3.5 | 233.3 | 466.7 | 8 | 25.0 | 50.0 |
| 1000_011 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 4 | 266.7 | 533.3 | 8 | 25.0 | 50.0 |
| 1000_100 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 4.5 | 300.0 | 600.0 | 8 | 25.0 | 50.0 |
| 1000_101 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 6 | 400.0 | 800.0 | 8 | 25.0 | 50.0 |
| 1000_110 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 6.5 | 433.3 | 866.7 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1001_000 | Reserved | | | | | | | | | | |
| 1001_001 | Reserved | | | | | | | | | | |
| 1001_010 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 3.5 | 200.0 | 400.0 | 8 | 25.0 | 50.0 |
| 1001_011 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 4 | 228.6 | 457.1 | 8 | 25.0 | 50.0 |
| 1001_100 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 4.5 | 257.1 | 514.3 | 8 | 25.0 | 50.0 |
| 1001_101 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 5 | 214.3 | 428.6 | 6 | 25.0 | 50.0 |
| 1001_110 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 5.5 | 235.7 | 471.4 | 6 | 25.0 | 50.0 |
| 1001_111 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 6 | 257.1 | 514.3 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1010_000 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 2 | 150.0 | 300.0 | 6 | 25.0 | 50.0 |
| 1010_001 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 2.5 | 187.5 | 375.0 | 6 | 25.0 | 50.0 |
| 1010_010 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 3 | 225.0 | 450.0 | 6 | 25.0 | 50.0 |
| 1010_011 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 3.5 | 262.5 | 525.0 | 6 | 25.0 | 50.0 |
| 1010_100 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 4 | 300.0 | 600.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1010_101 | 100.0 | 200.0 | 2 | 200.0 | 400.0 | 2.5 | 250.0 | 500.0 | 8 | 25.0 | 50.0 |
| 1010_110 | 100.0 | 200.0 | 2 | 200.0 | 400.0 | 3 | 300.0 | 600.0 | 8 | 25.0 | 50.0 |
| 1010_111 | 100.0 | 200.0 | 2 | 200.0 | 400.0 | 3.5 | 350.0 | 700.0 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1011_000 | Reserved | | | | | | | | | | |
| 1011_001 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 2.5 | 200.0 | 400.0 | 8 | 25.0 | 50.0 |
| 1011_010 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 3 | 240.0 | 480.0 | 8 | 25.0 | 50.0 |
| 1011_011 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 3.5 | 280.0 | 560.0 | 8 | 25.0 | 50.0 |
| 1011_100 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 4 | 320.0 | 640.0 | 8 | 25.0 | 50.0 |

**Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1011_101 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 4.5 | 360.0 | 720.0 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1101_000 | 50.0 | 100.0 | 2.5 | 125.0 | 250.0 | 3 | 150.0 | 300.0 | 5 | 25.0 | 50.0 |
| 1101_001 | 50.0 | 100.0 | 2.5 | 125.0 | 250.0 | 3.5 | 175.0 | 350.0 | 5 | 25.0 | 50.0 |
| 1101_010 | 50.0 | 100.0 | 2.5 | 125.0 | 250.0 | 4 | 200.0 | 400.0 | 5 | 25.0 | 50.0 |
| 1101_011 | 50.0 | 100.0 | 2.5 | 125.0 | 250.0 | 4.5 | 225.0 | 450.0 | 5 | 25.0 | 50.0 |
| 1101_100 | 50.0 | 100.0 | 2.5 | 125.0 | 250.0 | 5 | 250.0 | 500.0 | 5 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1101_101 | 62.5 | 125.0 | 2 | 125.0 | 250.0 | 3 | 187.5 | 375.0 | 5 | 25.0 | 50.0 |
| 1101_110 | 62.5 | 125.0 | 2 | 125.0 | 250.0 | 4 | 250.0 | 500.0 | 5 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1110_000 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 3.5 | 175.0 | 350.0 | 6 | 25.0 | 50.0 |
| 1110_001 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 6 | 25.0 | 50.0 |
| 1110_010 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 4.5 | 225.0 | 450.0 | 6 | 25.0 | 50.0 |
| 1110_011 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 5 | 250.0 | 500.0 | 6 | 25.0 | 50.0 |
| 1110_100 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 5.5 | 275.0 | 550.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1100_000 | Reserved | | | | | | | | | | |
| 1100_001 | Reserved | | | | | | | | | | |
| 1100_010 | Reserved | | | | | | | | | | |

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

2 PCI_MODCK determines the PCI clock frequency range. See Table 17 for higher range configurations.

3 MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

4 CPM multiplication factor = CPM clock/bus clock

5 CPU multiplication factor = Core PLL multiplication factor

6 CPM_CLK/PCI_CLK ratio. When PCI_MODCK = 1, the ratio of CPM_CLK/PCI_CLK should be calculated from PCIDF as follows:
PCIDF = 3 > CPM_CLK/PCI_CLK = 4
PCIDF = 5 > CPM_CLK/PCI_CLK = 6
PCIDF = 7 > CPM_CLK/PCI_CLK = 8
PCIDF = 9 > CPM_CLK/PCI_CLK = 5
PCIDF = B > CPM_CLK/PCI_CLK = 6

## 7.2 PCI Agent Mode

These tables show configurations for PCI agent mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device. Note that in PCI agent mode the input clock is PCI clock.

**Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2]**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| **Default Modes (MODCK_H=0000)** | | | | | | | | | | | |
| 0000_000 | 60.0 | 66.7 | 2 | 120.0 | 133.3 | 2.5 | 150.0 | 166.7 | 2 | 60.0 | 66.7 |
| 0000_001 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 3 | 150.0 | 200.0 | 2 | 50.0 | 66.7 |
| 0000_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0000_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 200.0 | 266.6 | 3 | 50.0 | 66.7 |
| 0000_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 2.5 | 60.0 | 80.0 |
| 0000_101 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 2.5 | 60.0 | 80.0 |
| 0000_110 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 233.3 | 311.1 | 3 | 66.7 | 88.9 |
| 0000_111 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 240.0 | 320.0 | 2.5 | 80.0 | 106.7 |
| **Full Configuration Modes** | | | | | | | | | | | |
| 0001_001 | 60.0 | 66.7 | 2 | 120.0 | 133.3 | 5 | 150.0 | 166.7 | 4 | 30.0 | 33.3 |
| 0001_010 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 6 | 150.0 | 200.0 | 4 | 25.0 | 33.3 |
| 0001_011 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 7 | 175.0 | 233.3 | 4 | 25.0 | 33.3 |
| 0001_100 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 8 | 200.0 | 266.6 | 4 | 25.0 | 33.3 |
| | | | | | | | | | | | |
| 0010_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 2.5 | 60.0 | 80.0 |
| 0010_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 2.5 | 60.0 | 80.0 |
| 0010_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 240.0 | 320.0 | 2.5 | 60.0 | 80.0 |
| 0010_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4.5 | 270.0 | 360.0 | 2.5 | 60.0 | 80.0 |
| | | | | | | | | | | | |

**Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 0011_000 | Reserved | | | | | | | | | | |
| 0011_001 | Reserved | | | | | | | | | | |
| 0011_010 | Reserved | | | | | | | | | | |
| 0011_011 | Reserved | | | | | | | | | | |
| 0011_100 | Reserved | | | | | | | | | | |
| | | | | | | | | | | | |
| 0100_000 | Reserved | | | | | | | | | | |
| 0100_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0100_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 175.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0100_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 200.0 | 266.6 | 3 | 50.0 | 66.7 |
| 0100_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4.5 | 225.0 | 300.0 | 3 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0101_000 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 2.5 | 250.0 | 333.3 | 2.5 | 100.0 | 133.3 |
| 0101_001 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 3 | 300.0 | 400.0 | 2.5 | 100.0 | 133.3 |
| 0101_010 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 3.5 | 350.0 | 466.6 | 2.5 | 100.0 | 133.3 |
| 0101_011 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 4 | 400.0 | 533.3 | 2.5 | 100.0 | 133.3 |
| 0101_100 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 4.5 | 450.0 | 599.9 | 2.5 | 100.0 | 133.3 |
| 0101_101 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 5 | 500.0 | 666.6 | 2.5 | 100.0 | 133.3 |
| 0101_110 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 5.5 | 550.0 | 733.3 | 2.5 | 100.0 | 133.3 |
| | | | | | | | | | | | |
| 0110_000 | Reserved | | | | | | | | | | |
| 0110_001 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 200.0 | 266.6 | 3 | 66.7 | 88.9 |
| 0110_010 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 233.3 | 311.1 | 3 | 66.7 | 88.9 |
| 0110_011 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4 | 266.7 | 355.5 | 3 | 66.7 | 88.9 |
| 0110_100 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4.5 | 300.0 | 400.0 | 3 | 66.7 | 88.9 |
| | | | | | | | | | | | |
| 0111_000 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 2 | 150.0 | 200.0 | 2 | 75.0 | 100.0 |
| 0111_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 2.5 | 187.5 | 250.0 | 2 | 75.0 | 100.0 |
| 0111_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 225.0 | 300.0 | 2 | 75.0 | 100.0 |
| 0111_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 262.5 | 350.0 | 2 | 75.0 | 100.0 |

**Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| | | | | | | | | | | | |
| 1000_000 | Reserved | | | | | | | | | | |
| 1000_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 2.5 | 150.0 | 166.7 | 2.5 | 60.0 | 80.0 |
| 1000_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 2.5 | 60.0 | 80.0 |
| 1000_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 2.5 | 60.0 | 80.0 |
| 1000_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 240.0 | 320.0 | 2.5 | 60.0 | 80.0 |
| 1000_101 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4.5 | 270.0 | 360.0 | 2.5 | 60.0 | 80.0 |
| | | | | | | | | | | | |
| 1001_000 | Reserved | | | | | | | | | | |
| 1001_001 | Reserved | | | | | | | | | | |
| 1001_010 | Reserved | | | | | | | | | | |
| 1001_011 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4 | 200.0 | 266.6 | 4 | 50.0 | 66.7 |
| 1001_100 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4.5 | 225.0 | 300.0 | 4 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1010_000 | Reserved | | | | | | | | | | |
| 1010_001 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 200.0 | 266.6 | 3 | 66.7 | 88.9 |
| 1010_010 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 233.3 | 311.1 | 3 | 66.7 | 88.9 |
| 1010_011 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4 | 266.7 | 355.5 | 3 | 66.7 | 88.9 |
| 1010_100 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4.5 | 300.0 | 400.0 | 3 | 66.7 | 88.9 |
| | | | | | | | | | | | |
| 1011_000 | Reserved | | | | | | | | | | |
| 1011_001 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 2.5 | 200.0 | 266.6 | 2.5 | 80.0 | 106.7 |
| 1011_010 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 240.0 | 320.0 | 2.5 | 80.0 | 106.7 |
| 1011_011 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 280.0 | 373.3 | 2.5 | 80.0 | 106.7 |
| 1011_100 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4 | 320.0 | 426.6 | 2.5 | 80.0 | 106.7 |
| | | | | | | | | | | | |
| 1011_101 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 2.5 | 250.0 | 333.3 | 2 | 100.0 | 133.3 |
| 1011_110 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 300.0 | 400.0 | 2 | 100.0 | 133.3 |
| 1011_111 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 350.0 | 466.6 | 2 | 100.0 | 133.3 |
| | | | | | | | | | | | |

**Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1100_101 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 4 | 400.0 | 533.3 | 3 | 100.0 | 133.3 |
| 1100_110 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 4.5 | 450.0 | 599.9 | 3 | 100.0 | 133.3 |
| 1100_111 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 5 | 500.0 | 666.6 | 3 | 100.0 | 133.3 |
| 1101_000 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 5.5 | 550.0 | 733.3 | 3 | 100.0 | 133.3 |
| | | | | | | | | | | | |
| 1101_001 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 3.5 | 420.0 | 559.9 | 2.5 | 120.0 | 160.0 |
| 1101_010 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 4 | 480.0 | 639.9 | 2.5 | 120.0 | 160.0 |
| 1101_011 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 4.5 | 540.0 | 719.9 | 2.5 | 120.0 | 160.0 |
| 1101_100 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 5 | 600.0 | 799.9 | 2.5 | 120.0 | 160.0 |
| | | | | | | | | | | | |
| 1110_000 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 2.5 | 312.5 | 416.6 | 2 | 125.0 | 166.7 |
| 1110_001 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 3 | 375.0 | 500.0 | 2 | 125.0 | 166.7 |
| 1110_010 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 3.5 | 437.5 | 583.3 | 2 | 125.0 | 166.7 |
| 1110_011 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 4 | 500.0 | 666.6 | 2 | 125.0 | 166.7 |
| | | | | | | | | | | | |
| 1110_100 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 4 | 333.3 | 444.4 | 3 | 83.3 | 111.1 |
| 1110_101 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 4.5 | 375.0 | 500.0 | 3 | 83.3 | 111.1 |
| 1110_110 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 5 | 416.7 | 555.5 | 3 | 83.3 | 111.1 |
| 1110_111 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 5.5 | 458.3 | 611.1 | 3 | 83.3 | 111.1 |
| | | | | | | | | | | | |
| 1100_000 | Reserved | | | | | | | | | | |
| 1100_001 | Reserved | | | | | | | | | | |
| 1100_010 | Reserved | | | | | | | | | | |

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

2 PCI_MODCK determines the PCI clock frequency range. See Table 20 for lower range configurations.

3 MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

4 CPM multiplication factor = CPM clock/bus clock

5 CPU multiplication factor = Core PLL multiplication factor

**Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2]**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| **Default Modes (MODCK_H=0000)** | | | | | | | | | | | |
| 0000_000 | 30.0 | 50.0 | 4 | 120.0 | 200.0 | 2.5 | 150.0 | 250.0 | 2 | 60.0 | 100.0 |
| 0000_001 | 25.0 | 50.0 | 4 | 100.0 | 200.0 | 3 | 150.0 | 300.0 | 2 | 50.0 | 100.0 |
| 0000_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 150.0 | 300.0 | 3 | 50.0 | 100.0 |
| 0000_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 3 | 50.0 | 100.0 |
| 0000_100 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 180.0 | 360.0 | 2.5 | 60.0 | 120.0 |
| 0000_101 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 2.5 | 60.0 | 120.0 |
| 0000_110 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3.5 | 233.3 | 466.7 | 3 | 66.7 | 133.3 |
| 0000_111 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3 | 240.0 | 480.0 | 2.5 | 80.0 | 160.0 |
| Full Configuration Modes | | | | | | | | | | | |
| 0001_001 | 30.0 | 50.0 | 4 | 120.0 | 200.0 | 5 | 150.0 | 250.0 | 4 | 30.0 | 50.0 |
| 0001_010 | 25.0 | 50.0 | 4 | 100.0 | 200.0 | 6 | 150.0 | 300.0 | 4 | 25.0 | 50.0 |
| 0001_011 | 25.0 | 50.0 | 4 | 100.0 | 200.0 | 7 | 175.0 | 350.0 | 4 | 25.0 | 50.0 |
| 0001_100 | 25.0 | 50.0 | 4 | 100.0 | 200.0 | 8 | 200.0 | 400.0 | 4 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 0010_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 180.0 | 360.0 | 2.5 | 60.0 | 120.0 |
| 0010_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 2.5 | 60.0 | 120.0 |
| 0010_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 240.0 | 480.0 | 2.5 | 60.0 | 120.0 |
| 0010_100 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4.5 | 270.0 | 540.0 | 2.5 | 60.0 | 120.0 |
| | | | | | | | | | | | |
| 0011_000 | Reserved | | | | | | | | | | |
| 0011_001 | 37.5 | 50.0 | 4 | 150.0 | 200.0 | 3 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0011_010 | 32.1 | 50.0 | 4 | 128.6 | 200.0 | 3.5 | 150.0 | 233.3 | 3 | 42.9 | 66.7 |
| 0011_011 | 28.1 | 50.0 | 4 | 112.5 | 200.0 | 4 | 150.0 | 266.7 | 3 | 37.5 | 66.7 |
| 0011_100 | 25.0 | 50.0 | 4 | 100.0 | 200.0 | 4.5 | 150.0 | 300.0 | 3 | 33.3 | 66.7 |
| | | | | | | | | | | | |
| 0100_000 | Reserved | | | | | | | | | | |
| 0100_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 150.0 | 300.0 | 3 | 50.0 | 100.0 |
| 0100_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 175.0 | 350.0 | 3 | 50.0 | 100.0 |
| 0100_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 3 | 50.0 | 100.0 |

**Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1110_000 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 2.5 | 156.3 | 312.5 | 2 | 62.5 | 125.0 |
| 1110_001 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 3 | 187.5 | 375.0 | 2 | 62.5 | 125.0 |
| 1110_010 | 28.6 | 50.0 | 5 | 142.9 | 250.0 | 3.5 | 250.0 | 437.5 | 2 | 71.4 | 125.0 |
| 1110_011 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 4 | 250.0 | 500.0 | 2 | 62.5 | 125.0 |
| | | | | | | | | | | | |
| 1110_100 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 4 | 166.7 | 333.3 | 3 | 41.7 | 83.3 |
| 1110_101 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 4.5 | 187.5 | 375.0 | 3 | 41.7 | 83.3 |
| 1110_110 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 5 | 208.3 | 416.7 | 3 | 41.7 | 83.3 |
| 1110_111 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 5.5 | 229.2 | 458.3 | 3 | 41.7 | 83.3 |
| | | | | | | | | | | | |
| 1100_000 | Reserved | | | | | | | | | | |
| 1100_001 | Reserved | | | | | | | | | | |
| 1100_010 | Reserved | | | | | | | | | | |

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

2 PCI_MODCK determines the PCI clock frequency range. See Table 19 for higher range configurations.

3 MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

4 CPM multiplication factor = CPM clock/bus clock

5 CPU multiplication factor = Core PLL multiplication factor

# 8 Pinout

This figure and table show the pin assignments and pinout for the 516 PBGA package.

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| $\overline{TS}$ | | D1 |
| A0 | | A3 |
| A1 | | B5 |
| A2 | | D8 |
| A3 | | C6 |
| A4 | | A4 |
| A5 | | A6 |
| A6 | | B6 |
| A7 | | C7 |
| A8 | | B7 |
| A9 | | A7 |
| A10 | | D9 |
| A11 | | E11 |
| A12 | | C9 |
| A13 | | B9 |
| A14 | | D11 |
| A15 | | A9 |
| A16 | | B10 |
| A17 | | A10 |
| A18 | | B11 |
| A19 | | A11 |
| A20 | | D12 |
| A21 | | A12 |
| A22 | | D13 |
| A23 | | B13 |
| A24 | | C13 |
| A25 | | C14 |
| A26 | | B14 |
| A27 | | D14 |
| A28 | | E14 |
| A29 | | A14 |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| **MPC8272/MPC8248 and MPC8271/MPC8247** | **MPC8272/MPC8271 Only** | |
| MODCK1/$\overline{\text{RSRV}}$/TC0/BNKSEL0 | | A20 |
| MODCK2/CSE0/TC1/BNKSEL1 | | C20 |
| MODCK3/CSE1/TC2/BNKSEL2 | | A21 |
| CLKIN1 | | D21 |
| PA8/SMRXD2 | | AF25[3] |
| PA9/SMTXD2 | | AA22[3] |
| PA10/MSNUM5 | FCC1_UT_RXD0 | AB23[3] |
| PA11/MSNUM4 | FCC1_UT_RXD1 | AD26[3] |
| PA12/MSNUM3 | FCC1_UT_RXD2 | AD25[3] |
| PA13/MSNUM2 | FCC1_UT_RXD3 | AA24[3] |
| PA14/FCC1_MII_HDLC_RXD3 | FCC1_UT_RXD4 | W22[3] |
| PA15/FCC1_MII_HDLC_RXD2 | FCC1_UT_RXD5 | Y24[3] |
| PA16/FCC1_MII_HDLC_RXD1 | FCC1_UT_RXD6 | T22[3] |
| PA17/FCC1_MII_HDLC_RXD0/ FCC1_MII_TRAN_RXD/FCC1_RMII_RXD0 | FCC1_UT_RXD7 | W26[3] |
| PA18/FCC1_MII_HDLC_TXD0/FCC1_MII_TRAN_TXD/ FCC1_RMII_TXD0 | FCC1_UT_TXD7 | V26[3] |
| PA19/FCC1_MII_HDLC_TXD1/FCC1_RMII_TXD1 | FCC1_UT_TXD6 | R23[3] |
| PA20/FCC1_MII_HDLC_TXD2 | FCC1_UT_TXD5 | P25[3] |
| PA21/FCC1_MII_HDLC_TXD3 | FCC1_UT_TXD4 | N22[3] |
| PA22 | FCC1_UT_TXD3 | N26[3] |
| PA23 | FCC1_UT_TXD2 | N23[3] |
| PA24/MSNUM1 | FCC1_UT_TXD1 | H26[3] |
| PA25/MSNUM0 | FCC1_UT_TXD0 | G25[3] |
| PA26/FCC1_MII_RMIIRX_ER | FCC1_UT_RXCLAV | L22[3] |
| PA27/FCC1_MII_RX_DV/FCC1_RMII_CRS_DV | FCC1_UT_RXSOC | G24[3] |
| PA28/FCC1_MII_RMII_TX_EN | FCC1_UT_RXENB | G23[3] |
| PA29/FCC1_MII_TX_ER | $\overline{\text{FCC1\_UT\_TXSOC}}$ | B26[3] |
| PA30/FCC1_MII_CRS/$\overline{\text{FCC1\_RTS}}$ | FCC1_UT_TXCLAV | A25[3] |

## 9.2 Mechanical Dimensions

This figure provides the mechanical dimensions and bottom surface nomenclature of the 516 PBGA package.

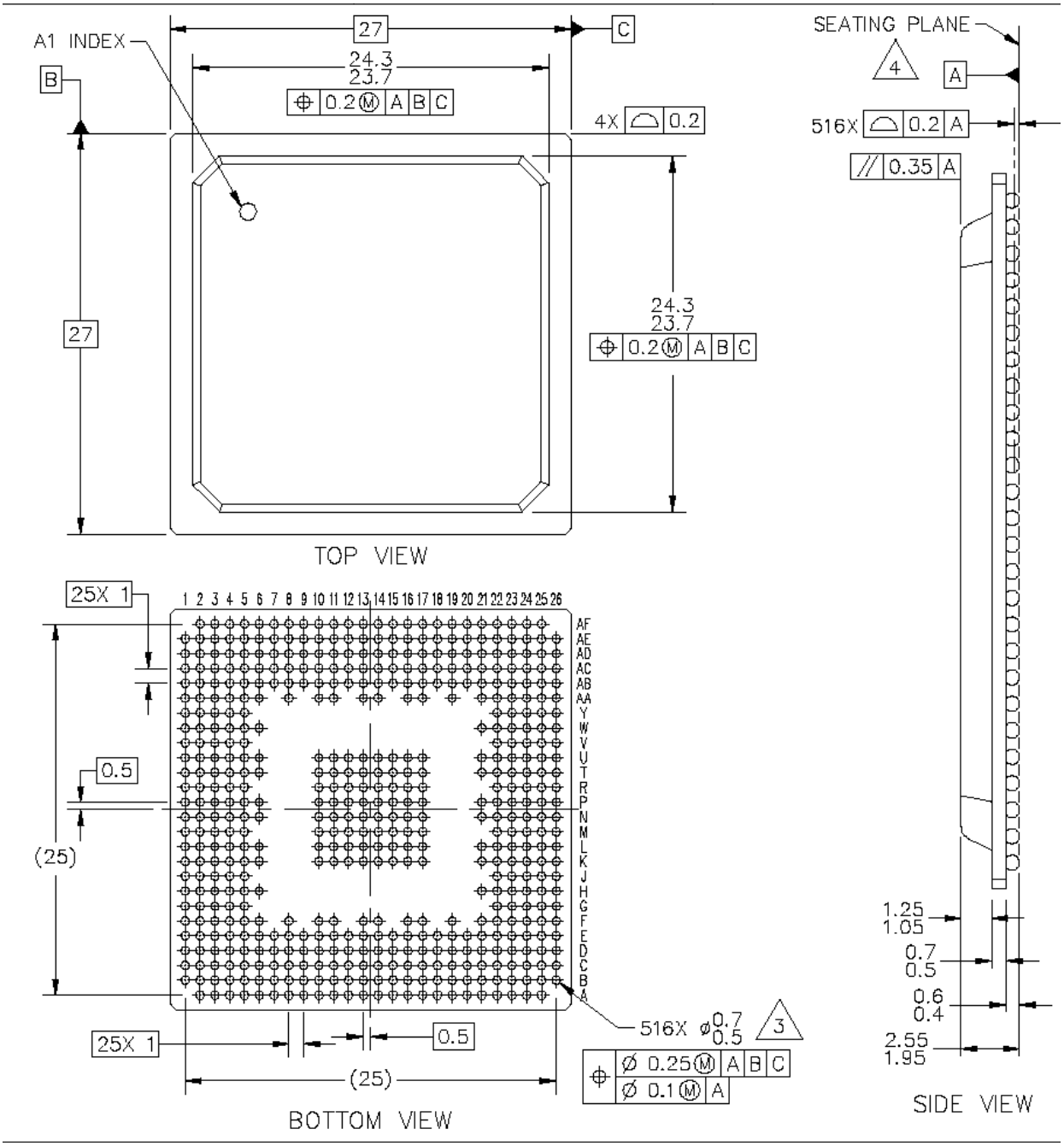



**Figure 14. Mechanical Dimensions and Bottom Surface Nomenclature—516 PBGA**

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1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

**Europe, Middle East, and Africa:**
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

**Japan:**
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

**Asia/Pacific:**
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

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Literature Distribution Center
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Document Number: MPC8272EC
Rev. 3
09/2011