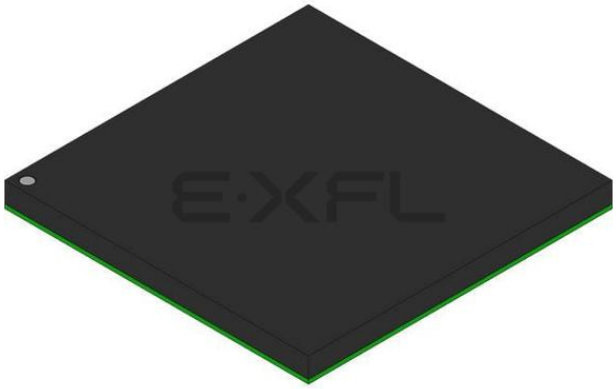

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PowerPC G2_LE |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 300MHz |
| Co-Processors/DSP | Communications; RISC CPM, Security; SEC |
| RAM Controllers | DRAM, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100Mbps (2) |
| SATA | - |
| USB | USB 2.0 (1) |
| Voltage - I/O | 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 516-BBGA |
| Supplier Device Package | 516-PBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8272vrpiea |

# 1 Overview

This table shows the functionality supported by each SoC in the MPC8272 family.

**Table 1. MPC8272 PowerQUICC II Family Functionality**

| Functionality | SoCs | | | |
|---|---|---|---|---|
| | MPC8272 | MPC8248 | MPC8271 | MPC8247 |
| Package[1] | 516 PBGA | | | |
| Serial communications controllers (SCCs) | 3 | 3 | 3 | 3 |
| QUICC multi-channel controller (QMC) | Yes | Yes | Yes | Yes |
| Fast communication controllers (FCCs) | 2 | 2 | 2 | 2 |
| I-Cache (Kbyte) | 16 | 16 | 16 | 16 |
| D-Cache (Kbyte) | 16 | 16 | 16 | 16 |
| Ethernet (10/100) | 2 | 2 | 2 | 2 |
| UTOPIA II Ports | 1 | 0 | 1 | 0 |
| Multi-channel controllers (MCCs) | 0 | 0 | 0 | 0 |
| PCI bridge | Yes | Yes | Yes | Yes |
| Transmission convergence (TC) layer | — | — | — | — |
| Inverse multiplexing for ATM (IMA) | — | — | — | — |
| Universal serial bus (USB) 2.0 full/low rate | 1 | 1 | 1 | 1 |
| Security engine (SEC) | Yes | Yes | — | — |

[1] See Table 2.

Devices in the MPC8272 family are available in two packages—the VR or ZQ package—as shown in . For package ordering information, see Section 10, “Ordering Information.”

**Table 2. MPC8272 PowerQUICC II Device Packages**

| Code (Package) | VR (516 PBGA—Lead free) | ZQ (516 PBGA—Lead spheres) |
|---|---|---|
| Device | MPC8272VR | MPC8272ZQ |
| | MPC8248VR | MPC8248ZQ |
| | MPC8271VR | MPC8271ZQ |
| | MPC8247VR | MPC8247ZQ |

This figure shows the block diagram of the SoC.

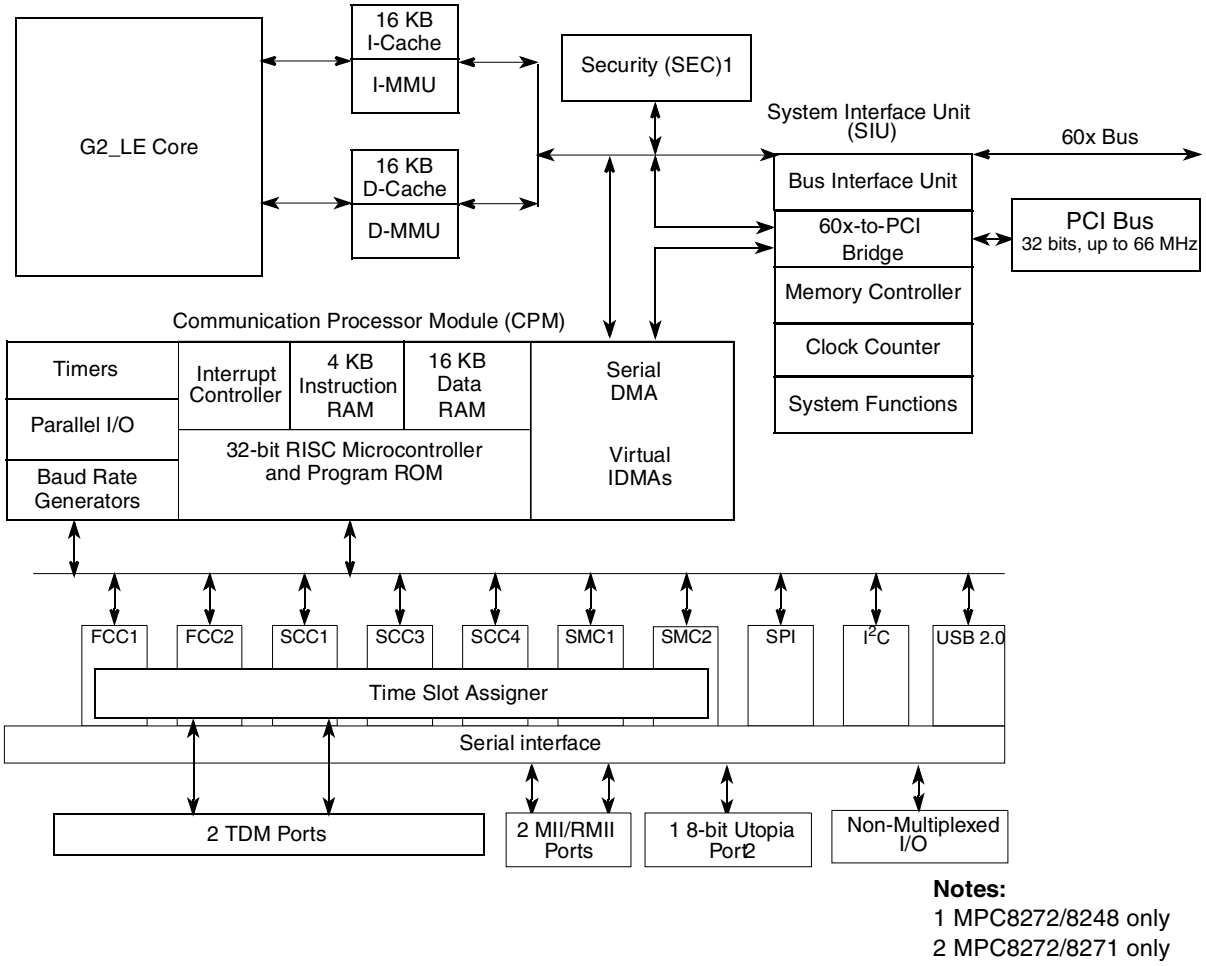



**Figure 1. SoC Block Diagram**

## 1.1 Features

The major features of the SoC are as follows:

- Dual-issue integer (G2_LE) core
  - A core version of the MPC603e microprocessor
  - System core microprocessor supporting frequencies of 266–400 MHz
  - Separate 16 KB data and instruction caches:
    - Four-way set associative
    - Physically addressed
    - LRU replacement algorithm
  - Power Architecture®-compliant memory management unit (MMU)
  - Common on-chip processor (COP) test interface
  - Supports bus snooping for cache coherency

5 MPC8272 and MPC8271 only.

**Table 6.**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input high voltage—all inputs except TCK, TRST and PORESET[1] | $V_{IH}$ | 2.0 | 3.465 | V |
| Input low voltage | $V_{IL}$ | GND | 0.8 | V |
| CLKIN input high voltage | $V_{IHC}$ | 2.4 | 3.465 | V |
| CLKIN input low voltage | $V_{ILC}$ | GND | 0.4 | V |
| Input leakage current, $V_{IN}$ = VDDH[2] | $I_{IN}$ | — | 10 | μA |
| Hi-Z (off state) leakage current, $V_{IN}$ = VDDH[2] | $I_{OZ}$ | — | 10 | μA |
| Signal low input current, $V_{IL}$ = 0.8 V[3] | $I_L$ | — | 1 | μA |
| Signal high input current, $V_{IH}$ = 2.0 V | $I_H$ | — | 1 | μA |
| Output high voltage, $I_{OH}$ = –2 mA<br>except UTOPIA mode, and open drain pins<br><br>In UTOPIA mode[4] (UTOPIA pins only): $I_{OH}$ = -8.0mA | $V_{OH}$ | 2.4 | — | V |
| In UTOPIA mode[4] (UTOPIA pins only): $I_{OL}$ = 8.0mA | $V_{OL}$ | — | 0.5 | V |
| $I_{OL}$ = 6.0mA<br>BR<br>BG<br>ABB/IRQ2<br>TS<br>A[0-31]<br>TT[0-4]<br>TBST<br>TSIZE[0–3]<br>AACK<br>ARTRY<br>DBG<br>DBB/IRQ3<br>D[0-63]<br>//EXT_BR3<br>//EXT_BG3<br>/TBEN/EXT_DBG3/CINT<br>PSDVAL<br>TA<br>TEA<br>GBL/IRQ1<br>CI/BADDR29/IRQ2<br>WT/BADDR30/IRQ3<br>BADDR31/IRQ5/CINT<br>CPU_BR<br>IRQ0/NMI_OUT<br>/PCI_RST<br>HRESET<br>SRESET<br>RSTCONF | $V_{OL}$ | — | 0.4 | V |

## 4.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

## 4.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages, especially PBGA packages, is strongly dependent on the board temperature.

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)

$T_B$ = board temperature (ºC)

$P_D$ = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

## 4.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application, or a more accurate and complex model of the package can be used in the thermal simulation.

## 4.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter ($\Psi_{JT}$) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

$\Psi_{JT}$ = thermal characterization parameter

$T_T$ = thermocouple temperature on top of package

$P_D$ = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the case to avoid measurement errors caused by cooling effects of the thermocouple wire.

## 4.6 Layout Practices

Each VDD and VDDH pin should be provided with a low-impedance path to the board's power supplies. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The VDD and VDDH power supplies should be bypassed to ground using bypass capacitors located as close as possible to the four sides of the package. For filtering high frequency noise, a capacitor of 0.1uF on each VDD and VDDH pin is recommended. Further, for medium frequency noise, a total of 2 capacitors of 47uF for VDD and 2 capacitors of 47uF for VDDH are also recommended. The capacitor leads and associated printed circuit traces connecting to chip VDD, VDDH and ground should be kept to less than half an inch per capacitor lead. Boards should employ separate inner layers for power and GND planes.

All output pins on the SoC have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the VDD and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

**NOTE**

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin's rising edge.

## 6.3 JTAG Timings

This table lists the JTAG timings.

**Table 15. JTAG Timings[1]**

| Parameter | Symbol[2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| JTAG external clock frequency of operation | $f_{JTG}$ | 0 | 33.3 | MHz | — |
| JTAG external clock cycle time | $t_{JTG}$ | 30 | — | ns | — |
| JTAG external clock pulse width measured at 1.4V | $t_{JTKHKL}$ | 15 | — | ns | — |
| JTAG external clock rise and fall times | $t_{JTGR}$ and $t_{JTGF}$ | 0 | 5 | ns | 6 |
| TRST assert time | $t_{TRST}$ | 25 | — | ns | 3, 6 |
| Input setup times<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDVKH}$<br>$t_{JTIVKH}$ | <br>4<br>4 | <br>—<br>— | <br>ns<br>ns | <br>4, 7<br>4, 7 |
| Input hold times<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDXKH}$<br>$t_{JTIXKH}$ | <br>10<br>10 | <br>—<br>— | <br>ns<br>ns | <br>4, 7<br>4, 7 |
| Output valid times<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDV}$<br>$t_{JTKLOV}$ | <br>—<br>— | <br>10<br>10 | <br>ns<br>ns | <br>5, 7<br>5, 7 |
| Output hold times<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDX}$<br>$t_{JTKLOX}$ | <br>1<br>1 | <br>—<br>— | <br>ns<br>ns | <br>5, 7<br>5, 7 |
| JTAG external clock to output high impedance<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDZ}$<br>$t_{JTKLOZ}$ | <br>1<br>1 | <br>10<br>10 | <br>ns<br>ns | <br>5, 6<br>5, 6 |

1 All outputs are measured from the midpoint voltage of the falling/rising edge of $t_{TCLK}$ to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2 The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{JTDVKH}$ symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{JTDXKH}$ symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

3 TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

4 Non-JTAG signal input timing with respect to $t_{TCLK}$.

5 Non-JTAG signal output timing with respect to $t_{TCLK}$.

6 Guaranteed by design.

7 Guaranteed by design and device characterization.

**Table 17. Clock Configurations for PCI Host Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 0100_001 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 6 | 300.0 | 400.0 | 6 | 50.0 | 66.7 |
| 0100_010 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 7 | 350.0 | 466.6 | 6 | 50.0 | 66.7 |
| 0100_011 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 8 | 400.0 | 533.3 | 6 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0101_000 | 60.0 | 66.7 | 2 | 120.0 | 133.3 | 2.5 | 150.0 | 166.7 | 2 | 60.0 | 66.7 |
| 0101_001 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 3 | 150.0 | 200.0 | 2 | 50.0 | 66.7 |
| 0101_010 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 3.5 | 175.0 | 233.3 | 2 | 50.0 | 66.7 |
| 0101_011 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 4 | 200.0 | 266.6 | 2 | 50.0 | 66.7 |
| 0101_100 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 4.5 | 225.0 | 300.0 | 2 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0101_101 | 83.3 | 111.1 | 3 | 250.0 | 333.3 | 3.5 | 291.7 | 388.9 | 5 | 50.0 | 66.7 |
| 0101_110 | 83.3 | 111.1 | 3 | 250.0 | 333.3 | 4 | 333.3 | 444.4 | 5 | 50.0 | 66.7 |
| 0101_111 | 83.3 | 111.1 | 3 | 250.0 | 333.3 | 4.5 | 375.0 | 500.0 | 5 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0110_000 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 2.5 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0110_001 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 3 | 50.0 | 66.7 |
| 0110_010 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 3 | 50.0 | 66.7 |
| 0110_011 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 4 | 240.0 | 320.0 | 3 | 50.0 | 66.7 |
| 0110_100 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 4.5 | 270.0 | 360.0 | 3 | 50.0 | 66.7 |
| 0110_101 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 5 | 300.0 | 400.0 | 3 | 50.0 | 66.7 |
| 0110_110 | 60.0 | 80.0 | 2.5 | 150.0 | 200.0 | 6 | 360.0 | 480.0 | 3 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 0111_000 | Reserved | | | | | | | | | | |
| 0111_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0111_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 175.0 | 233.3 | 3 | 50.0 | 66.7 |
| 0111_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 200.0 | 266.6 | 3 | 50.0 | 66.7 |
| 0111_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4.5 | 225.0 | 300.0 | 3 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1000_000 | Reserved | | | | | | | | | | |
| 1000_001 | 66.7 | 88.9 | 3 | 200.0 | 266.6 | 3 | 200.0 | 266.6 | 4 | 50.0 | 66.7 |

**Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1000_010 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 3.5 | 233.3 | 466.7 | 8 | 25.0 | 50.0 |
| 1000_011 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 4 | 266.7 | 533.3 | 8 | 25.0 | 50.0 |
| 1000_100 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 4.5 | 300.0 | 600.0 | 8 | 25.0 | 50.0 |
| 1000_101 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 6 | 400.0 | 800.0 | 8 | 25.0 | 50.0 |
| 1000_110 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 6.5 | 433.3 | 866.7 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1001_000 | Reserved | | | | | | | | | | |
| 1001_001 | Reserved | | | | | | | | | | |
| 1001_010 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 3.5 | 200.0 | 400.0 | 8 | 25.0 | 50.0 |
| 1001_011 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 4 | 228.6 | 457.1 | 8 | 25.0 | 50.0 |
| 1001_100 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 4.5 | 257.1 | 514.3 | 8 | 25.0 | 50.0 |
| 1001_101 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 5 | 214.3 | 428.6 | 6 | 25.0 | 50.0 |
| 1001_110 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 5.5 | 235.7 | 471.4 | 6 | 25.0 | 50.0 |
| 1001_111 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 6 | 257.1 | 514.3 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1010_000 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 2 | 150.0 | 300.0 | 6 | 25.0 | 50.0 |
| 1010_001 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 2.5 | 187.5 | 375.0 | 6 | 25.0 | 50.0 |
| 1010_010 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 3 | 225.0 | 450.0 | 6 | 25.0 | 50.0 |
| 1010_011 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 3.5 | 262.5 | 525.0 | 6 | 25.0 | 50.0 |
| 1010_100 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 4 | 300.0 | 600.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1010_101 | 100.0 | 200.0 | 2 | 200.0 | 400.0 | 2.5 | 250.0 | 500.0 | 8 | 25.0 | 50.0 |
| 1010_110 | 100.0 | 200.0 | 2 | 200.0 | 400.0 | 3 | 300.0 | 600.0 | 8 | 25.0 | 50.0 |
| 1010_111 | 100.0 | 200.0 | 2 | 200.0 | 400.0 | 3.5 | 350.0 | 700.0 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1011_000 | Reserved | | | | | | | | | | |
| 1011_001 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 2.5 | 200.0 | 400.0 | 8 | 25.0 | 50.0 |
| 1011_010 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 3 | 240.0 | 480.0 | 8 | 25.0 | 50.0 |
| 1011_011 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 3.5 | 280.0 | 560.0 | 8 | 25.0 | 50.0 |
| 1011_100 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 4 | 320.0 | 640.0 | 8 | 25.0 | 50.0 |

**Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1011_101 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 4.5 | 360.0 | 720.0 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1101_000 | 50.0 | 100.0 | 2.5 | 125.0 | 250.0 | 3 | 150.0 | 300.0 | 5 | 25.0 | 50.0 |
| 1101_001 | 50.0 | 100.0 | 2.5 | 125.0 | 250.0 | 3.5 | 175.0 | 350.0 | 5 | 25.0 | 50.0 |
| 1101_010 | 50.0 | 100.0 | 2.5 | 125.0 | 250.0 | 4 | 200.0 | 400.0 | 5 | 25.0 | 50.0 |
| 1101_011 | 50.0 | 100.0 | 2.5 | 125.0 | 250.0 | 4.5 | 225.0 | 450.0 | 5 | 25.0 | 50.0 |
| 1101_100 | 50.0 | 100.0 | 2.5 | 125.0 | 250.0 | 5 | 250.0 | 500.0 | 5 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1101_101 | 62.5 | 125.0 | 2 | 125.0 | 250.0 | 3 | 187.5 | 375.0 | 5 | 25.0 | 50.0 |
| 1101_110 | 62.5 | 125.0 | 2 | 125.0 | 250.0 | 4 | 250.0 | 500.0 | 5 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1110_000 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 3.5 | 175.0 | 350.0 | 6 | 25.0 | 50.0 |
| 1110_001 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 6 | 25.0 | 50.0 |
| 1110_010 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 4.5 | 225.0 | 450.0 | 6 | 25.0 | 50.0 |
| 1110_011 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 5 | 250.0 | 500.0 | 6 | 25.0 | 50.0 |
| 1110_100 | 50.0 | 100.0 | 3 | 150.0 | 300.0 | 5.5 | 275.0 | 550.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1100_000 | Reserved | | | | | | | | | | |
| 1100_001 | Reserved | | | | | | | | | | |
| 1100_010 | Reserved | | | | | | | | | | |

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

2 PCI_MODCK determines the PCI clock frequency range. See Table 17 for higher range configurations.

3 MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

4 CPM multiplication factor = CPM clock/bus clock

5 CPU multiplication factor = Core PLL multiplication factor

6 CPM_CLK/PCI_CLK ratio. When PCI_MODCK = 1, the ratio of CPM_CLK/PCI_CLK should be calculated from PCIDF as follows:
PCIDF = 3 > CPM_CLK/PCI_CLK = 4
PCIDF = 5 > CPM_CLK/PCI_CLK = 6
PCIDF = 7 > CPM_CLK/PCI_CLK = 8
PCIDF = 9 > CPM_CLK/PCI_CLK = 5
PCIDF = B > CPM_CLK/PCI_CLK = 6

## 7.2 PCI Agent Mode

These tables show configurations for PCI agent mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device. Note that in PCI agent mode the input clock is PCI clock.

**Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2]**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| **Default Modes (MODCK_H=0000)** | | | | | | | | | | | |
| 0000_000 | 60.0 | 66.7 | 2 | 120.0 | 133.3 | 2.5 | 150.0 | 166.7 | 2 | 60.0 | 66.7 |
| 0000_001 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 3 | 150.0 | 200.0 | 2 | 50.0 | 66.7 |
| 0000_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 150.0 | 200.0 | 3 | 50.0 | 66.7 |
| 0000_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 200.0 | 266.6 | 3 | 50.0 | 66.7 |
| 0000_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 2.5 | 60.0 | 80.0 |
| 0000_101 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 2.5 | 60.0 | 80.0 |
| 0000_110 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 233.3 | 311.1 | 3 | 66.7 | 88.9 |
| 0000_111 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 240.0 | 320.0 | 2.5 | 80.0 | 106.7 |
| **Full Configuration Modes** | | | | | | | | | | | |
| 0001_001 | 60.0 | 66.7 | 2 | 120.0 | 133.3 | 5 | 150.0 | 166.7 | 4 | 30.0 | 33.3 |
| 0001_010 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 6 | 150.0 | 200.0 | 4 | 25.0 | 33.3 |
| 0001_011 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 7 | 175.0 | 233.3 | 4 | 25.0 | 33.3 |
| 0001_100 | 50.0 | 66.7 | 2 | 100.0 | 133.3 | 8 | 200.0 | 266.6 | 4 | 25.0 | 33.3 |
| | | | | | | | | | | | |
| 0010_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 2.5 | 60.0 | 80.0 |
| 0010_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 2.5 | 60.0 | 80.0 |
| 0010_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 240.0 | 320.0 | 2.5 | 60.0 | 80.0 |
| 0010_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4.5 | 270.0 | 360.0 | 2.5 | 60.0 | 80.0 |
| | | | | | | | | | | | |

**Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1100_101 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 4 | 400.0 | 533.3 | 3 | 100.0 | 133.3 |
| 1100_110 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 4.5 | 450.0 | 599.9 | 3 | 100.0 | 133.3 |
| 1100_111 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 5 | 500.0 | 666.6 | 3 | 100.0 | 133.3 |
| 1101_000 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 5.5 | 550.0 | 733.3 | 3 | 100.0 | 133.3 |
| | | | | | | | | | | | |
| 1101_001 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 3.5 | 420.0 | 559.9 | 2.5 | 120.0 | 160.0 |
| 1101_010 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 4 | 480.0 | 639.9 | 2.5 | 120.0 | 160.0 |
| 1101_011 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 4.5 | 540.0 | 719.9 | 2.5 | 120.0 | 160.0 |
| 1101_100 | 50.0 | 66.7 | 6 | 300.0 | 400.0 | 5 | 600.0 | 799.9 | 2.5 | 120.0 | 160.0 |
| | | | | | | | | | | | |
| 1110_000 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 2.5 | 312.5 | 416.6 | 2 | 125.0 | 166.7 |
| 1110_001 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 3 | 375.0 | 500.0 | 2 | 125.0 | 166.7 |
| 1110_010 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 3.5 | 437.5 | 583.3 | 2 | 125.0 | 166.7 |
| 1110_011 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 4 | 500.0 | 666.6 | 2 | 125.0 | 166.7 |
| | | | | | | | | | | | |
| 1110_100 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 4 | 333.3 | 444.4 | 3 | 83.3 | 111.1 |
| 1110_101 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 4.5 | 375.0 | 500.0 | 3 | 83.3 | 111.1 |
| 1110_110 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 5 | 416.7 | 555.5 | 3 | 83.3 | 111.1 |
| 1110_111 | 50.0 | 66.7 | 5 | 250.0 | 333.3 | 5.5 | 458.3 | 611.1 | 3 | 83.3 | 111.1 |
| | | | | | | | | | | | |
| 1100_000 | Reserved | | | | | | | | | | |
| 1100_001 | Reserved | | | | | | | | | | |
| 1100_010 | Reserved | | | | | | | | | | |

1 The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

2 PCI_MODCK determines the PCI clock frequency range. See Table 20 for lower range configurations.

3 MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

4 CPM multiplication factor = CPM clock/bus clock

5 CPU multiplication factor = Core PLL multiplication factor

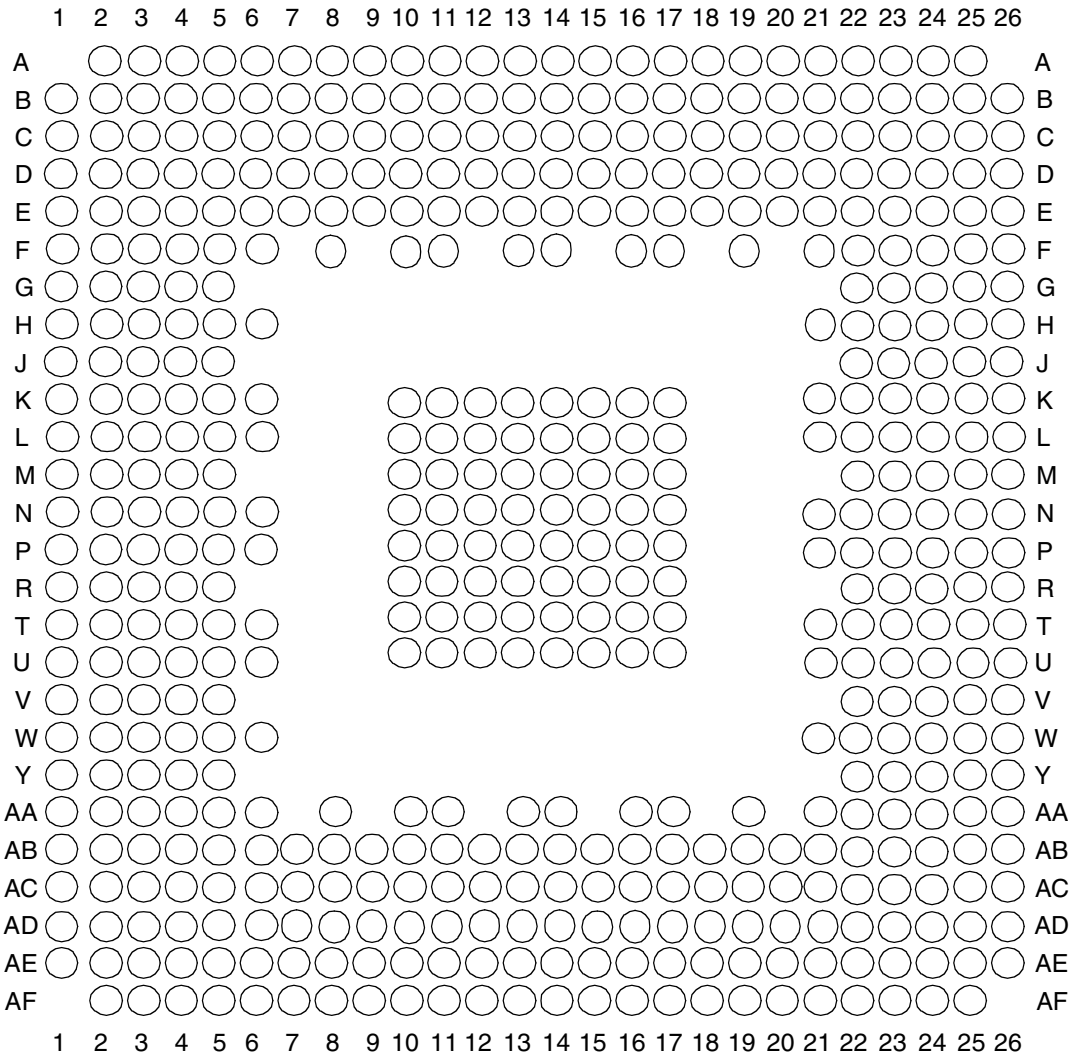
**Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 0100_100 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4.5 | 225.0 | 450.0 | 3 | 50.0 | 100.0 |
| | | | | | | | | | | | |
| 0101_000 | 30.0 | 50.0 | 5 | 150.0 | 250.0 | 2.5 | 150.0 | 250.0 | 2.5 | 60.0 | 100.0 |
| 0101_001 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 3 | 150.0 | 300.0 | 2.5 | 50.0 | 100.0 |
| 0101_010 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 3.5 | 175.0 | 350.0 | 2.5 | 50.0 | 100.0 |
| 0101_011 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 4 | 200.0 | 400.0 | 2.5 | 50.0 | 100.0 |
| 0101_100 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 4.5 | 225.0 | 450.0 | 2.5 | 50.0 | 100.0 |
| 0101_101 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 5 | 250.0 | 500.0 | 2.5 | 50.0 | 100.0 |
| 0101_110 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 5.5 | 275.0 | 550.0 | 2.5 | 50.0 | 100.0 |
| | | | | | | | | | | | |
| 0110_000 | Reserved | | | | | | | | | | |
| 0110_001 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3 | 200.0 | 400.0 | 3 | 66.7 | 133.3 |
| 0110_010 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3.5 | 233.3 | 466.7 | 3 | 66.7 | 133.3 |
| 0110_011 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4 | 266.7 | 533.3 | 3 | 66.7 | 133.3 |
| 0110_100 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4.5 | 300.0 | 600.0 | 3 | 66.7 | 133.3 |
| | | | | | | | | | | | |
| 0111_000 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 2 | 150.0 | 300.0 | 2 | 75.0 | 150.0 |
| 0111_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 2.5 | 187.5 | 375.0 | 2 | 75.0 | 150.0 |
| 0111_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 225.0 | 450.0 | 2 | 75.0 | 150.0 |
| 0111_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 262.5 | 525.0 | 2 | 75.0 | 150.0 |
| | | | | | | | | | | | |
| 1000_000 | Reserved | | | | | | | | | | |
| 1000_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 2.5 | 150.0 | 300.0 | 2.5 | 60.0 | 120.0 |
| 1000_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 180.0 | 360.0 | 2.5 | 60.0 | 120.0 |
| 1000_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 2.5 | 60.0 | 120.0 |
| 1000_100 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 240.0 | 480.0 | 2.5 | 60.0 | 120.0 |
| 1000_101 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4.5 | 270.0 | 540.0 | 2.5 | 60.0 | 120.0 |
| | | | | | | | | | | | |
| 1001_000 | Reserved | | | | | | | | | | |
| 1001_001 | Reserved | | | | | | | | | | |

**Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1001_010 | Reserved | | | | | | | | | | |
| 1001_011 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4 | 200.0 | 400.0 | 4 | 50.0 | 100.0 |
| 1001_100 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4.5 | 225.0 | 450.0 | 4 | 50.0 | 100.0 |
| | | | | | | | | | | | |
| 1010_000 | Reserved | | | | | | | | | | |
| 1010_001 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3 | 200.0 | 400.0 | 3 | 66.7 | 133.3 |
| 1010_010 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3.5 | 233.3 | 466.7 | 3 | 66.7 | 133.3 |
| 1010_011 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4 | 266.7 | 533.3 | 3 | 66.7 | 133.3 |
| 1010_100 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4.5 | 300.0 | 600.0 | 3 | 66.7 | 133.3 |
| | | | | | | | | | | | |
| 1011_000 | Reserved | | | | | | | | | | |
| 1011_001 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 2.5 | 200.0 | 400.0 | 2.5 | 80.0 | 160.0 |
| 1011_010 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3 | 240.0 | 480.0 | 2.5 | 80.0 | 160.0 |
| 1011_011 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3.5 | 280.0 | 560.0 | 2.5 | 80.0 | 160.0 |
| 1011_100 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4 | 320.0 | 640.0 | 2.5 | 80.0 | 160.0 |
| | | | | | | | | | | | |
| 1011_101 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 2.5 | 250.0 | 500.0 | 2 | 100.0 | 200.0 |
| 1011_110 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3 | 300.0 | 600.0 | 2 | 100.0 | 200.0 |
| 1011_111 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3.5 | 350.0 | 700.0 | 2 | 100.0 | 200.0 |
| | | | | | | | | | | | |
| 1100_101 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 200.0 | 400.0 | 3 | 50.0 | 100.0 |
| 1100_110 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4.5 | 225.0 | 450.0 | 3 | 50.0 | 100.0 |
| 1100_111 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 5 | 250.0 | 500.0 | 3 | 50.0 | 100.0 |
| 1101_000 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 5.5 | 275.0 | 550.0 | 3 | 50.0 | 100.0 |
| | | | | | | | | | | | |
| 1101_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 2.5 | 60.0 | 120.0 |
| 1101_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 240.0 | 480.0 | 2.5 | 60.0 | 120.0 |
| 1101_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4.5 | 270.0 | 540.0 | 2.5 | 60.0 | 120.0 |
| 1101_100 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 5 | 300.0 | 600.0 | 2.5 | 60.0 | 120.0 |
| | | | | | | | | | | | |

This figure shows the pinout of the 516 PBGA package as viewed from the top surface.




Not to Scale

**Figure 12. Pinout of the 516 PBGA Package (View from Top)**

This table lists the pins of the MPC8272. Note that the pins in the “MPC8272/8271 Only” column relate to Utopia functionality.

**Table 21. Pinout**

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| $\overline{BR}$ | | A19 |
| $\overline{BG}$/$\overline{IRQ6}$ | | D2 |
| $\overline{ABB}$/$\overline{IRQ2}$ | | C1 |

Table 21. Pinout (continued)

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| D15 | | G3 |
| D16 | | AB3 |
| D17 | | Y1 |
| D18 | | T4 |
| D19 | | T3 |
| D20 | | P2 |
| D21 | | M1 |
| D22 | | J1 |
| D23 | | G4 |
| D24 | | AB2 |
| D25 | | W4 |
| D26 | | V2 |
| D27 | | T1 |
| D28 | | N5 |
| D29 | | L1 |
| D30 | | H1 |
| D31 | | G5 |
| D32 | | W5 |
| D33 | | W2 |
| D34 | | T5 |
| D35 | | T2 |
| D36 | | N1 |
| D37 | | K3 |
| D38 | | H2 |
| D39 | | F1 |
| D40 | | AA2 |
| D41 | | W1 |
| D42 | | U3 |
| D43 | | R2 |
| D44 | | N2 |
| D45 | | L2 |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| $\overline{\text{PCI\_IRDY}}$ | | AF15 |
| $\overline{\text{PCI\_STOP}}$ | | AE15 |
| $\overline{\text{PCI\_DEVSEL}}$ | | AE14 |
| PCI_IDSEL | | AC17 |
| $\overline{\text{PCI\_PERR}}$ | | AD14 |
| $\overline{\text{PCI\_SERR}}$ | | AD13 |
| $\overline{\text{PCI\_REQ0}}$ | | AE20 |
| $\overline{\text{PCI\_REQ1}}$/CPCI_HS_ES | | AF14 |
| $\overline{\text{PCI\_GNT0}}$ | | AD20 |
| $\overline{\text{PCI\_GNT1}}$/CPCI_HS_LED | | AE13 |
| $\overline{\text{PCI\_GNT2}}$/$\overline{\text{CPCI\_HS\_ENUM}}$ | | AF21 |
| $\overline{\text{PCI\_RST}}$ | | AF22 |
| $\overline{\text{PCI\_INTA}}$ | | AE21 |
| $\overline{\text{PCI\_REQ2}}$ | | AB14 |
| DLLOUT | | AC22 |
| PCI_AD0 | | AF7 |
| PCI_AD1 | | AE10 |
| PCI_AD2 | | AB10 |
| PCI_AD3 | | AD10 |
| PCI_AD4 | | AE9 |
| PCI_AD5 | | AF8 |
| PCI_AD6 | | AC10 |
| PCI_AD7 | | AE11 |
| PCI_AD8 | | AB11 |
| PCI_AD9 | | AF10 |
| PCI_AD10 | | AF9 |
| PCI_AD11 | | AB12 |
| PCI_AD12 | | AC12 |
| PCI_AD13 | | AD12 |
| PCI_AD14 | | AF11 |
| PCI_AD15 | | AB13 |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| **MPC8272/MPC8248 and MPC8271/MPC8247** | **MPC8272/MPC8271 Only** | |
| PA31/FCC1_MII_COL | $\overline{\text{FCC1\_UT\_TXENB}}$ | G22[3] |
| PB18/FCC2_MII_HDLC_RXD3 | | T25[3] |
| PB19/FCC2_MII_HDLC_RXD2 | | P22[3] |
| PB20/FCC2_MII_HDLC_RMII_RXD1 | | L25[3] |
| PB21/FCC2_MII_HDLC_RMII_RXD0/FCC2_TRAN_RXD | | J26[3] |
| PB22/FCC2_MII_HDLC_TXD0/FCC2_TRAN_TXD/ FCC2_RMII_TXD0 | | U23[3] |
| PB23/FCC2_MII_HDLC_TXD1/FCC2_RMII_TXD1 | | U26[3] |
| PB24/FCC2_MII_HDLC_TXD2/L1RSYNCB2 | | M24[3] |
| PB25/FCC2_MII_HDLC_TXD3/L1TSYNCB2 | | M23[3] |
| PB26/FCC2_MII_CRS/L1RXDB2 | | H24[3] |
| PB27/FCC2_MII_COL/L1TXDB2 | | E25[3] |
| PB28/FCC2_MII_RMII_RX_ER/$\overline{\text{FCC2\_RTS}}$/TXD1 | | D26[3] |
| PB29/FCC2_MII_RMII_TX_EN | | K21[3] |
| PB30/FCC2_MII_RX_DV/FCC2_RMII_CRS_DV | | D24[3] |
| PB31/FCC2_MII_TX_ER | | E23[3] |
| PC0/$\overline{\text{DREQ3}}$/BRGO7/$\overline{\text{SMSYN1}}$/L1CLKOA2 | | AF23[3] |
| PC1/BRGO6/$\overline{\text{L1RQA2}}$ | | AD23[3] |
| PC4/SMRXD1/SI2_L1ST4/$\overline{\text{FCC2\_CD}}$ | | AB22[3] |
| PC5/SMTXD1/SI2_L1ST3/$\overline{\text{FCC2\_CTS}}$ | | AE24[3] |
| PC6/$\overline{\text{FCC1\_CD}}$/SI2_L1ST2 | FCC1_UT_RXADDR2 | AF24[3] |
| PC7/$\overline{\text{FCC1\_CTS}}$ | FCC1_UT_TXADDR2 | AE26[3] |
| PC8/$\overline{\text{CD4}}$/RTS1/SI2_L1ST2/$\overline{\text{CTS3}}$ | | AC24[3] |
| PC9/$\overline{\text{CTS4}}$/L1TSYNCA2 | | AA23[3] |
| PC10/$\overline{\text{CD3}}$/USB_RN | | AB25[3] |
| PC11/$\overline{\text{CTS3}}$/USB_RP/L1TXD3A2 | | V22[3] |
| PC12 | FCC1_UT_RXADDR1 | AA26[3] |
| PC13/BRGO5 | FCC1_UT_TXADDR1 | V23[3] |
| PC14/$\overline{\text{CD1}}$ | FCC1_UT_RXADDR0 | W24[3] |
| PC15/$\overline{\text{CTS1}}$ | FCC1_UT_TXADDR0 | U24[3] |
| PC16/CLK16 | | T23[3] |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| CLKIN2 | | C21 |
| No connect[4] | | D19[4], J3[4], AD24[5] |
| I/O power | | B4, F3, J2, N4, AD1, AD5, AE8, AC13, AD18, AB24, AB26, W23, R25, M25, F25, C25, C22, B17, B12, B8, E6, F6, H6, L5, L6, P6, T6, U6, V5, Y5, AA6, AA8, AA10, AA11, AA14, AA16, AA17, AB19, AB20, W21, U21, T21, P21, N21, M22, J22, H21, F21, F19, F17, E16, F14, E13, E12, F10, E10, E9 |
| Core Power | | F5, K5, M5, AA5, AB7, AA13, AA19, AA21, Y22, AC25, U22, R22, L21, H22, E22, E20, E15, F13, F11, F8, L3, V4, W3, AC11, AD11, AB15, U25, T24, J24, H25, F23, B19, D17, C17, D10, C10 |
| Ground | | E19, E2, K1, Y2, AE1, AE4, AD9, AC14, AE17, AC19, AE25, V24, P26, M26, G26, E26, B21, C12, C11, C8, A8, B18, A18, A2, B1, B2, A5, C5, D4, D6, G2, L4, P1, R1, R4, AC4, AE7, AC23, Y25, N24, J23, A23, D23, D20, E18, A13, A16, K10, K11, K12, K13, K14, K15, K16, K17, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, R10, R11,R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17 |

1 Must be tied to ground.

2 Should be tied to VDDH via a 2K Ω external pull-up resistor.

3 The default configuration of the CPM pins (PA[8–31], PB[18–31], PC[0–1,4–29], PD[7–25, 29–31]) is input. To prevent excessive DC current, it is recommended either to pull unused pins to GND or VDDH, or to configure them as outputs.

4 This pin is not connected. It should be left floating.

5 Must be pulled down or left floating

**Table 23. Document Revision History (continued)**

| Revision | Date | Substantive Changes |
|---|---|---|
| 1.2 | 09/2005 | • Added 133-MHz to the list of frequencies in the opening sentence of Section 6, "AC Electrical Characteristics".<br>• Added 133 MHz columns to Table 9, Table 11, Table 12, and Table 13.<br>• Added footnote 2 to Table 13.<br>• Added the conditions note directly above Table 12. |
| 1.1 | 01/2005 | • Modification for correct display of assertion level ("overbar") for some signals |
| 1.0 | 12/2004 | • Section 1.1: Added 8:1 ratio to Internal CPM/bus clock multiplier values<br>• Section 2: removed voltage tracking note<br>• Table 3: Note 2 updated regarding VDD/VCCSYN relationship to VDDH during power-on reset<br>• Table 4: Updated VDD and VCCSYN to 1.425 V - 1.575 V<br>• Table 8: Note 2 updated to reflect VIH=2.5 for TCK, TRST, PORESET; request for external pull-up removed.<br>• Section 4.6: Updated description of layout practices<br>• Table 8: Note 3 added regarding IIC compatibility<br>• Table 8: Updated nominal and maximum power dissipation values<br>• Table 9: updated PCI impedance to 27Ω, updated 60x and MEMC values and added note to reflect configurable impedance<br>• Section 6: Added sentence providing derating factor<br>• Section 6.1: added Note: Rise/Fall Time on CPM Input Pins<br>• Table 9: updated values for following specs: sp36b, sp37a, sp38a, sp39a, sp38b, sp40, sp41, sp42, sp43, sp42a<br>• Table 11: updated values for following specs: sp16a, sp16b, sp18a, sp18b, sp20, sp21, sp22<br>• Section 6.2: added spread spectrum clocking note<br>• Section 6.2: added CLKIN jitter note<br>• Table 12: combined specs sp11 and sp11a<br>• Table 13: sp30 Data Bus minimum delay values changed to 0.8<br>• Section 7: unit of ns added to Tval notes<br>• Section 7: Updated all notes to reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz.<br>• Section 7, "Clock Configuration Modes": Updated all table footnotes reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz.<br>• Table 21: correct superscript of footnote number after pin AD22<br>• Table 21: remove DONE3 from PC12<br>• Table 21: signals referring to TDMs C2 and D2 removed |

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