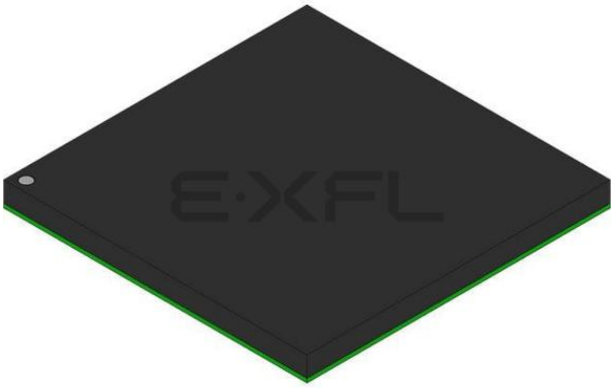
# Freescale Semiconductor - MPC8272VRTIEA Datasheet



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## Understanding Embedded - Microprocessors

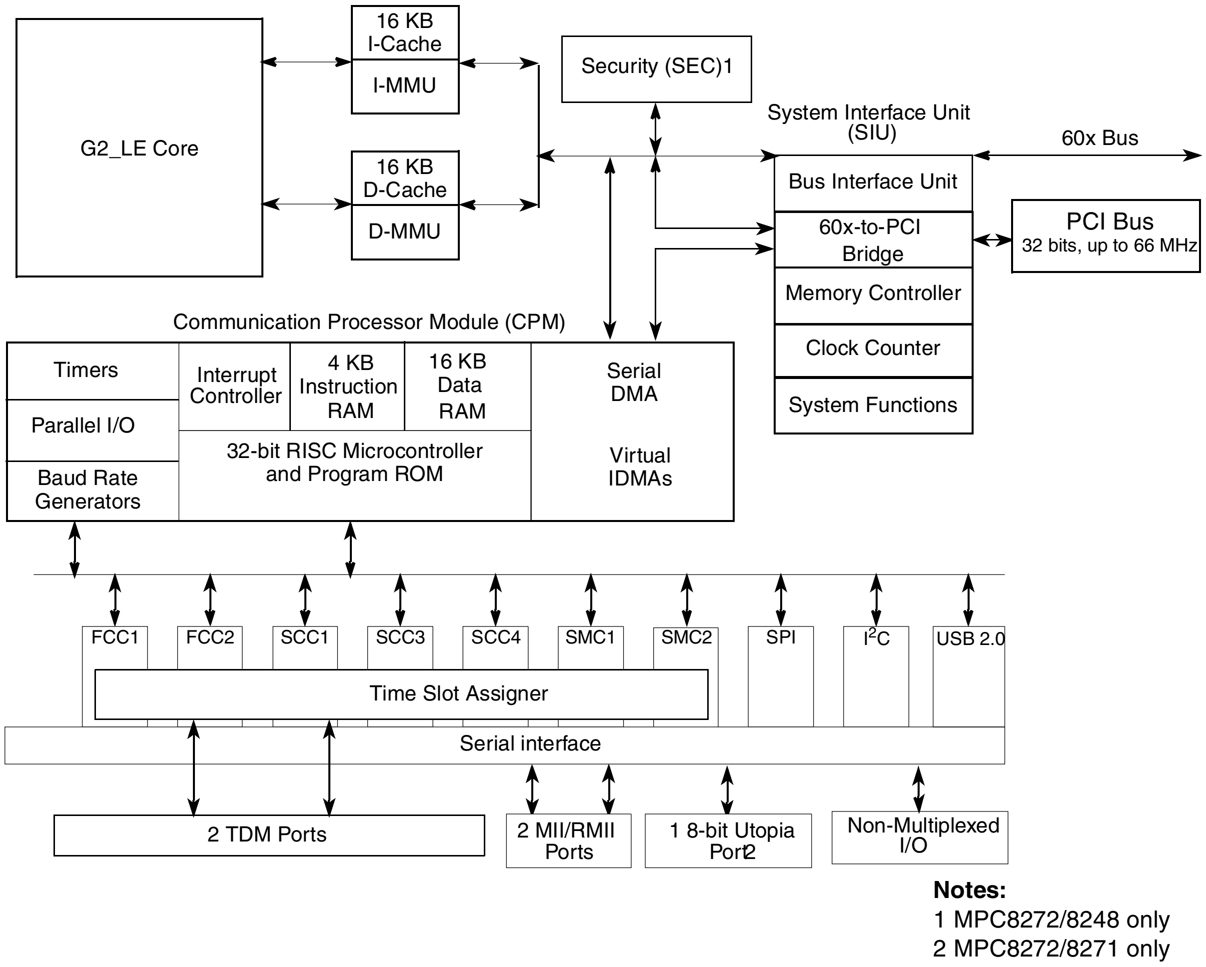
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | PowerPC G2_LE |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 400MHz |
| Co-Processors/DSP | Communications; RISC CPM, Security; SEC |
| RAM Controllers | DRAM, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100Mbps (2) |
| SATA | - |
| USB | USB 2.0 (1) |
| Voltage - I/O | 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 516-BBGA |
| Supplier Device Package | 516-FPBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8272vrtiea |

This figure shows the block diagram of the SoC.



**Notes:**
1 MPC8272/8248 only
2 MPC8272/8271 only

**Figure 1. SoC Block Diagram**

## 1.1 Features

The major features of the SoC are as follows:

- Dual-issue integer (G2_LE) core
  - — A core version of the MPC603e microprocessor
  - — System core microprocessor supporting frequencies of 266–400 MHz
  - — Separate 16 KB data and instruction caches:
    - – Four-way set associative
    - – Physically addressed
    - – LRU replacement algorithm
  - — Power Architecture®-compliant memory management unit (MMU)
  - — Common on-chip processor (COP) test interface
  - — Supports bus snooping for cache coherency

[5] MPC8272 and MPC8271 only.

**Table 6.**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input high voltage—all inputs except TCK, TRST and PORESET[1] | $V_{IH}$ | 2.0 | 3.465 | V |
| Input low voltage | $V_{IL}$ | GND | 0.8 | V |
| CLKIN input high voltage | $V_{IHC}$ | 2.4 | 3.465 | V |
| CLKIN input low voltage | $V_{ILC}$ | GND | 0.4 | V |
| Input leakage current, $V_{IN}$ = VDDH[2] | $I_{IN}$ | — | 10 | µA |
| Hi-Z (off state) leakage current, $V_{IN}$ = VDDH[2] | $I_{OZ}$ | — | 10 | µA |
| Signal low input current, $V_{IL}$ = 0.8 V[3] | $I_L$ | — | 1 | µA |
| Signal high input current, $V_{IH}$ = 2.0 V | $I_H$ | — | 1 | µA |
| Output high voltage, $I_{OH}$ = –2 mA<br>except UTOPIA mode, and open drain pins<br><br>In UTOPIA mode[4] (UTOPIA pins only): $I_{OH}$ = -8.0mA | $V_{OH}$ | 2.4 | — | V |
| In UTOPIA mode[4] (UTOPIA pins only): $I_{OL}$ = 8.0mA | $V_{OL}$ | — | 0.5 | V |
| $I_{OL}$ = 6.0mA<br>BR<br>BG<br>ABB/IRQ2<br>TS<br>A[0-31]<br>TT[0-4]<br>TBST<br>TSIZE[0–3]<br>AACK<br>ARTRY<br>DBG<br>DBB/IRQ3<br>D[0-63]<br>//EXT_BR3<br>//EXT_BG3<br>/TBEN/EXT_DBG3/CINT<br>PSDVAL<br>TA<br>TEA<br>GBL/IRQ1<br>CI/BADDR29/IRQ2<br>WT/BADDR30/IRQ3<br>BADDR31/IRQ5/CINT<br>CPU_BR<br>IRQ0/NMI_OUT<br>/PCI_RST<br>HRESET<br>SRESET<br>RSTCONF | $V_{OL}$ | — | 0.4 | V |

## 4.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

## 4.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages, especially PBGA packages, is strongly dependent on the board temperature.

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)
$T_B$ = board temperature (ºC)
$P_D$ = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

## 4.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application, or a more accurate and complex model of the package can be used in the thermal simulation.

## 4.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter ($\Psi_{JT}$) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

$\Psi_{JT}$ = thermal characterization parameter

$T_T$ = thermocouple temperature on top of package

$P_D$ = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the case to avoid measurement errors caused by cooling effects of the thermocouple wire.

## 4.6 Layout Practices

Each VDD and VDDH pin should be provided with a low-impedance path to the board’s power supplies. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The VDD and VDDH power supplies should be bypassed to ground using bypass capacitors located as close as possible to the four sides of the package. For filtering high frequency noise, a capacitor of 0.1uF on each VDD and VDDH pin is recommended. Further, for medium frequency noise, a total of 2 capacitors of 47uF for VDD and 2 capacitors of 47uF for VDDH are also recommended. The capacitor leads and associated printed circuit traces connecting to chip VDD, VDDH and ground should be kept to less than half an inch per capacitor lead. Boards should employ separate inner layers for power and GND planes.

All output pins on the SoC have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the VDD and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

This figure shows the FCC external clock.

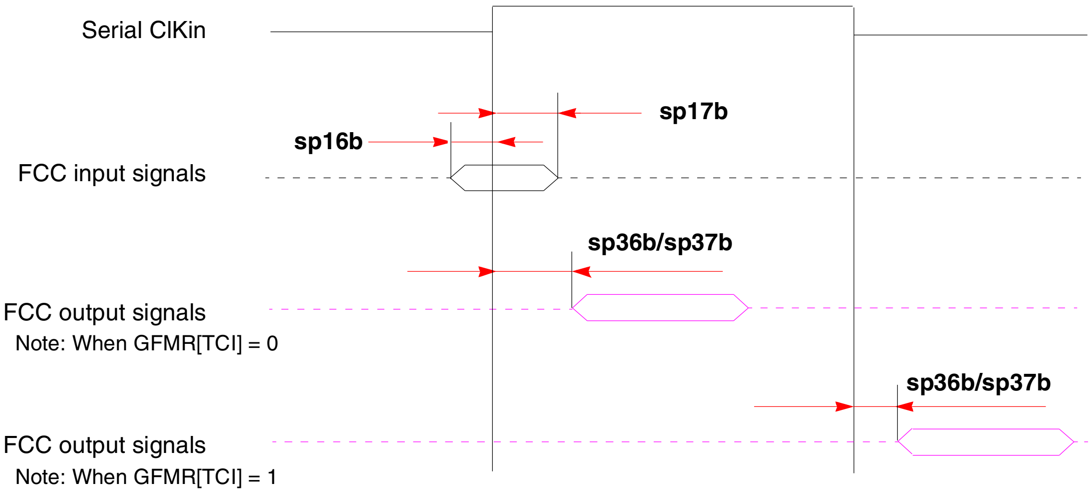
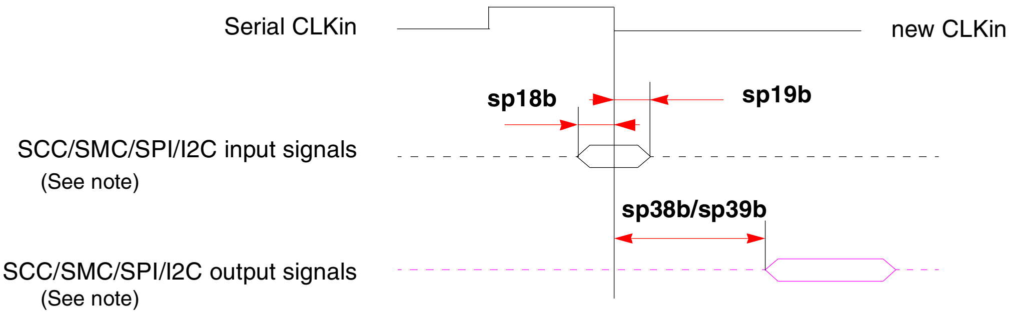


**Figure 4. FCC External Clock Diagram**

This figure shows the SCC/SMC/SPI/I$^2$C external clock.



**Note:** There are four possible timing conditions for SPI:

1. Input sampled on the rising edge and output driven on the rising edge.
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge (shown).
4. Input sampled on the falling edge and output driven on the rising edge.

**Note:** There are two possible timing conditions for SCC/SMC/I$^2$C:

1. Input sampled on the falling edge and output driven on the falling edge (shown).
2. Input sampled on the falling edge and output driven on the rising edge.

**Figure 5. SCC/SMC/SPI/I$^2$C External Clock Diagram**

## NOTE: Conditions

The following conditions must be met in order to operate the MPC8272 family devices with 133 MHz bus: single PowerQUICC II Bus mode must be used (no external master, BCR[EBM] = 0); data bus must be in Pipeline mode (BRx[DR] = 1); internal arbiter and memory controller must be used. For expected load of above 40 pF, it is recommended that data and address buses be configured to low (25 Ω) impedance (SIUMCR[HLBE0] = 1, SIUMCR[HLBE1] = 1).

**Table 12. AC Characteristics for SIU Inputs[1]**

| Spec Number | | Characteristic | Value (ns) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Setup | | | | Hold | | | |
| Setup | Hold | | 66 MHz | 83 MHz | 100 MHz | 133 MHz | 66 MHz | 83 MHz | 100 MHz | 133 MHz |
| sp11 | sp10 | $\overline{\mathrm{AACK}}$/$\overline{\mathrm{TA}}$/$\overline{\mathrm{TS}}$/$\overline{\mathrm{DBG}}$/$\overline{\mathrm{BG}}$/$\overline{\mathrm{BR}}$/$\overline{\mathrm{ARTRY}}$/$\overline{\mathrm{TEA}}$ | 6 | 5 | 3.5 | N/A | 0.5 | 0.5 | 0.5 | N/A |
| sp12 | sp10 | Data bus in normal mode | 5 | 4 | 3.5 | N/A | 0.5 | 0.5 | 0.5 | N/A |
| sp13 | sp10 | Data bus in pipeline mode (without ECC and PARITY) | N/A | 4 | 2.5 | 1.5 | N/A | 0.5 | 0.5 | 0.5 |
| sp15 | sp10 | All other pins | 5 | 4 | 3.5 | N/A | 0.5 | 0.5 | 0.5 | N/A |

[1] Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

This table lists SIU output characteristics.

**Table 13. AC Characteristics for SIU Outputs[1]**

| Spec Number | | Characteristic | Value (ns) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Maximum Delay | | | | Minimum Delay | | | |
| Max | Min | | 66 MHz | 83 MHz | 100 MHz | 133 MHz | 66 MHz | 83 MHz | 100 MHz | 133 MHz |
| sp31 | sp30 | $\overline{\mathrm{PSDVAL}}$/$\overline{\mathrm{TEA}}$/$\overline{\mathrm{TA}}$ | 7 | 6 | 5.5 | N/A | 1 | 1 | 1 | N/A |
| sp32 | sp30 | ADD/ADD_atr./BADDR/CI/GBL/WT | 8 | 6.5 | 5.5 | 4.5[2] | 1 | 1 | 1 | 1 [2] |
| sp33 | sp30 | Data bus[3] | 6.5 | 6.5 | 5.5 | 4.5 | 0.8 | 0.8 | 0.8 | 1 |
| sp34 | sp30 | Memory controller signals/ALE | 6 | 5.5 | 5.5 | 4.5 | 1 | 1 | 1 | 1 |
| sp35 | sp30 | All other signals | 6 | 5.5 | 5.5 | N/A | 1 | 1 | 1 | N/A |

[1] Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

[2] Value is for ADD only; other sp32/sp30 signals are not applicable.

[3] To achieve 1 ns of hold time at 66.67/83.33/100 MHZ, a minimum loading of 20 pF is required.

This figure shows signal behavior in MEMC mode.

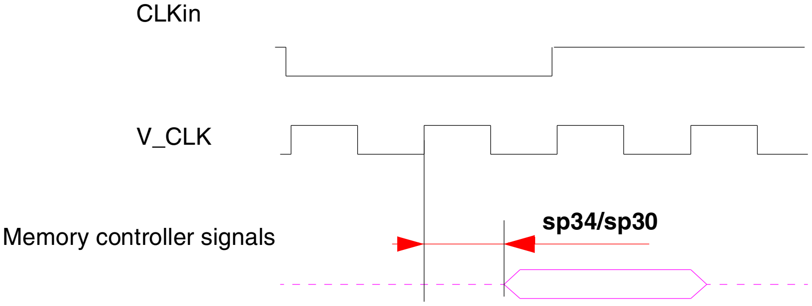


**Figure 10. MEMC Mode Diagram**

**NOTE**

Generally, all SoC bus and system output signals are driven from the rising edge of the input clock (CLKin). Memory controller signals, however, trigger on four points within a CLKin cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKin. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 14.

**Table 14. Tick Spacing for Memory Controller Signals**

| PLL Clock Ratio | Tick Spacing (T1 Occurs at the Rising Edge of CLKin) | | |
|---|---|---|---|
| | T2 | T3 | T4 |
| 1:2, 1:3, 1:4, 1:5, 1:6 | 1/4 CLKin | 1/2 CLKin | 3/4 CLKin |
| 1:2.5 | 3/10 CLKin | 1/2 CLKin | 8/10 CLKin |
| 1:3.5 | 4/14 CLKin | 1/2 CLKin | 11/14 CLKin |

This table is a representation of the information in Table 14.

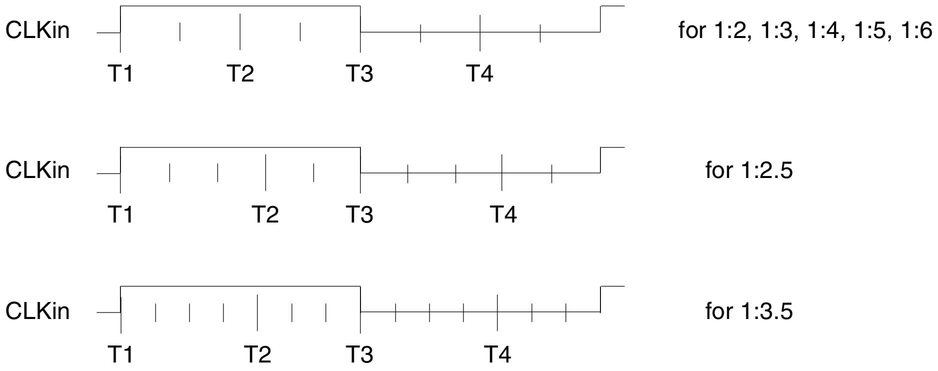


**Figure 11. Internal Tick Spacing for Memory Controller Signals**

**NOTE**

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin’s rising edge.

## 6.3 JTAG Timings

This table lists the JTAG timings.

**Table 15. JTAG Timings[1]**

| Parameter | Symbol[2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| JTAG external clock frequency of operation | $f_{JTG}$ | 0 | 33.3 | MHz | — |
| JTAG external clock cycle time | $t_{JTG}$ | 30 | — | ns | — |
| JTAG external clock pulse width measured at 1.4V | $t_{JTKHKL}$ | 15 | — | ns | — |
| JTAG external clock rise and fall times | $t_{JTGR}$ and $t_{JTGF}$ | 0 | 5 | ns | 6 |
| TRST assert time | $t_{TRST}$ | 25 | — | ns | 3, 6 |
| Input setup times | | | | | |
| Boundary-scan data | $t_{JTDVKH}$ | 4 | — | ns | 4, 7 |
| TMS, TDI | $t_{JTIVKH}$ | 4 | — | ns | 4, 7 |
| Input hold times | | | | | |
| Boundary-scan data | $t_{JTDXKH}$ | 10 | — | ns | 4, 7 |
| TMS, TDI | $t_{JTIXKH}$ | 10 | — | ns | 4, 7 |
| Output valid times | | | | | |
| Boundary-scan data | $t_{JTKLDV}$ | — | 10 | ns | 5, 7 |
| TDO | $t_{JTKLOV}$ | — | 10 | ns | 5. 7 |
| Output hold times | | | | | |
| Boundary-scan data | $t_{JTKLDX}$ | 1 | — | ns | 5, 7 |
| TDO | $t_{JTKLOX}$ | 1 | — | ns | 5, 7 |
| JTAG external clock to output high impedance | | | | | |
| Boundary-scan data | $t_{JTKLDZ}$ | 1 | 10 | ns | 5, 6 |
| TDO | $t_{JTKLOZ}$ | 1 | 10 | ns | 5, 6 |

[1] All outputs are measured from the midpoint voltage of the falling/rising edge of $t_{TCLK}$ to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

[2] The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{JTDVKH}$ symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{JTDXKH}$ symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

[3] TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

[4] Non-JTAG signal input timing with respect to $t_{TCLK}$.

[5] Non-JTAG signal output timing with respect to $t_{TCLK}$.

[6] Guaranteed by design.

[7] Guaranteed by design and device characterization.

**Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | Bus Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | PCI Division Factor[6] | PCI Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 1000_010 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 3.5 | 233.3 | 466.7 | 8 | 25.0 | 50.0 |
| 1000_011 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 4 | 266.7 | 533.3 | 8 | 25.0 | 50.0 |
| 1000_100 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 4.5 | 300.0 | 600.0 | 8 | 25.0 | 50.0 |
| 1000_101 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 6 | 400.0 | 800.0 | 8 | 25.0 | 50.0 |
| 1000_110 | 66.7 | 133.3 | 3 | 200.0 | 400.0 | 6.5 | 433.3 | 866.7 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1001_000 | Reserved | | | | | | | | | | |
| 1001_001 | Reserved | | | | | | | | | | |
| 1001_010 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 3.5 | 200.0 | 400.0 | 8 | 25.0 | 50.0 |
| 1001_011 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 4 | 228.6 | 457.1 | 8 | 25.0 | 50.0 |
| 1001_100 | 57.1 | 114.3 | 3.5 | 200.0 | 400.0 | 4.5 | 257.1 | 514.3 | 8 | 25.0 | 50.0 |
| 1001_101 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 5 | 214.3 | 428.6 | 6 | 25.0 | 50.0 |
| 1001_110 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 5.5 | 235.7 | 471.4 | 6 | 25.0 | 50.0 |
| 1001_111 | 42.9 | 85.7 | 3.5 | 150.0 | 300.0 | 6 | 257.1 | 514.3 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1010_000 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 2 | 150.0 | 300.0 | 6 | 25.0 | 50.0 |
| 1010_001 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 2.5 | 187.5 | 375.0 | 6 | 25.0 | 50.0 |
| 1010_010 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 3 | 225.0 | 450.0 | 6 | 25.0 | 50.0 |
| 1010_011 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 3.5 | 262.5 | 525.0 | 6 | 25.0 | 50.0 |
| 1010_100 | 75.0 | 150.0 | 2 | 150.0 | 300.0 | 4 | 300.0 | 600.0 | 6 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1010_101 | 100.0 | 200.0 | 2 | 200.0 | 400.0 | 2.5 | 250.0 | 500.0 | 8 | 25.0 | 50.0 |
| 1010_110 | 100.0 | 200.0 | 2 | 200.0 | 400.0 | 3 | 300.0 | 600.0 | 8 | 25.0 | 50.0 |
| 1010_111 | 100.0 | 200.0 | 2 | 200.0 | 400.0 | 3.5 | 350.0 | 700.0 | 8 | 25.0 | 50.0 |
| | | | | | | | | | | | |
| 1011_000 | Reserved | | | | | | | | | | |
| 1011_001 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 2.5 | 200.0 | 400.0 | 8 | 25.0 | 50.0 |
| 1011_010 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 3 | 240.0 | 480.0 | 8 | 25.0 | 50.0 |
| 1011_011 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 3.5 | 280.0 | 560.0 | 8 | 25.0 | 50.0 |
| 1011_100 | 80.0 | 160.0 | 2.5 | 200.0 | 400.0 | 4 | 320.0 | 640.0 | 8 | 25.0 | 50.0 |

### Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)[1,2] (continued)

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| | | | | | | | | | | | |
| 1000_000 | Reserved | | | | | | | | | | |
| 1000_001 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 2.5 | 150.0 | 166.7 | 2.5 | 60.0 | 80.0 |
| 1000_010 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3 | 180.0 | 240.0 | 2.5 | 60.0 | 80.0 |
| 1000_011 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 3.5 | 210.0 | 280.0 | 2.5 | 60.0 | 80.0 |
| 1000_100 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4 | 240.0 | 320.0 | 2.5 | 60.0 | 80.0 |
| 1000_101 | 50.0 | 66.7 | 3 | 150.0 | 200.0 | 4.5 | 270.0 | 360.0 | 2.5 | 60.0 | 80.0 |
| | | | | | | | | | | | |
| 1001_000 | Reserved | | | | | | | | | | |
| 1001_001 | Reserved | | | | | | | | | | |
| 1001_010 | Reserved | | | | | | | | | | |
| 1001_011 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4 | 200.0 | 266.6 | 4 | 50.0 | 66.7 |
| 1001_100 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4.5 | 225.0 | 300.0 | 4 | 50.0 | 66.7 |
| | | | | | | | | | | | |
| 1010_000 | Reserved | | | | | | | | | | |
| 1010_001 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 200.0 | 266.6 | 3 | 66.7 | 88.9 |
| 1010_010 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 233.3 | 311.1 | 3 | 66.7 | 88.9 |
| 1010_011 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4 | 266.7 | 355.5 | 3 | 66.7 | 88.9 |
| 1010_100 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4.5 | 300.0 | 400.0 | 3 | 66.7 | 88.9 |
| | | | | | | | | | | | |
| 1011_000 | Reserved | | | | | | | | | | |
| 1011_001 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 2.5 | 200.0 | 266.6 | 2.5 | 80.0 | 106.7 |
| 1011_010 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 240.0 | 320.0 | 2.5 | 80.0 | 106.7 |
| 1011_011 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 280.0 | 373.3 | 2.5 | 80.0 | 106.7 |
| 1011_100 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 4 | 320.0 | 426.6 | 2.5 | 80.0 | 106.7 |
| | | | | | | | | | | | |
| 1011_101 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 2.5 | 250.0 | 333.3 | 2 | 100.0 | 133.3 |
| 1011_110 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3 | 300.0 | 400.0 | 2 | 100.0 | 133.3 |
| 1011_111 | 50.0 | 66.7 | 4 | 200.0 | 266.6 | 3.5 | 350.0 | 466.6 | 2 | 100.0 | 133.3 |
| | | | | | | | | | | | |

**Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)[1,2] (continued)**

| Mode[3] | PCI Clock (MHz) | | CPM Multiplication Factor[4] | CPM Clock (MHz) | | CPU Multiplication Factor[5] | CPU Clock (MHz) | | Bus Division Factor | Bus Clock (MHz) | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MODCK_H-MODCK[1-3] | Low | High | | Low | High | | Low | High | | Low | High |
| 0100_100 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4.5 | 225.0 | 450.0 | 3 | 50.0 | 100.0 |
| | | | | | | | | | | | |
| 0101_000 | 30.0 | 50.0 | 5 | 150.0 | 250.0 | 2.5 | 150.0 | 250.0 | 2.5 | 60.0 | 100.0 |
| 0101_001 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 3 | 150.0 | 300.0 | 2.5 | 50.0 | 100.0 |
| 0101_010 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 3.5 | 175.0 | 350.0 | 2.5 | 50.0 | 100.0 |
| 0101_011 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 4 | 200.0 | 400.0 | 2.5 | 50.0 | 100.0 |
| 0101_100 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 4.5 | 225.0 | 450.0 | 2.5 | 50.0 | 100.0 |
| 0101_101 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 5 | 250.0 | 500.0 | 2.5 | 50.0 | 100.0 |
| 0101_110 | 25.0 | 50.0 | 5 | 125.0 | 250.0 | 5.5 | 275.0 | 550.0 | 2.5 | 50.0 | 100.0 |
| | | | | | | | | | | | |
| 0110_000 | Reserved | | | | | | | | | | |
| 0110_001 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3 | 200.0 | 400.0 | 3 | 66.7 | 133.3 |
| 0110_010 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 3.5 | 233.3 | 466.7 | 3 | 66.7 | 133.3 |
| 0110_011 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4 | 266.7 | 533.3 | 3 | 66.7 | 133.3 |
| 0110_100 | 25.0 | 50.0 | 8 | 200.0 | 400.0 | 4.5 | 300.0 | 600.0 | 3 | 66.7 | 133.3 |
| | | | | | | | | | | | |
| 0111_000 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 2 | 150.0 | 300.0 | 2 | 75.0 | 150.0 |
| 0111_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 2.5 | 187.5 | 375.0 | 2 | 75.0 | 150.0 |
| 0111_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 225.0 | 450.0 | 2 | 75.0 | 150.0 |
| 0111_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 262.5 | 525.0 | 2 | 75.0 | 150.0 |
| | | | | | | | | | | | |
| 1000_000 | Reserved | | | | | | | | | | |
| 1000_001 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 2.5 | 150.0 | 300.0 | 2.5 | 60.0 | 120.0 |
| 1000_010 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3 | 180.0 | 360.0 | 2.5 | 60.0 | 120.0 |
| 1000_011 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 3.5 | 210.0 | 420.0 | 2.5 | 60.0 | 120.0 |
| 1000_100 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4 | 240.0 | 480.0 | 2.5 | 60.0 | 120.0 |
| 1000_101 | 25.0 | 50.0 | 6 | 150.0 | 300.0 | 4.5 | 270.0 | 540.0 | 2.5 | 60.0 | 120.0 |
| | | | | | | | | | | | |
| 1001_000 | Reserved | | | | | | | | | | |
| 1001_001 | Reserved | | | | | | | | | | |

**Table 21. Pinout (continued)**

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| A30 | | B15 |
| A31 | | A15 |
| TT0 | | B3 |
| TT1 | | E8 |
| TT2 | | D7 |
| TT3 | | C4 |
| TT4 | | E7 |
| $\overline{\text{TBST}}$ | | E3 |
| TSIZ0 | | E4 |
| TSIZ1 | | E5 |
| TSIZ2 | | C3 |
| TSIZ3 | | D5 |
| $\overline{\text{AACK}}$ | | D3 |
| $\overline{\text{ARTRY}}$ | | C2 |
| $\overline{\text{DBG}}/\overline{\text{IRQ7}}$ | | F16 |
| $\overline{\text{DBB}}/\overline{\text{IRQ3}}$ | | D18 |
| D0 | | AC1 |
| D1 | | AA1 |
| D2 | | V3 |
| D3 | | R5 |
| D4 | | P4 |
| D5 | | M4 |
| D6 | | J4 |
| D7 | | G1 |
| D8 | | W6 |
| D9 | | Y3 |
| D10 | | V1 |
| D11 | | N6 |
| D12 | | P3 |
| D13 | | M2 |
| D14 | | J5 |

## Table 21. Pinout (continued)

| Pin Name | | Ball |
|---|---|---|
| **MPC8272/MPC8248 and MPC8271/MPC8247** | **MPC8272/MPC8271 Only** | |
| D46 | | H4 |
| D47 | | F2 |
| D48 | | AB1 |
| D49 | | U4 |
| D50 | | U1 |
| D51 | | R3 |
| D52 | | N3 |
| D53 | | K2 |
| D54 | | H5 |
| D55 | | F4 |
| D56 | | AA3 |
| D57 | | U5 |
| D58 | | U2 |
| D59 | | P5 |
| D60 | | M3 |
| D61 | | K4 |
| D62 | | H3 |
| D63 | | E1 |
| $\overline{\text{IRQ3}}$/$\overline{\text{CKSTP\_OUT}}$/$\overline{\text{EXT\_BR3}}$ | | B16 |
| $\overline{\text{IRQ4}}$/$\overline{\text{CORE\_SRESET}}$/$\overline{\text{EXT\_BG3}}$ | | C15 |
| $\overline{\text{IRQ5}}$/$\overline{\text{TBEN}}$/$\overline{\text{EXT\_DBG3}}$/$\overline{\text{CINT}}$ | | Y4 |
| $\overline{\text{PSDVAL}}$ | | C19 |
| $\overline{\text{TA}}$ | | AA4 |
| $\overline{\text{TEA}}$ | | AB6 |
| $\overline{\text{GBL}}$/$\overline{\text{IRQ1}}$ | | D15 |
| $\overline{\text{CI}}$/BADDR29/$\overline{\text{IRQ2}}$ | | D16 |
| $\overline{\text{WT}}$/BADDR30/$\overline{\text{IRQ3}}$ | | C16 |
| BADDR31/$\overline{\text{IRQ5}}$/$\overline{\text{CINT}}$ | | E17 |
| $\overline{\text{CPU\_BR}}$/$\overline{\text{INT\_OUT}}$ | | B20 |
| $\overline{\text{CS0}}$ | | AE6 |
| $\overline{\text{CS1}}$ | | AD7 |

### Table 21. Pinout (continued)

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| CS2 | | AF5 |
| CS3 | | AC8 |
| CS4 | | AF6 |
| CS5 | | AD8 |
| CS6/BCTL1/SMI | | AC9 |
| CS7/TLBISYNC | | AB9 |
| BADDR27/IRQ1 | | AB8 |
| BADDR28/IRQ2 | | AC7 |
| ALE/IRQ4 | | AF4 |
| BCTL0 | | AF3 |
| PWE0/PSDDQM0/PBS0 | | AD6 |
| PWE1/PSDDQM1/PBS1 | | AE5 |
| PWE2/PSDDQM2/PBS2 | | AE3 |
| PWE3/PSDDQM3/PBS3 | | AF2 |
| PWE4/PSDDQM4/PBS4 | | AC6 |
| PWE5/PSDDQM5/PBS5 | | AC5 |
| PWE6/PSDDQM6/PBS6 | | AD4 |
| PWE7/PSDDQM7/PBS7 | | AB5 |
| PSDA10/PGPL0 | | AE2 |
| PSDWE/PGPL1 | | AD3 |
| POE/PSDRAS/PGPL2 | | AB4 |
| PSDCAS/PGPL3 | | AC3 |
| PGTA/PUPMWAIT/PGPL4 | | AD2 |
| PSDAMUX/PGPL5 | | AC2 |
| PCI_MODE[1] | | AD22 |
| PCI_CFG0 (PCI_HOST_EN) | | AC21 |
| PCI_CFG1 (PCI_ARB_EN) | | AE22 |
| PCI_CFG2 (DLL_ENABLE) | | AE23 |
| PCI_ PAR | | AF12 |
| PCI_FRAME | | AD15 |
| PCI_TRDY | | AF16 |

Table 21. Pinout (continued)

| Pin Name | | Ball |
|---|---|---|
| **MPC8272/MPC8248 and MPC8271/MPC8247** | **MPC8272/MPC8271 Only** | |
| $\overline{\text{PCI\_IRDY}}$ | | AF15 |
| $\overline{\text{PCI\_STOP}}$ | | AE15 |
| $\overline{\text{PCI\_DEVSEL}}$ | | AE14 |
| PCI_IDSEL | | AC17 |
| $\overline{\text{PCI\_PERR}}$ | | AD14 |
| $\overline{\text{PCI\_SERR}}$ | | AD13 |
| $\overline{\text{PCI\_REQ0}}$ | | AE20 |
| $\overline{\text{PCI\_REQ1}}$/CPCI_HS_ES | | AF14 |
| $\overline{\text{PCI\_GNT0}}$ | | AD20 |
| $\overline{\text{PCI\_GNT1}}$/CPCI_HS_LED | | AE13 |
| $\overline{\text{PCI\_GNT2/CPCI\_HS\_ENUM}}$ | | AF21 |
| $\overline{\text{PCI\_RST}}$ | | AF22 |
| $\overline{\text{PCI\_INTA}}$ | | AE21 |
| $\overline{\text{PCI\_REQ2}}$ | | AB14 |
| DLLOUT | | AC22 |
| PCI_AD0 | | AF7 |
| PCI_AD1 | | AE10 |
| PCI_AD2 | | AB10 |
| PCI_AD3 | | AD10 |
| PCI_AD4 | | AE9 |
| PCI_AD5 | | AF8 |
| PCI_AD6 | | AC10 |
| PCI_AD7 | | AE11 |
| PCI_AD8 | | AB11 |
| PCI_AD9 | | AF10 |
| PCI_AD10 | | AF9 |
| PCI_AD11 | | AB12 |
| PCI_AD12 | | AC12 |
| PCI_AD13 | | AD12 |
| PCI_AD14 | | AF11 |
| PCI_AD15 | | AB13 |

Table 21. Pinout (continued)

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| PA31/FCC1_MII_COL | FCC1_UT_TXENB | G22[3] |
| PB18/FCC2_MII_HDLC_RXD3 | | T25[3] |
| PB19/FCC2_MII_HDLC_RXD2 | | P22[3] |
| PB20/FCC2_MII_HDLC_RMII_RXD1 | | L25[3] |
| PB21/FCC2_MII_HDLC_RMII_RXD0/FCC2_TRAN_RXD | | J26[3] |
| PB22/FCC2_MII_HDLC_TXD0/FCC2_TRAN_TXD/ FCC2_RMII_TXD0 | | U23[3] |
| PB23/FCC2_MII_HDLC_TXD1/FCC2_RMII_TXD1 | | U26[3] |
| PB24/FCC2_MII_HDLC_TXD2/L1RSYNCB2 | | M24[3] |
| PB25/FCC2_MII_HDLC_TXD3/L1TSYNCB2 | | M23[3] |
| PB26/FCC2_MII_CRS/L1RXDB2 | | H24[3] |
| PB27/FCC2_MII_COL/L1TXDB2 | | E25[3] |
| PB28/FCC2_MII_RMII_RX_ER/FCC2_RTS/TXD1 | | D26[3] |
| PB29/FCC2_MII_RMII_TX_EN | | K21[3] |
| PB30/FCC2_MII_RX_DV/FCC2_RMII_CRS_DV | | D24[3] |
| PB31/FCC2_MII_TX_ER | | E23[3] |
| PC0/DREQ3/BRGO7/SMSYN1/L1CLKOA2 | | AF23[3] |
| PC1/BRGO6/L1RQA2 | | AD23[3] |
| PC4/SMRXD1/SI2_L1ST4/FCC2_CD | | AB22[3] |
| PC5/SMTXD1/SI2_L1ST3/FCC2_CTS | | AE24[3] |
| PC6/FCC1_CD/SI2_L1ST2 | FCC1_UT_RXADDR2 | AF24[3] |
| PC7/FCC1_CTS | FCC1_UT_TXADDR2 | AE26[3] |
| PC8/CD4/RTS1/SI2_L1ST2/CTS3 | | AC24[3] |
| PC9/CTS4/L1TSYNCA2 | | AA23[3] |
| PC10/CD3/USB_RN | | AB25[3] |
| PC11/CTS3/USB_RP/L1TXD3A2 | | V22[3] |
| PC12 | FCC1_UT_RXADDR1 | AA26[3] |
| PC13/BRGO5 | FCC1_UT_TXADDR1 | V23[3] |
| PC14/CD1 | FCC1_UT_RXADDR0 | W24[3] |
| PC15/CTS1 | FCC1_UT_TXADDR0 | U24[3] |
| PC16/CLK16 | | T23[3] |

### Table 21. Pinout (continued)

| Pin Name | | Ball |
|---|---|---|
| MPC8272/MPC8248 and MPC8271/MPC8247 | MPC8272/MPC8271 Only | |
| CLKIN2 | | C21 |
| No connect[4] | | D19[4], J3[4], AD24[5] |
| I/O power | | B4, F3, J2, N4, AD1, AD5, AE8, AC13, AD18, AB24, AB26, W23, R25, M25, F25, C25, C22, B17, B12, B8, E6, F6, H6, L5, L6, P6, T6, U6, V5, Y5, AA6, AA8, AA10, AA11, AA14, AA16, AA17, AB19, AB20, W21, U21, T21, P21, N21, M22, J22, H21, F21, F19, F17, E16, F14, E13, E12, F10, E10, E9 |
| Core Power | | F5, K5, M5, AA5, AB7, AA13, AA19, AA21, Y22, AC25, U22, R22, L21, H22, E22, E20, E15, F13, F11, F8, L3, V4, W3, AC11, AD11, AB15, U25, T24, J24, H25, F23, B19, D17, C17, D10, C10 |
| Ground | | E19, E2, K1, Y2, AE1, AE4, AD9, AC14, AE17, AC19, AE25, V24, P26, M26, G26, E26, B21, C12, C11, C8, A8, B18, A18, A2, B1, B2, A5, C5, D4, D6, G2, L4, P1, R1, R4, AC4, AE7, AC23, Y25, N24, J23, A23, D23, D20, E18, A13, A16, K10, K11, K12, K13, K14, K15, K16, K17, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, R10, R11,R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17 |

[1] Must be tied to ground.

[2] Should be tied to VDDH via a 2K Ω external pull-up resistor.

[3] The default configuration of the CPM pins (PA[8–31], PB[18–31], PC[0–1,4–29], PD[7–25, 29–31]) is input. To prevent excessive DC current, it is recommended either to pull unused pins to GND or VDDH, or to configure them as outputs.

[4] This pin is not connected. It should be left floating.

[5] Must be pulled down or left floating

# 10 Ordering Information

This figure provides an example of the Freescale part numbering nomenclature for the SoC. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

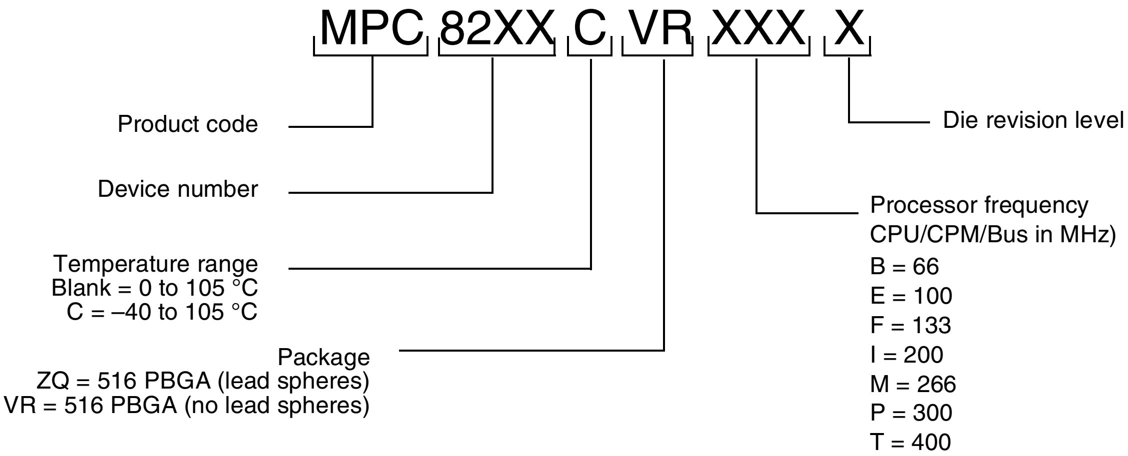


**Figure 15. Freescale Part Number Key**

# 11 Document Revision History

This table summarizes changes to this document.

**Table 23. Document Revision History**

| Revision | Date | Substantive Changes |
|---|---|---|
| 3 | 09/2011 | In Figure 15, “Freescale Part Number Key,” added speed decoding information below processor frequency information. |
| 2 | 12/2008 | • Modified Figure 5, “SCC/SMC/SPI/I2C External Clock Diagram,” and added second section of figure notes.<br>• In Table 12, modified “Data bus in pipeline mode” row and showed 66 MHz as “N/A.”<br>• In Section 10, “Ordering Information,” added “F = 133” to CPU/CPM/Bus Frequency.<br>• Added footnote concerning CPM_CLK/PCI_CLK ratio to column “PCI Division Factor” in Table 17, “Clock Configurations for PCI Host Mode (PCI_MODCK=0),” and Table 18, “Clock Configurations for PCI Host Mode (PCI_MODCK=1),.”<br>• Removed overbar from DLL_ENABLE in Table 21, “Pinout.” |
| 1.5 | 12/2006 | • Section 6, “AC Electrical Characteristics,” removed deratings statement and clarified AC timing descriptions. |
| 1.4 | 05/2006 | • Added row for 133 MHz configurations to Table 8. |
| 1.3 | 02/2006 | • Inserted Section 6.3, “JTAG Timings.” |

**Table 23. Document Revision History (continued)**

| Revision | Date | Substantive Changes |
|---|---|---|
| 1.2 | 09/2005 | • Added 133-MHz to the list of frequencies in the opening sentence of Section 6, “AC Electrical Characteristics”.<br>• Added 133 MHz columns to Table 9, Table 11, Table 12, and Table 13.<br>• Added footnote 2 to Table 13.<br>• Added the conditions note directly above Table 12. |
| 1.1 | 01/2005 | • Modification for correct display of assertion level (“$\overline{\text{overbar}}$”) for some signals |
| 1.0 | 12/2004 | • Section 1.1: Added 8:1 ratio to Internal CPM/bus clock multiplier values<br>• Section 2: removed voltage tracking note<br>• Table 3: Note 2 updated regarding VDD/VCCSYN relationship to VDDH during power-on reset<br>• Table 4: Updated VDD and VCCSYN to 1.425 V - 1.575 V<br>• Table 8: Note 2 updated to reflect VIH=2.5 for TCK, TRST, PORESET; request for external pull-up removed.<br>• Section 4.6: Updated description of layout practices<br>• Table 8: Note 3 added regarding IIC compatibility<br>• Table 8: Updated nominal and maximum power dissipation values<br>• Table 9: updated PCI impedance to 27Ω, updated 60x and MEMC values and added note to reflect configurable impedance<br>• Section 6: Added sentence providing derating factor<br>• Section 6.1: added Note: Rise/Fall Time on CPM Input Pins<br>• Table 9: updated values for following specs: sp36b, sp37a, sp38a, sp39a, sp38b, sp40, sp41, sp42, sp43, sp42a<br>• Table 11: updated values for following specs: sp16a, sp16b, sp18a, sp18b, sp20, sp21, sp22<br>• Section 6.2: added spread spectrum clocking note<br>• Section 6.2: added CLKIN jitter note<br>• Table 12: combined specs sp11 and sp11a<br>• Table 13: sp30 Data Bus minimum delay values changed to 0.8<br>• Section 7: unit of ns added to Tval notes<br>• Section 7: Updated all notes to reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz.<br>• Section 7, “Clock Configuration Modes”: Updated all table footnotes reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz.<br>• Table 21: correct superscript of footnote number after pin AD22<br>• Table 21: remove DONE3 from PC12<br>• Table 21: signals referring to TDMs C2 and D2 removed |

**Table 23. Document Revision History (continued)**

| Revision | Date | Substantive Changes |
|---|---|---|
| 0.2 | 12/2003 | • Table 1: New<br>• Table 2: New<br>• Table 4: Modification of VDD and VCCSYN to 1.45–1.60 V<br>• Table 8: Addition of note 2 regarding $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ (see $V_{IH}$ row of Table 8)<br>• Table 8 and Table 21: Addition of muxed signals<br>CPCI_HS_ES to $\overline{\text{PCI\_REQ1}}$ (AF14)<br>CPCI_HS_LED to $\overline{\text{PCI\_GNT1}}$ (AE13)<br>$\overline{\text{CPCI\_HS\_ENUM}}$ to $\overline{\text{PCI\_GNT2}}$ (AF21)<br>• Table 8 and Table 21: Modification of PCI signal names for consistency with PCI signal names on other PowerQUICC II devices:<br>PCI_CFG0 ($\overline{\text{PCI\_HOST\_EN}}$) (AC21)<br>PCI_CFG1 ($\overline{\text{PCI\_ARB\_EN}}$) (AE22)<br>PCI_CFG2 (DLL_ENABLE) (AE23)<br>PCI_PAR (AF12)<br>$\overline{\text{PCI\_FRAME}}$ (AD15)<br>$\overline{\text{PCI\_TRDY}}$(AF16)<br>$\overline{\text{PCI\_IRDY}}$ (AF15)<br>$\overline{\text{PCI\_STOP}}$ (AE15)<br>$\overline{\text{DEVSEL}}$ (AE14)<br>PCI_IDSEL (AC17)<br>$\overline{\text{PCI\_PERR}}$ (AD14)<br>$\overline{\text{PCI\_SERR}}$ (AD13)<br>$\overline{\text{PCI\_REQ0–2}}$ (AAE20, AF14, AB14)<br>$\overline{\text{PCI\_GNT0–2}}$ (AD20, AE13, AF21)<br>$\overline{\text{PCI\_RST}}$ (AF22)<br>$\overline{\text{PCI\_INTA}}$ (AE21)<br>$\overline{\text{PCI\_C0-3}}$ (AE12, AF13, AC15, AE18)<br>PCI_AD0-31<br>• Table 8 and Table 21: Corrected assertion level (added “$\overline{\ \ }$“) $\overline{\text{PCI\_HOST\_EN}}$ (AC21) and $\overline{\text{PCI\_ARB\_EN}}$ (AE22)<br>• Table 7: Addition of $R_{\theta JT}$ and note 4<br>• Sections 4.1–4.5 and 4.7 on thermal characteristics: New<br>• Section 7, “Clock Configuration Modes”: Modification to first paragraph. Note that PCI_MODCK is a bit in the Hard Reset Configuration Word. It is not an input signal as it is in the MPC8280 Family and MPC8260 Family.<br>• Addition of “Note: Temperature Reflow for the VR Package" on page 56<br>• Table 21: Addition of note 2 to $\overline{\text{TRST}}$ (E21) and $\overline{\text{PORESET}}$ (C24)<br>• Table 21: Removal of Thermal0 (D19) and Thermal1(J3). These pins are now “No connects.” Note 4 unchanged.<br>• Table 21: Removal of Spare0 (AD24). This pin is now a “No connect.” Note 5 unchanged.<br>• Table 21: Addition of $\overline{\text{PCI\_MODE}}$ (AD22). This pin was previously listed as “Ground.” Addition of note 1. |
| 0.1 | 9/2003 | • Addition of the MPC8271 and the MPC8247 (these devices do not have a security engine)<br>• Table 8: Addition of note 2 to $V_{IH}$<br>• Table 8: Changed $I_{OL}$ for 60x signals to 6.0 mA<br>• Modification of note 1 for Table 17, Table 18, Table 19, and Table 20<br>• Table 21: Addition of ball AD9 to GND. In rev 0 of this document, AD8 was listed as assigned to both $\overline{\text{CS5}}$ and GND. AD8 is only assigned to $\overline{\text{CS5}}$.<br>• Table 21: Addition of note 4 to Thermal0 (D19) and Thermal1(J3)<br>• Addition of ZQ package code to Figure 15 |
| 0 | 5/2003 | NDA release |