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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G2_LE
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	300MHz
Co-Processors/DSP	Communications; RISC CPM, Security; SEC
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8272zqpiea

- Integrated security engine (SEC) (MPC8272 and MPC8248 only)
 - Supports DES, 3DES, MD-5, SHA-1, AES, PKEU, RNG and RC-4 encryption algorithms in hardware
- Communications processor module (CPM)
 - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications peripherals
 - Interfaces to G2_LE core through on-chip dual-port RAM and DMA controller. (Dual-port RAM size is 16 KB plus 4 KB dedicated instruction RAM.)
 - Microcode tracing capabilities
 - Eight CPM trap registers
- Universal serial bus (USB) controller
 - Supports USB 2.0 full/low rate compatible
 - USB host mode
 - Supports control, bulk, interrupt, and isochronous data transfers
 - CRC16 generation and checking
 - NRZI encoding/decoding with bit stuffing
 - Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
 - Flexible data buffers with multiple buffers per frame
 - Supports local loopback mode for diagnostics (12 Mbps only)
 - Supports USB slave mode
 - Four independent endpoints support control, bulk, interrupt, and isochronous data transfers
 - CRC16 generation and checking
 - CRC5 checking
 - NRZI encoding/decoding with bit stuffing
 - 12- or 1.5-Mbps data rate
 - Flexible data buffers with multiple buffers per frame
 - Automatic retransmission upon transmit error
 - Serial DMA channels for receive and transmit on all serial channels
 - Parallel I/O registers with open-drain and interrupt capability
 - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
 - Two fast communication controllers (FCCs) supporting the following protocols:
 - 10-/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through media independent interface (MII)
 - Transparent
 - HDLC—up to T3 rates (clear channel)

Table 5. DC Electrical Characteristics¹ (continued)

Characteristic	Symbol	Min	Max	Unit
$I_{OL} = 6.0\text{mA}$ \overline{BR} $\overline{BG}/\overline{IRQ6}$ $\overline{ABB}/\overline{IRQ2}$ \overline{TS} $A[0-31]$ $TT[0-4]$ \overline{TBST} $TSIZE[0-3]$ \overline{AACK} \overline{ARTRY} $\overline{DBG}/\overline{IRQ7}$ $\overline{DBB}/\overline{IRQ3}$ $D[0-63]$ $\overline{IRQ3}/\overline{CKSTP_OUT}/\overline{EXT_BR3}$ $\overline{IRQ4}/\overline{CORE_SRESET}/\overline{EXT_BG3}$ $\overline{IRQ5}/\overline{TBEN}/\overline{EXT_DBG3}/\overline{CINT}$ \overline{PSDVAL} \overline{TA} \overline{TEA} $\overline{GBL}/\overline{IRQ1}$ $\overline{CI}/\overline{BADDR29}/\overline{IRQ2}$ $\overline{WT}/\overline{BADDR30}/\overline{IRQ3}$ $\overline{BADDR31}/\overline{IRQ5}/\overline{CINT}$ $\overline{CPU_BR}/\overline{INT_OUT}$ $\overline{IRQ0}/\overline{NMI_OUT}$ $\overline{PORESET}/\overline{PCI_RST}$ \overline{HRESET} \overline{SRESET} $\overline{RSTCONF}$	V_{OL}	—	0.4	V

Table 6.

Characteristic	Symbol	Min	Max	Unit
$I_{OL} = 5.3\text{mA}$ $\overline{CS}[0-9]$ $\overline{CS}(10)/\overline{BCTL1}$ $\overline{CS}(11)/\overline{AP}(0)$ $\overline{BADDR}[27-28]$ \overline{ALE} $\overline{BCTL0}$ $\overline{PWE}[0-7]/\overline{PSDDQM}[0-7]/\overline{PBS}[0-7]$ $\overline{PSDA10}/\overline{PGPL0}$ $\overline{PSDWE}/\overline{PGPL1}$ $\overline{POE}/\overline{PSDRAS}/\overline{PGPL2}$ $\overline{PSDCAS}/\overline{PGPL3}$ $\overline{PGTA}/\overline{PUPMWAIT}/\overline{PGPL4}/\overline{PPBS}$ $\overline{PSDAMUX}/\overline{PGPL5}$ $\overline{LWE}[0-3]/\overline{LSDDQM}[0-3]/\overline{LBS}[0-3]/\overline{PCI_CFG}[0-3]$ $\overline{LSDA10}/\overline{LGPL0}/\overline{PCI_MODCKH0}$ $\overline{LSDWE}/\overline{LGPL1}/\overline{PCI_MODCKH1}$ $\overline{LOE}/\overline{LSDRAS}/\overline{LGPL2}/\overline{PCI_MODCKH2}$ $\overline{LSDCAS}/\overline{LGPL3}/\overline{PCI_MODCKH3}$ $\overline{LGTA}/\overline{LUPMWAIT}/\overline{LGPL4}/\overline{LPBS}$ $\overline{LSDAMUX}/\overline{LGPL5}/\overline{PCI_MODCK}$ \overline{LWR} $\overline{MODCK}[1-3]/\overline{AP}[1-3]/\overline{TC}[0-2]/\overline{BNKSEL}[0-2]$ $I_{OL} = 3.2\text{mA}$ $\overline{L_A14}/\overline{PAR}$ $\overline{L_A15}/\overline{FRAME}/\overline{SMI}$ $\overline{L_A16}/\overline{TRDY}$ $\overline{L_A17}/\overline{IRDY}/\overline{CKSTP_OUT}$ $\overline{L_A18}/\overline{STOP}$ $\overline{L_A19}/\overline{DEVSEL}$ $\overline{L_A20}/\overline{IDSEL}$ $\overline{L_A21}/\overline{PERR}$ $\overline{L_A22}/\overline{SERR}$ $\overline{L_A23}/\overline{REQ0}$ $\overline{L_A24}/\overline{REQ1}/\overline{HSEJSW}$ $\overline{L_A25}/\overline{GNT0}$ $\overline{L_A26}/\overline{GNT1}/\overline{HSLED}$ $\overline{L_A27}/\overline{GNT2}/\overline{HSENUM}$ $\overline{L_A28}/\overline{RST}/\overline{CORE_SRESET}$ $\overline{L_A29}/\overline{INTAL_A30}/\overline{REQ2}$ $\overline{L_A31}$ $\overline{LCL_D}[0-31]/\overline{AD}[0-31]$ $\overline{LCL_DP}[03]/\overline{C}/\overline{BE}[0-3]$ $\overline{PA}[0-31]$ $\overline{PB}[4-31]$ $\overline{PC}[0-31]$ $\overline{PD}[4-31]$ \overline{TDO} \overline{QREQ}	V_{OL}	—	0.4	V

¹ TCK, TRST and PORESET have min $V_{IH} = 2.5\text{V}$.

² The leakage current is measured for nominal VDDH, VCCSYN, and VDD.

³ V_{IL} for IIC interface does not match IIC standard, but does meet IIC standard for V_{OL} and should not cause any compatibility issue.

4.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

4.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case thermal resistance covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. It has been observed that the thermal performance of most plastic packages, especially PBGA packages, is strongly dependent on the board temperature.

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W)

T_B = board temperature (°C)

P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and by attaching the thermal balls to the ground plane.

4.7 References

Semiconductor Equipment and Materials International(415) 964-5111
805 East Middlefield Rd.
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) Specifications800-854-7179 or
(Available from Global Engineering Documents)303-397-7956

JEDEC Specifications <http://www.jedec.org>

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

5 Power Dissipation

This table provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink. For a complete list of possible clock configurations, see [Section 7, “Clock Configuration Modes.”](#)

Table 8. Estimated Power Dissipation for Various Configurations¹

Bus (MHz)	CPM Multiplication Factor	CPM (MHz)	CPU Multiplication Factor	CPU (MHz)	$P_{INT}(W)^{2,3}$	
					V _{ddl} 1.5 Volts	
					Nominal	Maximum
66.67	3	200	4	266	1	1.2
100	2	200	3	300	1.1	1.3
100	2	200	4	400	1.3	1.5
133	2	267	3	400	1.5	1.8

¹ Test temperature = 105° C

² $P_{INT} = I_{DD} \times V_{DD}$ Watts

³ Values do not include I/O. Add the following estimates for active I/O based on the following bus speeds:

66.7 MHz = 0.35 W (nominal), 0.4 W (maximum)

83.3 MHz = 0.4 W (nominal), 0.5 W (maximum)

100 MHz = 0.5 W (nominal), 0.6 W (maximum)

133 MHz = 0.7 W (nominal), 0.8 W (maximum)

6 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for 66.67/83.33/100/133 MHz devices. Note that AC timings are based on a 50-pf load for MAX Delay and 10-pf load for MIN delay. Typical output buffer impedances are shown in this table.

Table 9. Output Buffer Impedances¹

Output Buffers	Typical Impedance (Ω)
60x bus	45 or 27 ²
Memory controller	45 or 27 ²
Parallel I/O	45
PCI	27

¹ These are typical values at 65° C. Impedance may vary by $\pm 25\%$ with process and temperature.

² Impedance value is selected through SIUMCR[20,21]. See the SoC reference manual.

6.1 CPM AC Characteristics

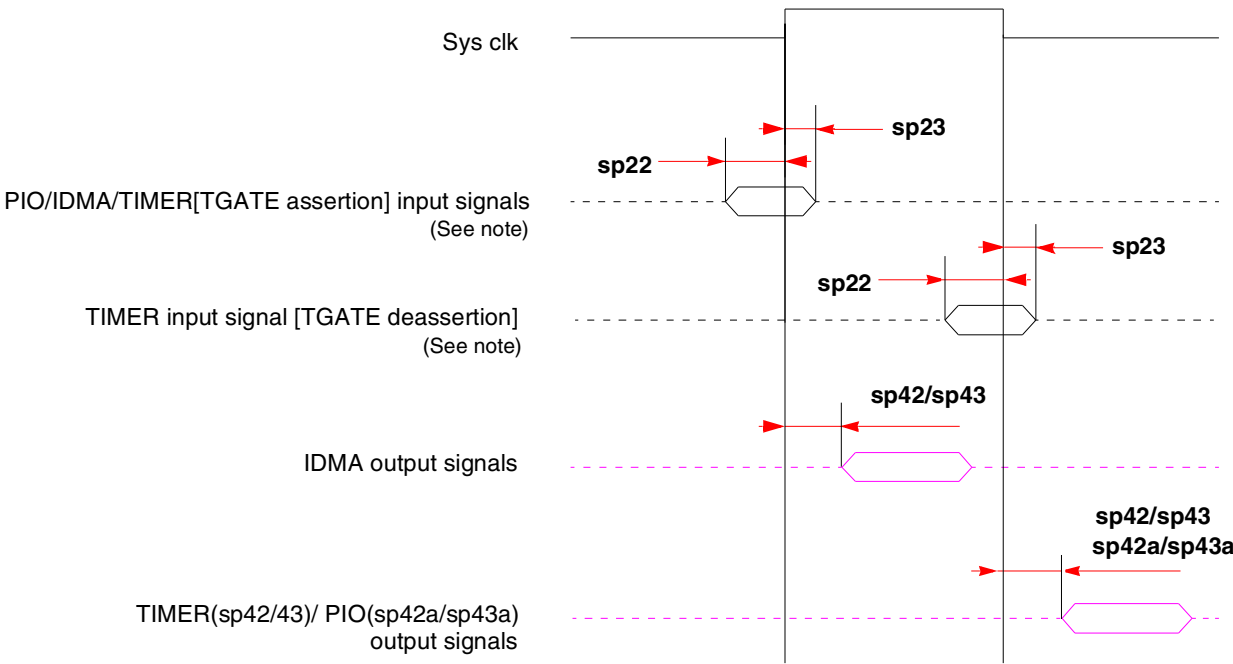
This table lists CPM output characteristics.

Table 10. AC Characteristics for CPM Outputs¹

Spec Number		Characteristic	Value (ns)							
Max	Min		Maximum Delay				Minimum Delay			
			66 MHz	83 MHz	100 MHz	133 MHz	66 MHz	83 MHz	100 MHz	133 MHz
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	5.5	5.5	5.5	0.5	0.5	0.5	0.5
sp36b	sp37b	FCC outputs—external clock (NMSI)	8	8	8	8	2	2	2	2
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	10	10	10	10	0	0	0	0
sp38b	sp39b	SCC/SMC/SPI/I2C outputs—external clock (NMSI)	8	8	8	8	2	2	2	2
sp40	sp41	TDM outputs/SI	11	11	11	11	2.5	2.5	2.5	2.5
sp42	sp43	TIMER/IDMA outputs	11	11	11	11	0.5	0.5	0.5	0.5
sp42a	sp43a	PIO outputs	11	11	11	11	0.5	0.5	0.5	0.5

¹ Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

This figure shows PIO and timer signals.



Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

Figure 8. PIO and Timer Signal Diagram

6.2 SIU AC Characteristics

This table lists SIU input characteristics.

NOTE: CLKIN Jitter and Duty Cycle

The CLKIN input to the SoC should not exceed ± 150 psec of jitter (peak-to-peak). This represents total input jitter—the combination of short term (peak-to-peak) and long term (cumulative). The duty cycle of CLKIN should not exceed the ratio of 40:60.

NOTE: Spread Spectrum Clocking

Spread spectrum clocking is allowed with 1% input frequency down-spread at maximum 60 KHz modulation rate regardless of input frequency.

NOTE: PCI AC Timing

The SoC meets the timing requirements of *PCI Specification Revision 2.2*. See [Section 7, “Clock Configuration Modes,”](#) and “Note: Tval (Output Hold)” to determine if a specific clock configuration is compliant.

NOTE

Activating data pipelining (setting BRx[DR] in the memory controller) improves the AC timing.

This figure shows the interaction of several bus signals.

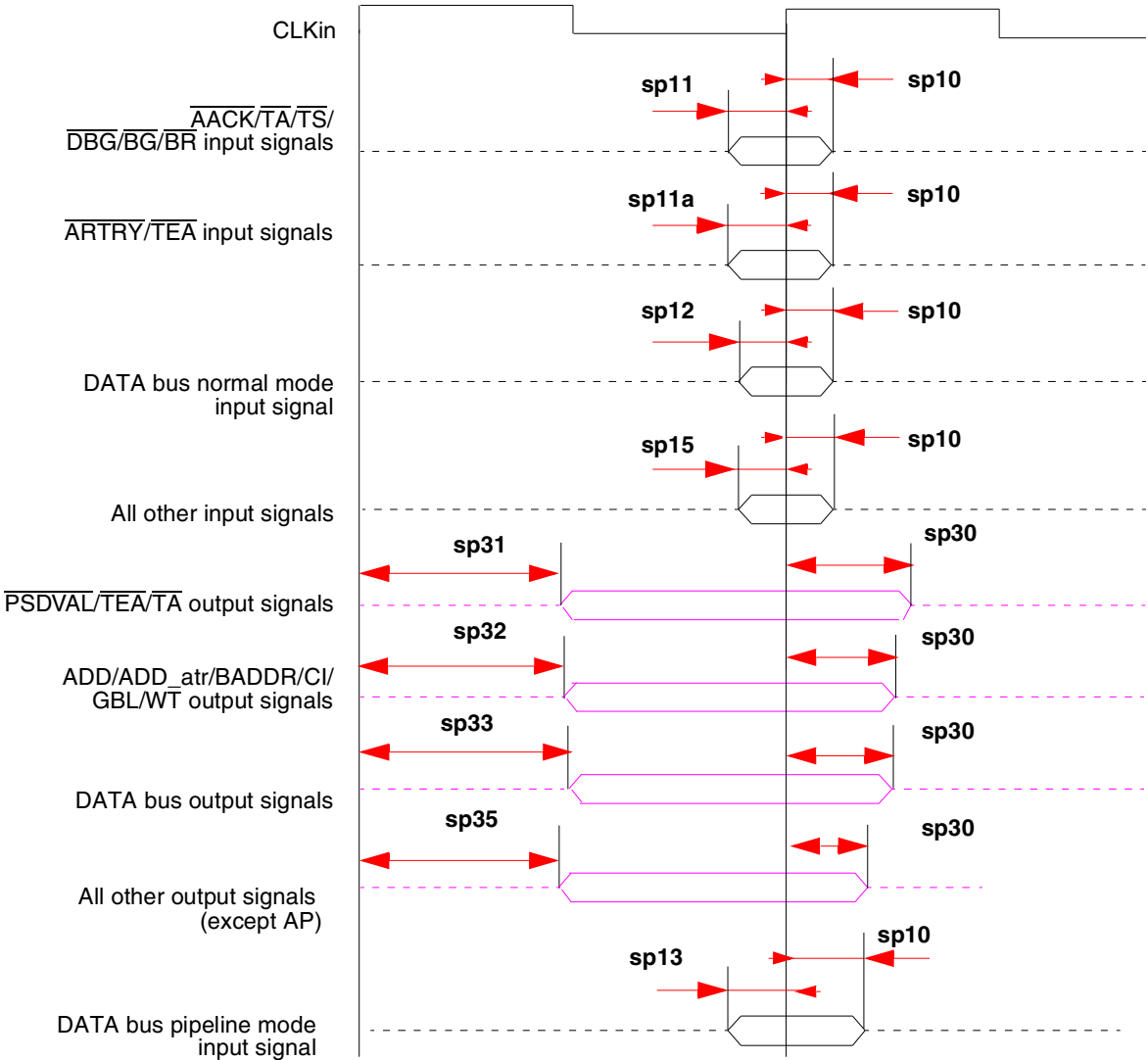


Figure 9. Bus Signals

7 Clock Configuration Modes

As shown in this table, the clocking mode is set according to two sources:

- PCI_CFG[0]— An input signal. Also defined as “PCI_HOST_EN.” See Chapter 6, “External Signals,” and Chapter 9, “PCI Bridge,” in the SoC reference manual.
- PCI_MODCK—Bit 27 in the Hard Reset Configuration Word. See Chapter 5, “Reset,” in the SoC reference manual.

Table 16. SoC Clocking Modes

Pins		Clocking Mode	PCI Clock Frequency Range (MHz)	Reference
PCI_CFG[0] ¹	PCI_MODCK ²			
0	0	PCI host	50–66	Table 17
0	1		25–50	Table 18
1	0	PCI agent	50–66	Table 19
1	1		25–50	Table 20

¹ PCI_HOST_EN

² Determines PCI clock frequency range.

Within each mode, the configuration of bus, core, PCI, and CPM frequencies is determined by seven bits during the power-on reset—three hardware configuration pins (MODCK[1–3]) and four bits from hardware configuration word[28–31] (MODCK_H). Both the PLLs and the dividers are set according to the selected clock operation mode as described in the following sections.

NOTE

Clock configurations change only after $\overline{\text{PORESET}}$ is asserted.

NOTE: Tval (Output Hold)

The minimum Tval = 2 ns when PCI_MODCK = 1, and the minimum Tval = 1 ns when PCI_MODCK = 0. Therefore, designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

7.1 PCI Host Mode

These tables show configurations for PCI host mode. The frequency values listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. Note that in PCI host mode the input clock is the bus clock.

Table 18. Clock Configurations for PCI Host Mode (PCI_MODCK=1)^{1,2} (continued)

Mode ³	Bus Clock (MHz)		CPM Multiplication Factor ⁴	CPM Clock (MHz)		CPU Multiplication Factor ⁵	CPU Clock (MHz)		PCI Division Factor ⁶	PCI Clock (MHz)	
	Low	High		Low	High		Low	High		Low	High
0100_001	25.0	50.0	6	150.0	300.0	6	150.0	300.0	6	25.0	50.0
0100_010	25.0	50.0	6	150.0	300.0	7	175.0	350.0	6	25.0	50.0
0100_011	25.0	50.0	6	150.0	300.0	8	200.0	400.0	6	25.0	50.0
0101_000	60.0	100.0	2	120.0	200.0	2.5	150.0	250.0	4	30.0	50.0
0101_001	50.0	100.0	2	100.0	200.0	3	150.0	300.0	4	25.0	50.0
0101_010	50.0	100.0	2	100.0	200.0	3.5	175.0	350.0	4	25.0	50.0
0101_011	50.0	100.0	2	100.0	200.0	4	200.0	400.0	4	25.0	50.0
0101_100	50.0	100.0	2	100.0	200.0	4.5	225.0	450.0	4	25.0	50.0
0101_101	42.9	83.3	3	128.6	250.0	3.5	150.0	291.7	5	25.7	50.0
0101_110	41.7	83.3	3	125.0	250.0	4	166.7	333.3	5	25.0	50.0
0101_111	41.7	83.3	3	125.0	250.0	4.5	187.5	375.0	5	25.0	50.0
0110_000	60.0	120.0	2.5	150.0	300.0	2.5	150.0	300.0	6	25.0	50.0
0110_001	60.0	120.0	2.5	150.0	300.0	3	180.0	360.0	6	25.0	50.0
0110_010	60.0	120.0	2.5	150.0	300.0	3.5	210.0	420.0	6	25.0	50.0
0110_011	60.0	120.0	2.5	150.0	300.0	4	240.0	480.0	6	25.0	50.0
0110_100	60.0	120.0	2.5	150.0	300.0	4.5	270.0	540.0	6	25.0	50.0
0110_101	60.0	120.0	2.5	150.0	300.0	5	300.0	600.0	6	25.0	50.0
0110_110	60.0	120.0	2.5	150.0	300.0	6	360.0	720.0	6	25.0	50.0
0111_000	Reserved										
0111_001	50.0	100.0	3	150.0	300.0	3	150.0	300.0	6	25.0	50.0
0111_010	50.0	100.0	3	150.0	300.0	3.5	175.0	350.0	6	25.0	50.0
0111_011	50.0	100.0	3	150.0	300.0	4	200.0	400.0	6	25.0	50.0
0111_100	50.0	100.0	3	150.0	300.0	4.5	225.0	450.0	6	25.0	50.0
1000_000	Reserved										
1000_001	66.7	133.3	3	200.0	400.0	3	200.0	400.0	8	25.0	50.0

Table 19. Clock Configurations for PCI Agent Mode (PCI_MODCK=0)^{1,2} (continued)

Mode ³	PCI Clock (MHz)		CPM Multiplication Factor ⁴	CPM Clock (MHz)		CPU Multiplication Factor ⁵	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
	Low	High		Low	High		Low	High		Low	High
1100_101	50.0	66.7	6	300.0	400.0	4	400.0	533.3	3	100.0	133.3
1100_110	50.0	66.7	6	300.0	400.0	4.5	450.0	599.9	3	100.0	133.3
1100_111	50.0	66.7	6	300.0	400.0	5	500.0	666.6	3	100.0	133.3
1101_000	50.0	66.7	6	300.0	400.0	5.5	550.0	733.3	3	100.0	133.3
1101_001	50.0	66.7	6	300.0	400.0	3.5	420.0	559.9	2.5	120.0	160.0
1101_010	50.0	66.7	6	300.0	400.0	4	480.0	639.9	2.5	120.0	160.0
1101_011	50.0	66.7	6	300.0	400.0	4.5	540.0	719.9	2.5	120.0	160.0
1101_100	50.0	66.7	6	300.0	400.0	5	600.0	799.9	2.5	120.0	160.0
1110_000	50.0	66.7	5	250.0	333.3	2.5	312.5	416.6	2	125.0	166.7
1110_001	50.0	66.7	5	250.0	333.3	3	375.0	500.0	2	125.0	166.7
1110_010	50.0	66.7	5	250.0	333.3	3.5	437.5	583.3	2	125.0	166.7
1110_011	50.0	66.7	5	250.0	333.3	4	500.0	666.6	2	125.0	166.7
1110_100	50.0	66.7	5	250.0	333.3	4	333.3	444.4	3	83.3	111.1
1110_101	50.0	66.7	5	250.0	333.3	4.5	375.0	500.0	3	83.3	111.1
1110_110	50.0	66.7	5	250.0	333.3	5	416.7	555.5	3	83.3	111.1
1110_111	50.0	66.7	5	250.0	333.3	5.5	458.3	611.1	3	83.3	111.1
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

¹ The “low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency in a table entry guarantees only the required minimum CPU operating frequency. The “high” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. The minimum CPU frequency is 150 MHz for commercial temperature devices and 175 MHz for extended temperature devices. The minimum CPM frequency is 120 MHz.

² PCI_MODCK determines the PCI clock frequency range. See [Table 20](#) for lower range configurations.

³ MODCK_H = hard reset configuration word [28–31] (see Section 5.4 in the SoC reference manual). MODCK[1-3] = three hardware configuration pins.

⁴ CPM multiplication factor = CPM clock/bus clock

⁵ CPU multiplication factor = Core PLL multiplication factor

Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)^{1,2}

Mode ³	PCI Clock (MHz)		CPM Multiplication Factor ⁴	CPM Clock (MHz)		CPU Multiplication Factor ⁵	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H- MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
Default Modes (MODCK_H=0000)											
0000_000	30.0	50.0	4	120.0	200.0	2.5	150.0	250.0	2	60.0	100.0
0000_001	25.0	50.0	4	100.0	200.0	3	150.0	300.0	2	50.0	100.0
0000_010	25.0	50.0	6	150.0	300.0	3	150.0	300.0	3	50.0	100.0
0000_011	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0
0000_100	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
0000_101	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
0000_110	25.0	50.0	8	200.0	400.0	3.5	233.3	466.7	3	66.7	133.3
0000_111	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
Full Configuration Modes											
0001_001	30.0	50.0	4	120.0	200.0	5	150.0	250.0	4	30.0	50.0
0001_010	25.0	50.0	4	100.0	200.0	6	150.0	300.0	4	25.0	50.0
0001_011	25.0	50.0	4	100.0	200.0	7	175.0	350.0	4	25.0	50.0
0001_100	25.0	50.0	4	100.0	200.0	8	200.0	400.0	4	25.0	50.0
0010_001	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
0010_010	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
0010_011	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
0010_100	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
0011_000	Reserved										
0011_001	37.5	50.0	4	150.0	200.0	3	150.0	200.0	3	50.0	66.7
0011_010	32.1	50.0	4	128.6	200.0	3.5	150.0	233.3	3	42.9	66.7
0011_011	28.1	50.0	4	112.5	200.0	4	150.0	266.7	3	37.5	66.7
0011_100	25.0	50.0	4	100.0	200.0	4.5	150.0	300.0	3	33.3	66.7
0100_000	Reserved										
0100_001	25.0	50.0	6	150.0	300.0	3	150.0	300.0	3	50.0	100.0
0100_010	25.0	50.0	6	150.0	300.0	3.5	175.0	350.0	3	50.0	100.0
0100_011	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0

Table 20. Clock Configurations for PCI Agent Mode (PCI_MODCK=1)^{1,2} (continued)

Mode ³	PCI Clock (MHz)		CPM Multiplication Factor ⁴	CPM Clock (MHz)		CPU Multiplication Factor ⁵	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	Low	High		Low	High		Low	High		Low	High
1001_010	Reserved										
1001_011	25.0	50.0	8	200.0	400.0	4	200.0	400.0	4	50.0	100.0
1001_100	25.0	50.0	8	200.0	400.0	4.5	225.0	450.0	4	50.0	100.0
1010_000	Reserved										
1010_001	25.0	50.0	8	200.0	400.0	3	200.0	400.0	3	66.7	133.3
1010_010	25.0	50.0	8	200.0	400.0	3.5	233.3	466.7	3	66.7	133.3
1010_011	25.0	50.0	8	200.0	400.0	4	266.7	533.3	3	66.7	133.3
1010_100	25.0	50.0	8	200.0	400.0	4.5	300.0	600.0	3	66.7	133.3
1011_000	Reserved										
1011_001	25.0	50.0	8	200.0	400.0	2.5	200.0	400.0	2.5	80.0	160.0
1011_010	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
1011_011	25.0	50.0	8	200.0	400.0	3.5	280.0	560.0	2.5	80.0	160.0
1011_100	25.0	50.0	8	200.0	400.0	4	320.0	640.0	2.5	80.0	160.0
1011_101	25.0	50.0	8	200.0	400.0	2.5	250.0	500.0	2	100.0	200.0
1011_110	25.0	50.0	8	200.0	400.0	3	300.0	600.0	2	100.0	200.0
1011_111	25.0	50.0	8	200.0	400.0	3.5	350.0	700.0	2	100.0	200.0
1100_101	25.0	50.0	6	150.0	300.0	4	200.0	400.0	3	50.0	100.0
1100_110	25.0	50.0	6	150.0	300.0	4.5	225.0	450.0	3	50.0	100.0
1100_111	25.0	50.0	6	150.0	300.0	5	250.0	500.0	3	50.0	100.0
1101_000	25.0	50.0	6	150.0	300.0	5.5	275.0	550.0	3	50.0	100.0
1101_001	25.0	50.0	6	150.0	300.0	3.5	210.0	420.0	2.5	60.0	120.0
1101_010	25.0	50.0	6	150.0	300.0	4	240.0	480.0	2.5	60.0	120.0
1101_011	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
1101_100	25.0	50.0	6	150.0	300.0	5	300.0	600.0	2.5	60.0	120.0

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
D15		G3
D16		AB3
D17		Y1
D18		T4
D19		T3
D20		P2
D21		M1
D22		J1
D23		G4
D24		AB2
D25		W4
D26		V2
D27		T1
D28		N5
D29		L1
D30		H1
D31		G5
D32		W5
D33		W2
D34		T5
D35		T2
D36		N1
D37		K3
D38		H2
D39		F1
D40		AA2
D41		W1
D42		U3
D43		R2
D44		N2
D45		L2

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
$\overline{CS2}$		AF5
$\overline{CS3}$		AC8
$\overline{CS4}$		AF6
$\overline{CS5}$		AD8
$\overline{CS6/BCTL1/SMI}$		AC9
$\overline{CS7/TLBISYNC}$		AB9
BADDR27/ $\overline{IRQ1}$		AB8
BADDR28/ $\overline{IRQ2}$		AC7
ALE/ $\overline{IRQ4}$		AF4
$\overline{BCTL0}$		AF3
$\overline{PWE0/PSDDQM0/PBS0}$		AD6
$\overline{PWE1/PSDDQM1/PBS1}$		AE5
$\overline{PWE2/PSDDQM2/PBS2}$		AE3
$\overline{PWE3/PSDDQM3/PBS3}$		AF2
$\overline{PWE4/PSDDQM4/PBS4}$		AC6
$\overline{PWE5/PSDDQM5/PBS5}$		AC5
$\overline{PWE6/PSDDQM6/PBS6}$		AD4
$\overline{PWE7/PSDDQM7/PBS7}$		AB5
PSDA10/PGPL0		AE2
$\overline{PSDWE/PGPL1}$		AD3
$\overline{POE/PSDRAS/PGPL2}$		AB4
$\overline{PSDCAS/PGPL3}$		AC3
$\overline{PGTA/PUPMWAIT/PGPL4}$		AD2
PSDAMUX/PGPL5		AC2
PCI_MODE ¹		AD22
PCI_CFG0 ($\overline{PCI_HOST_EN}$)		AC21
PCI_CFG1 ($\overline{PCI_ARB_EN}$)		AE22
PCI_CFG2 (DLL_ENABLE)		AE23
PCI_PAR		AF12
$\overline{PCI_FRAME}$		AD15
$\overline{PCI_TRDY}$		AF16

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
MODCK1/ $\overline{\text{RSRV}}$ /TC0/BNKSEL0		A20
MODCK2/CSE0/TC1/BNKSEL1		C20
MODCK3/CSE1/TC2/BNKSEL2		A21
CLKIN1		D21
PA8/SMRXD2		AF25 ³
PA9/SMTXD2		AA22 ³
PA10/MSNUM5	FCC1_UT_RXD0	AB23 ³
PA11/MSNUM4	FCC1_UT_RXD1	AD26 ³
PA12/MSNUM3	FCC1_UT_RXD2	AD25 ³
PA13/MSNUM2	FCC1_UT_RXD3	AA24 ³
PA14/FCC1_MII_HDLC_RXD3	FCC1_UT_RXD4	W22 ³
PA15/FCC1_MII_HDLC_RXD2	FCC1_UT_RXD5	Y24 ³
PA16/FCC1_MII_HDLC_RXD1	FCC1_UT_RXD6	T22 ³
PA17/FCC1_MII_HDLC_RXD0/ FCC1_MII_TRAN_RXD/FCC1_RMII_RX D0	FCC1_UT_RXD7	W26 ³
PA18/FCC1_MII_HDLC_TXD0/FCC1_MII _TRAN_TXD/ FCC1_RMII_TXD0	FCC1_UT_TXD7	V26 ³
PA19/FCC1_MII_HDLC_TXD1/FCC1_RM II_TXD1	FCC1_UT_TXD6	R23 ³
PA20/FCC1_MII_HDLC_TXD2	FCC1_UT_TXD5	P25 ³
PA21/FCC1_MII_HDLC_TXD3	FCC1_UT_TXD4	N22 ³
PA22	FCC1_UT_TXD3	N26 ³
PA23	FCC1_UT_TXD2	N23 ³
PA24/MSNUM1	FCC1_UT_TXD1	H26 ³
PA25/MSNUM0	FCC1_UT_TXD0	G25 ³
PA26/FCC1_MII_RMII_RX_ER	FCC1_UT_RXCLAV	L22 ³
PA27/FCC1_MII_RX_DV/FCC1_RMII_CR S_DV	FCC1_UT_RXSOC	G24 ³
PA28/FCC1_MII_RMII_TX_EN	FCC1_UT_RXENB	G23 ³
PA29/FCC1_MII_TX_ER	$\overline{\text{FCC1_UT_TXSOC}}$	B26 ³
PA30/FCC1_MII_CR $\overline{\text{S}}$ /FCC1_RT $\overline{\text{S}}$	FCC1_UT_TXCLAV	A25 ³

Table 21. Pinout (continued)

Pin Name		Ball
MPC8272/MPC8248 and MPC8271/MPC8247	MPC8272/MPC8271 Only	
PC17/CLK15/BRGO8/ $\overline{\text{DONE2}}$		T26 ³
PC18/CLK14/ $\overline{\text{TGATE2}}$		R26 ³
PC19/CLK13/BRGO7/ $\overline{\text{TGATE1}}$		P24 ³
PC20/CLK12/ $\overline{\text{USB0E}}$		L26 ³
PC21/CLK11/BRGO6/CP_INT		L24 ³
PC22/CLK10/ $\overline{\text{DONE3}}$	FCC1_UT_TXPRTY	L23 ³
PC23/CLK9/BRGO5/ $\overline{\text{DACK3}}/\overline{\text{CD1}}$		K24 ³
PC24/CLK8/TIN3/ $\overline{\text{TOUT4}}$ /DREQ2/BRGO1		K23 ³
PC25/CLK7/BRGO4/ $\overline{\text{DACK2}}$ /SPISEL		F26 ³
PC26/CLK6/ $\overline{\text{TOUT3}}$ /TMCLK		H23 ³
PC27/CLK5/BRGO3/ $\overline{\text{TOUT1}}$	FCC1_UT_RXPRTY	K22 ³
PC28/CLK4/TIN1/ $\overline{\text{TOUT2}}$ /SPICLK		D25 ³
PC29/CLK3/TIN2/BRGO2/ $\overline{\text{CTS1}}$		F24 ³
PD7/SMSYN2	FCC1_UT_TXADDR3	AB21 ³
PD14/I2CSCL		AC26 ³
PD15/I2CSDA		Y23 ³
PD16/SPIMISO	FCC1_UT_TXPRTY	AA25 ³
PD17/BRGO2/SPIMOSI	FCC1_UT_RXPRTY	Y26 ³
PD18/SPICLK	FCC1_UT_RXADDR4	W25 ³
PD19/SPISEL/BRGO1	FCC1_UT_TXADDR4	V25 ³
PD20/ $\overline{\text{RTS4}}$ /L1RSYNCA2		R24 ³
PD21/TXD4/L1RXD0A2		P23 ³
PD22/RXD4/L1TXD0A2		N25 ³
PD23/ $\overline{\text{RTS3}}$ /USB_TP		K26 ³
PD24/TXD3/USB_TN		K25 ³
PD25/RXD3/USB_RXD		J25 ³
PD29/ $\overline{\text{RTS1}}$	FCC1_UT_RXADDR3	C26 ³
PD30/TXD1		E24 ³
PD31/RXD1		B25 ³
VCCSYN		C18
VCCSYN1		K6

9.2 Mechanical Dimensions

This figure provides the mechanical dimensions and bottom surface nomenclature of the 516 PBGA package.

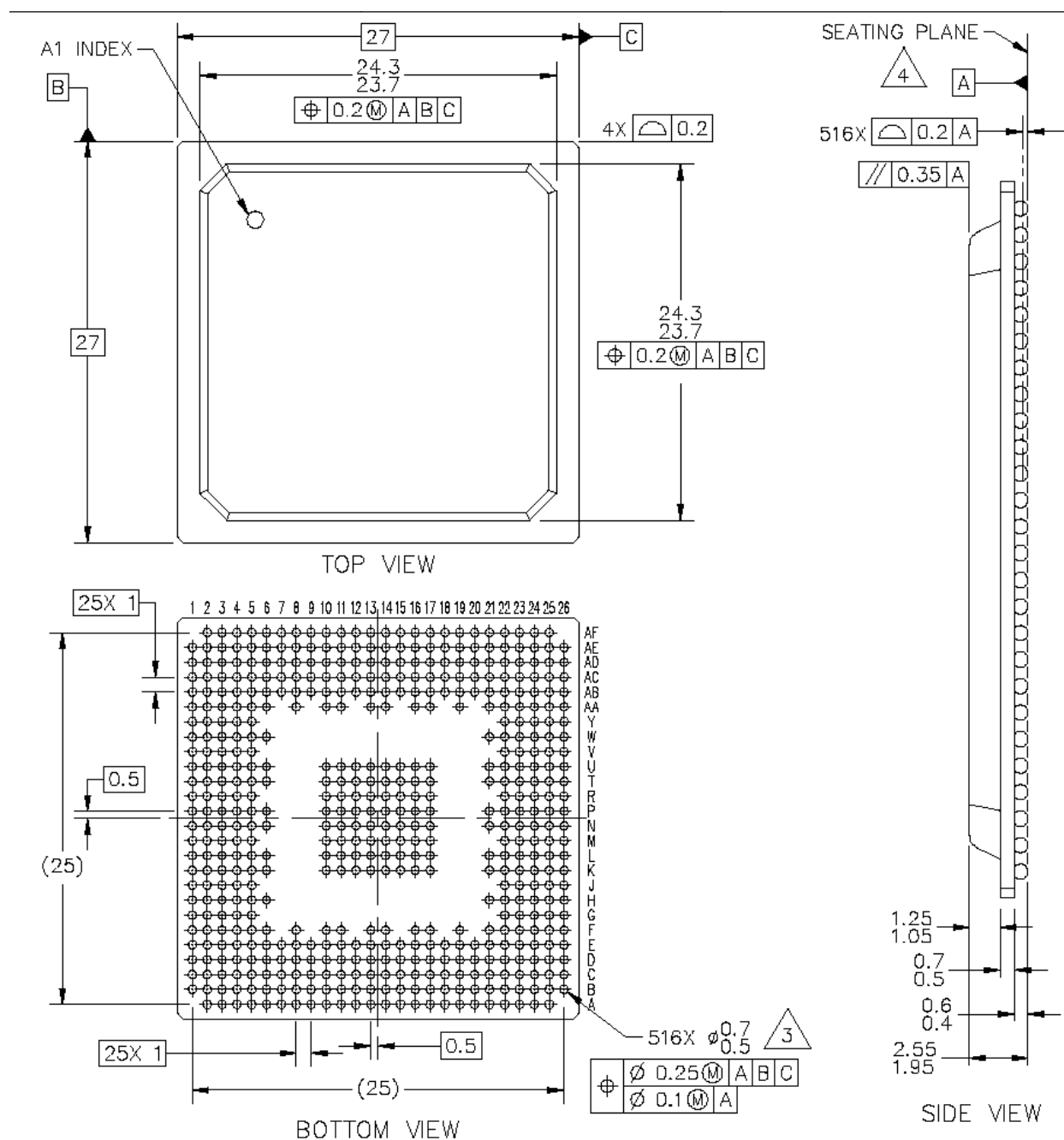


Figure 14. Mechanical Dimensions and Bottom Surface Nomenclature—516 PBGA

Table 23. Document Revision History (continued)

Revision	Date	Substantive Changes
1.2	09/2005	<ul style="list-style-type: none"> Added 133-MHz to the list of frequencies in the opening sentence of Section 6, “AC Electrical Characteristics”. Added 133 MHz columns to Table 9, Table 11, Table 12, and Table 13. Added footnote 2 to Table 13. Added the conditions note directly above Table 12.
1.1	01/2005	<ul style="list-style-type: none"> Modification for correct display of assertion level (“overbar”) for some signals
1.0	12/2004	<ul style="list-style-type: none"> Section 1.1: Added 8:1 ratio to Internal CPM/bus clock multiplier values Section 2: removed voltage tracking note Table 3: Note 2 updated regarding VDD/VCCSYN relationship to VDDH during power-on reset Table 4: Updated VDD and VCCSYN to 1.425 V - 1.575 V Table 8: Note 2 updated to reflect VIH=2.5 for TCK, TRST, PORESET; request for external pull-up removed. Section 4.6: Updated description of layout practices Table 8: Note 3 added regarding IIC compatibility Table 8: Updated nominal and maximum power dissipation values Table 9: updated PCI impedance to 27Ω, updated 60x and MEMC values and added note to reflect configurable impedance Section 6: Added sentence providing derating factor Section 6.1: added Note: Rise/Fall Time on CPM Input Pins Table 9: updated values for following specs: sp36b, sp37a, sp38a, sp39a, sp38b, sp40, sp41, sp42, sp43, sp42a Table 11: updated values for following specs: sp16a, sp16b, sp18a, sp18b, sp20, sp21, sp22 Section 6.2: added spread spectrum clocking note Section 6.2: added CLKIN jitter note Table 12: combined specs sp11 and sp11a Table 13: sp30 Data Bus minimum delay values changed to 0.8 Section 7: unit of ns added to Tval notes Section 7: Updated all notes to reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz. Section 7, “Clock Configuration Modes”: Updated all table footnotes reflect updated CPU Fmin of 150 MHz commercial temp devices, 175 MHz extended temp; CPM Fmin of 120 MHz. Table 21: correct superscript of footnote number after pin AD22 Table 21: remove DONE3 from PC12 Table 21: signals referring to TDMs C2 and D2 removed

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