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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I ² C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	18
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc920fdh-529

3. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
P89LPC920FDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
P89LPC921FDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
P89LPC922FDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
P89LPC922FN	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
P89LPC9221FN	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
P89LPC9221FDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

3.1 Ordering options

Table 2: Part options

Type number	Flash memory	Temperature range	Frequency
P89LPC920FDH	2 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC921FDH	4 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC922FDH	8 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC922FN	8 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC9221FN	8 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC9221FDH	8 kB	−40 °C to +85 °C	0 MHz to 18 MHz

4. Block diagram

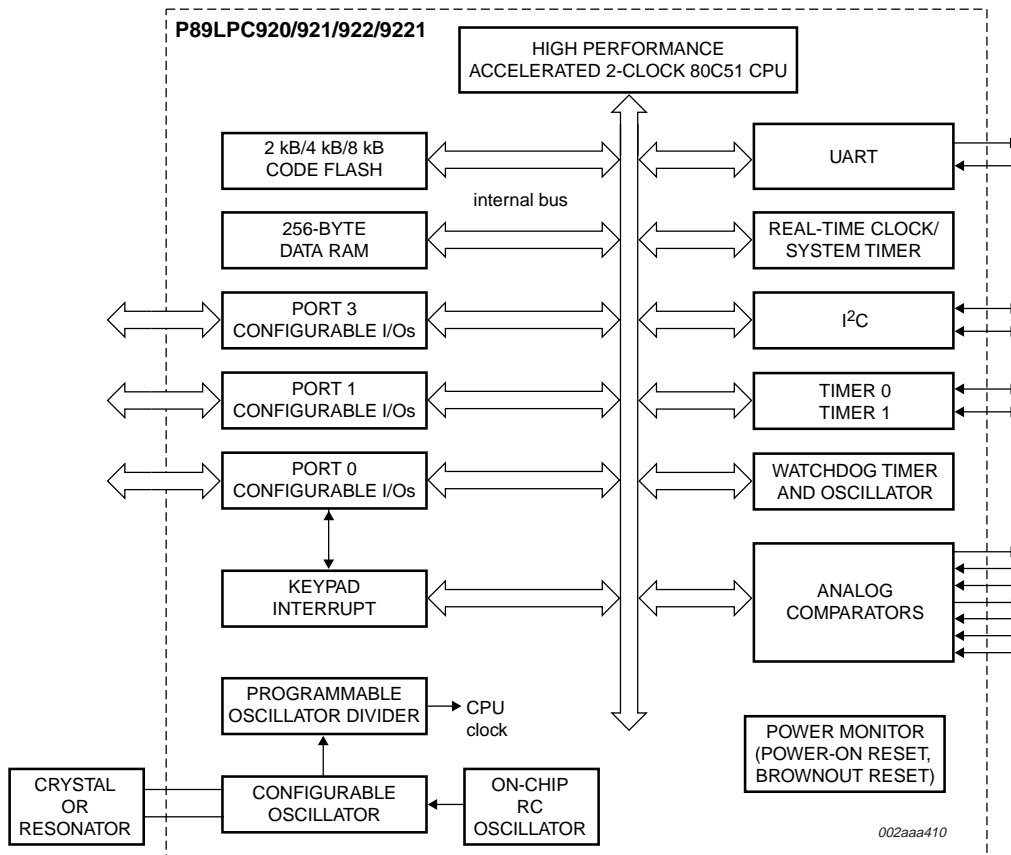


Fig 1. Block diagram.

Table 3: Pin description...continued

Symbol	Pin	Type	Description
P1.0 to P1.7		I/O, I ^[1]	<p>Port 1: Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.12.1 "Port configurations" and Table 8 "DC electrical characteristics" for details. P1.2 - P1.3 are open drain when used as outputs. P1.5 is input only.</p> <p>All pins have Schmitt triggered inputs.</p> <p>Port 1 also provides various special functions as described below:</p>
12		I/O	P1.0 — Port 1 bit 0.
		O	TXD — Transmitter output for the serial port.
11		I/O	P1.1 — Port 1 bit 1.
		I	RXD — Receiver input for the serial port.
10		I/O	P1.2 — Port 1 bit 2 (open-drain when used as output).
		I/O	T0 — Timer/counter 0 external count input or overflow output (open-drain when used as output).
		I/O	SCL — I ² C serial clock input/output.
9		I/O	P1.3 — Port 1 bit 3 (open-drain when used as output).
		I	INT0 — External interrupt 0 input.
		I/O	SDA — I ² C serial data input/output.
8		I/O	P1.4 — Port 1 bit 4. High current source (P89LPC9221).
		I	INT1 — External interrupt 1 input.
4		I	P1.5 — Port 1 bit 5 (input only).
		I	RST — External Reset input (if selected via FLASH configuration). A LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.
3		I/O	P1.6 — Port 1 bit 6. High current source (P89LPC9221).
2		I/O	P1.7 — Port 1 bit 7. High current source (P89LPC9221).

Table 3: Pin description...continued

Symbol	Pin	Type	Description
P3.0 to P3.1		I/O	<p>Port 3: Port 3 is an 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 8 "DC electrical characteristics" for details.</p> <p>All pins have Schmitt triggered inputs.</p> <p>Port 3 also provides various special functions as described below:</p>
	7	I/O	P3.0 — Port 3 bit 0.
		O	XTAL2 — Output from the oscillator amplifier (when a crystal oscillator option is selected via the FLASH configuration).
		O	CLKOUT — CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the real time clock/system timer.
	6	I/O	P3.1 — Port 3 bit 1.
		I	XTAL1 — Input to the oscillator circuit and internal clock generator circuits (when selected via the FLASH configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, and if XTAL1/XTAL2 are not used to generate the clock for the real time clock/system timer.
V _{SS}	5	I	Ground: 0 V reference.
V _{DD}	15	I	Power Supply: This is the power supply voltage for normal operation as well as Idle and Power down modes.

[1] Input/Output for P1.0-P1.4, P1.6, P1.7. Input for P1.5.

6. Logic symbol

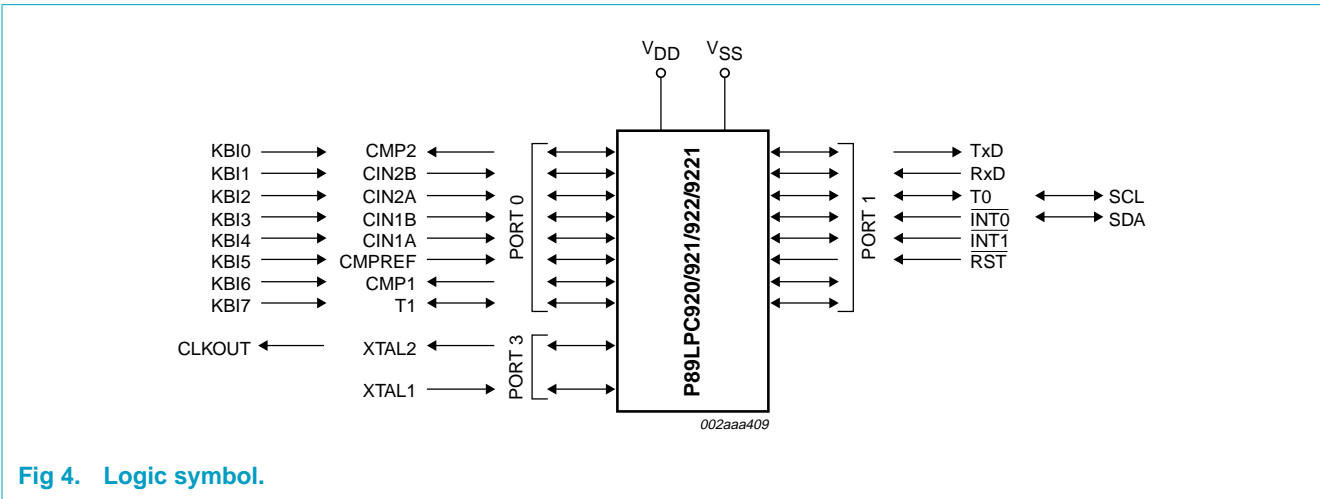


Fig 4. Logic symbol.

Table 4: Special function registers

* indicates SFRs that are bit addressable.

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB				LSB				Hex	Binary
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	00000000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-	DPS	00 ^[1]	000000x0
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	00000000
BRGR0 ^[2]	Baud rate generator rate LOW	BEH									00	00000000
BRGR1 ^[2]	Baud rate generator rate HIGH	BFH									00	00000000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00	xxxxxx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	OE1	CO1	CMF1	00 ^[1]	xx000000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00 ^[1]	xx000000
DIVM	CPU clock divide-by-M control	95H									00	00000000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer HIGH	83H									00	00000000
DPL	Data pointer LOW	82H									00	00000000
FMADRH	Program Flash address HIGH	E7H									00	00000000
FMADRL	Program Flash address LOW	E6H									00	00000000
FMCON	Program Flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	01110000
	Program Flash control (Write)	E4H	FMCMD. 7	FMCMD. 6	FMCMD. 5	FMCMD. 4	FMCMD. 3	FMCMD. 2	FMCMD. 1	FMCMD. 0		
FMDATA	Program Flash data	E5H									00	00000000
I2ADR	I ² C slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	00000000
		Bit address	DF	DE	DD	DC	DB	DA	D9	D8		
I2CON*	I ² C control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x00000x0
I2DAT	I ² C data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register HIGH	DDH									00	00000000

Table 4: Special function registers...continued

* indicates SFRs that are bit addressable.

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB				LSB				Hex	Binary
TRIM	Internal oscillator trim register	96H	-	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[5] [6]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[4] [6]	
WDL	Watchdog load	C1H									FF	11111111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

- [1] All ports are in input only (high impedance) state after power-up.
- [2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is '0'. If any are written while BRGEN = 1, the result is unpredictable.
- [3] The RSTSRC register reflects the cause of the P89LPC920/921/922/9221 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx110000.
- [4] After reset, the value is 111001x1, i.e., PRE2-PRE0 are all '1', WDRUN = 1 and WDCLK = 1. WDTOF bit is '1' after watchdog reset and is '0' after power-on reset. Other resets will not affect WDTOF.
- [5] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.
- [6] The only reset source that affects these SFRs is power-on reset.

8. Functional description

Remark: Please refer to the *P89LPC920/921/922/9221 User's Manual* for a more detailed functional description.

8.1 Enhanced CPU

The P89LPC920/921/922/9221 uses an enhanced 80C51 CPU which runs at 6 times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

8.2 Clocks

8.2.1 Clock definitions

The P89LPC920/921/922/9221 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see Figure 5) and can also be optionally divided to a slower frequency (see Section 8.7 “CPU Clock (CCLK) modification: DIVM register”).

Note: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output.

PCLK — Clock for the various peripheral devices and is CCLK/2

8.2.2 CPU clock (OSCCLK)

The P89LPC920/921/922/9221 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the FLASH is programmed and include an on-chip watchdog oscillator, an on-chip RC oscillator, an oscillator using an external crystal, or an external clock source. The crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 12 MHz.

8.2.3 Low speed oscillator option

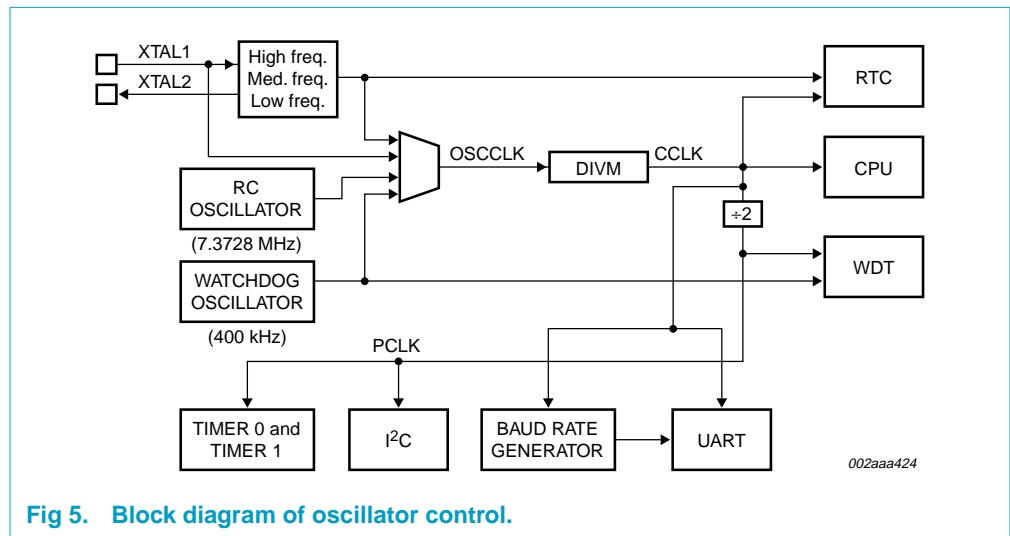
This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

8.2.4 Medium speed oscillator option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

8.2.5 High speed oscillator option

This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below**



8.10 Data RAM arrangement

The 256 bytes of on-chip RAM are organized as shown in Table 5.

Table 5: On-chip data memory usages

Type	Data RAM	Size (bytes)
DATA	Memory that can be addressed directly and indirectly	128
IDATA	Memory that can be addressed indirectly	256

8.11 Interrupts

The P89LPC920/921/922/9221 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources. The P89LPC920/921/922/9221 supports 12 interrupt sources: external interrupts 0 and 1, timers 0 and 1, serial port Tx, serial port Rx, combined serial port Rx/Tx, brownout detect, watchdog/real-time clock, I²C, keyboard, and comparators 1 and 2.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1, and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

8.11.1 External interrupt inputs

The P89LPC920/921/922/9221 has two external interrupt inputs as well as the Keypad Interrupt function. The two interrupt inputs are identical to those present on the standard 80C51 microcontrollers.

These external interrupts can be programmed to be level-triggered or edge-triggered by setting or clearing bit IT1 or IT0 in Register TCON.

In edge-triggered mode if successive samples of the $\overline{\text{INTn}}$ pin show a HIGH in one cycle and a LOW in the next cycle, the interrupt request flag IEN in TCON is set, causing an interrupt request.

If an external interrupt is enabled when the P89LPC920/921/922/9221 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 8.14 "Power reduction modes" for details.

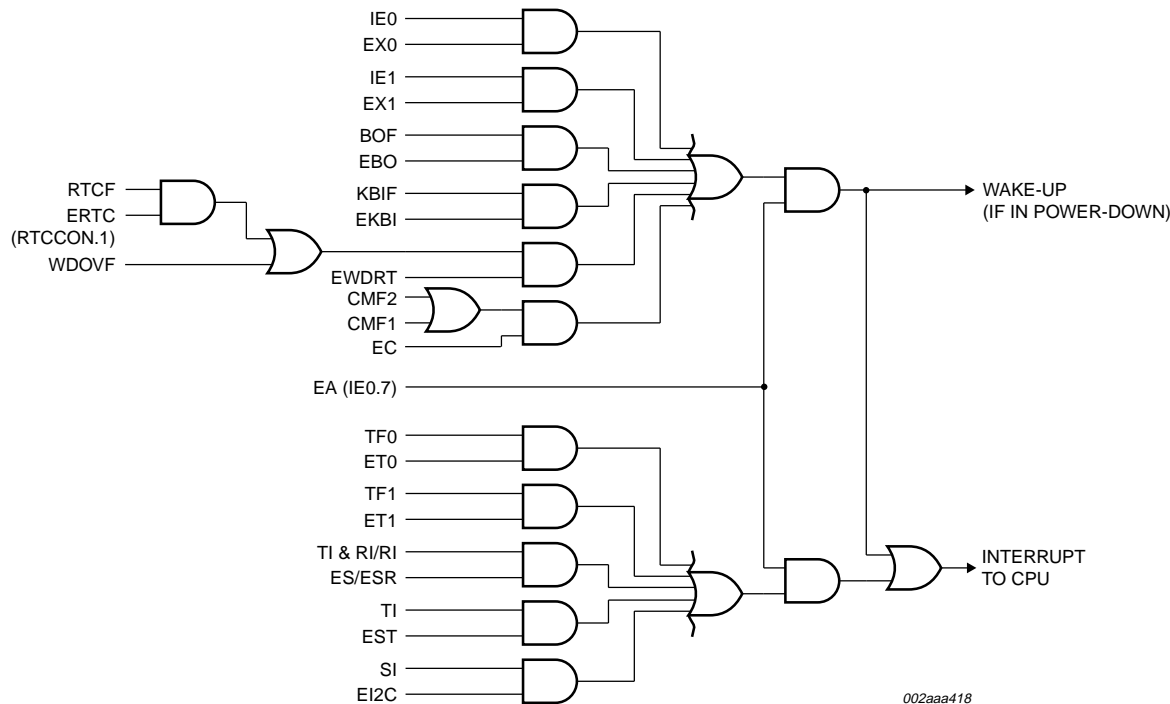


Fig 6. Interrupt sources, interrupt enables, and power-down wake-up sources.

8.12 I/O ports

The P89LPC920/921/922/9221 has three I/O ports: Port 0, Port 1, and Port 3. Ports 0 and 1 are 8-bit ports, and Port 3 is a 2-bit port. The exact number of I/O pins available depend upon the clock and reset options chosen, as shown in Table 6.

Table 6: Number of I/O pins available

Clock source	Reset option	Number of I/O pins (20-pin package)
On-chip oscillator or watchdog oscillator	No external reset (except during power-up)	18
	External $\overline{\text{RST}}$ pin supported ^[1]	17
External clock input	No external reset (except during power-up)	17
	External $\overline{\text{RST}}$ pin supported ^[1]	16
Low/medium/high speed oscillator (external crystal or resonator)	No external reset (except during power-up)	16
	External $\overline{\text{RST}}$ pin supported ^[1]	15

[1] Required for operation above 12 MHz.

8.12.1 Port configurations

All but three I/O port pins on the P89LPC920/921/922/9221 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

P1.5 ($\overline{\text{RST}}$) can only be an input and cannot be configured.

P1.2 (SCL/T0) and P1.3 (SDA/ $\overline{\text{INT0}}$) may only be configured to be either input-only or open-drain.

8.12.2 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC920/921/922/9221 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD} , causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.12.3 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic '0'. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD} .

An open-drain port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.12.4 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt-triggered input that also has a glitch suppression circuit.

8.12.5 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic '1'. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt-triggered input that also has a glitch suppression circuit. The P89LPC9221 device has high source current on eight pins in push-pull mode. See [Table 8 "DC electrical characteristics"](#).

8.12.6 Port 0 analog functions

The P89LPC920/921/922/9221 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high impedance) mode as described in [Section 8.12.4](#).

Digital inputs on Port 0 may be disabled through the use of the PT0AD register, bits 1:5. On any reset, PT0AD1:5 defaults to '0's to enable digital functions.

8.14.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

8.14.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC920/921/922/9221 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the RAM keep-alive voltage V_{RAM} . This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{RAM} , therefore it is highly recommended to wake up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during Power-down. These include: Brownout detect, Watchdog Timer, Comparators (note that Comparators can be powered-down separately), and Real-Time Clock (RTC)/System Timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock AND the RTC is enabled.

8.14.3 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock the RTC during Power-down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the Real-Time Clock running during Power-down.

8.15 Reset

The P1.5/ \overline{RST} pin can function as either an active-LOW reset input or as a digital input, P1.5. The RPE (Reset Pin Enable) bit in UCFG1, when set to '1', enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, the RPE selection is overridden and this pin will always function as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this input will function either as an external reset input or as a digital input as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit.

Remark: During a power cycle, V_{DD} must fall below V_{POR} (see [Table 8 "DC electrical characteristics" on page 36](#)) before power is reapplied, in order to ensure a power-on reset.

Reset can be triggered from the following sources:

8.16.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

8.16.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

8.16.5 Mode 6

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

8.16.6 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

8.17 Real-Time clock/system timer

The P89LPC920/921/922/9221 has a simple Real-Time clock that allows a user to continue running an accurate timer while the rest of the device is powered-down. The Real-Time clock can be a wake-up or an interrupt source. The Real-Time clock is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all '0's, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator, provided that the XTAL oscillator is not being used as the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source. Only power-on reset will reset the Real-Time clock and its associated SFRs to the default state.

8.18 UART

The P89LPC920/921/922/9221 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC920/921/922/9221 does include an independent Baud Rate Generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in 4 modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16.

8.18.1 Mode 0

Serial data enters and exits through Rx/D. Tx/D outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $\frac{1}{16}$ of the CPU clock frequency.

8.18.2 Mode 1

10 bits are transmitted (through TxD) or received (through RxD): a start bit (logical '0'), 8 data bits (LSB first), and a stop bit (logical '1'). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in [Section 8.18.5 "Baud rate generator and selection"](#)).

8.18.3 Mode 2

11 bits are transmitted (through TxD) or received (through RxD): start bit (logical '0'), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical '1'). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of '0' or '1'. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is not saved. The baud rate is programmable to either $\frac{1}{16}$ or $\frac{1}{32}$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

8.18.4 Mode 3

11 bits are transmitted (through TxD) or received (through RxD): a start bit (logical '0'), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical '1'). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in [Section 8.18.5 "Baud rate generator and selection"](#)).

8.18.5 Baud rate generator and selection

The P89LPC920/921/922/9221 enhanced UART has an independent Baud Rate Generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1 and BRGR0 SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1 but is much more accurate. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UART can use either Timer 1 or the baud rate generator output (see [Figure 7](#)). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is set. The independent Baud Rate Generator uses OSCCLK.

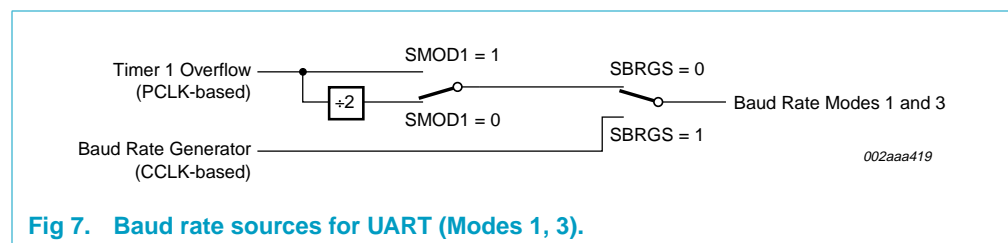


Fig 7. Baud rate sources for UART (Modes 1, 3).

8.18.6 Framing error

Framing error is reported in the status register (SSTAT). In addition, if SMOD0 (PCON.6) is '1', framing errors can be made available in SCON.7 respectively. If SMOD0 is '0', SCON.7 is SM0. It is recommended that SM0 and SM1 (SCON.7:6) are set up when SMOD0 is '0'.

8.18.7 Break detect

Break detect is reported in the status register (SSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device and force the device into ISP mode.

8.18.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = '0'), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = '0').

8.18.9 Transmit interrupts with double buffering enabled (Modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the Tx interrupt is generated when the double buffer is ready to receive new data.

8.18.10 The 9th bit (bit 8) in double buffering (Modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the Tx interrupt.

If double buffering is enabled, TB8 **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

Flash programming and erasing: There are three methods of erasing or programming of the Flash memory that may be used. First, the Flash may be programmed or erased in the end-user application by calling low-level routines through a common entry point. Second, the on-chip ISP boot loader may be invoked. This ISP boot loader will, in turn, call low-level routines through the same common entry point that can be used by the end-user application. Third, the Flash may be programmed or erased using the parallel method by using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead this device provides a 32-bit CRC result on either a sector or the entire 2 kB/4 kB/8 kB of user code space.

Boot ROM: When the microcontroller programs its own Flash memory, all of the low-level details are handled by code that is contained in a Boot ROM that is separate from the Flash memory. A user program simply calls the common entry point in the Boot ROM with appropriate parameters to accomplish the desired operation. The Boot ROM include operations such as erase sector, erase page, program page, CRC, program security bit, etc. The Boot ROM occupies the program memory space at the top of the address space from FF00H to FFFFH, thereby not conflicting with the user program memory space.

Power-on reset code execution: The P89LPC920/921/922/9221 contains two special Flash elements: the Boot Vector and the Boot Status Bit. Following reset, the P89LPC920/921/922/9221 examines the contents of the Boot Status Bit. If the Boot Status Bit is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Boot Status Bit is set to a one, the contents of the Boot Vector is used as the high byte of the execution address and the low byte is set to 00H. The factory default setting is 1FH for the P89LPC9221 and P89LPC922, and corresponds to the address 1F00H for the default ISP boot loader. The factory default setting is 0FH for the P89LPC921 and corresponds to the address 0F00H for the default ISP boot loader. The factory default setting for the LPC920 is 07H and corresponds to the address 0700H. This boot loader is pre-programmed at the factory into this address space and can be erased by the user. **Users who wish to use this loader should take precautions to avoid erasing the 1 kB sector from 1C00H to 1FFFH in the P89LPC922/9221 or the 1 kB sector from 0C00H to 0FFFH in the P89LPC921, or the 1 kB sector from 0400H to 07FFH in the P89LPC920. Instead, the page erase function can be used to erase the eight 64-byte pages which comprise the lower 512 bytes of the sector.** A custom boot loader can be written with the Boot Vector set to the custom boot loader, if desired.

Hardware activation of the boot loader: The boot loader can also be executed by forcing the device into ISP mode during a power-on sequence (see the *P89LPC920/921/922/9221 User's Manual* for specific information). This has the same effect as having a non-zero Boot Status Bit. This allows an application to be built that will normally execute user code but can be manually forced into ISP operation. If the factory default setting for the Boot Vector is changed, it will no longer point to the factory pre-programmed ISP boot loader code. If this happens, the only way it is possible to change the contents of the Boot Vector is through the parallel programming method, provided that the end user application does not contain a customized loader that provides for erasing and reprogramming of the Boot Vector

and Boot Status Bit. After programming the Flash, the Boot Status Bit should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

In-System Programming (ISP): In-System Programming is performed without removing the microcontroller from the system. The In-System Programming facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the P89LPC920/921/922/9221 through the serial port. This firmware is provided by Philips and embedded within each P89LPC920/921/922/9221 device. The Philips In-System Programming facility has made in-system programming in an embedded application possible with a minimum of additional expense in components and circuit board area. The ISP function uses five pins (V_{DD} , V_{SS} , TXD, RXD, and \overline{RST}). Only a small connector needs to be available to interface your application to an external circuit in order to use this feature. Please see the *P89LPC920/921/922/9221 User's Manual* for additional details.

In-Application Programming (IAP): Several In-Application Programming (IAP) calls are available for use by an application program to permit selective erasing and programming of Flash sectors, pages, security bits, configuration bytes, and device identification. All calls are made through a common interface, PGM_MTP. The programming functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FF00H. Please see the *P89LPC920/921/922/9221 User's Manual* for additional details.

In-Circuit Programming (ICP): In-Circuit Programming is a method intended to allow commercial programmers to program and erase these devices without removing the microcontroller from the system. The In-Circuit Programming facility consists of a series of internal hardware resources to facilitate remote programming of the P89LPC920/921/922/9221 through a two-wire serial interface. Philips has made in-circuit programming in an embedded application possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins (V_{DD} , V_{SS} , P0.5, P0.4, and \overline{RST}). Only a small connector needs to be available to interface your application to an external programmer in order to use this feature.

8.25 User configuration bytes

A number of user-configurable features of the P89LPC920/921/922/9221 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the Flash byte UCFG1. Please see the *P89LPC920/921/922/9221 User's Manual* for additional details.

8.26 User sector security bytes

There are two/four/eight User Sector Security Bytes, each corresponding to one sector. Please see the *P89LPC920/921/922/9221 User's Manual* for additional details.

13. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

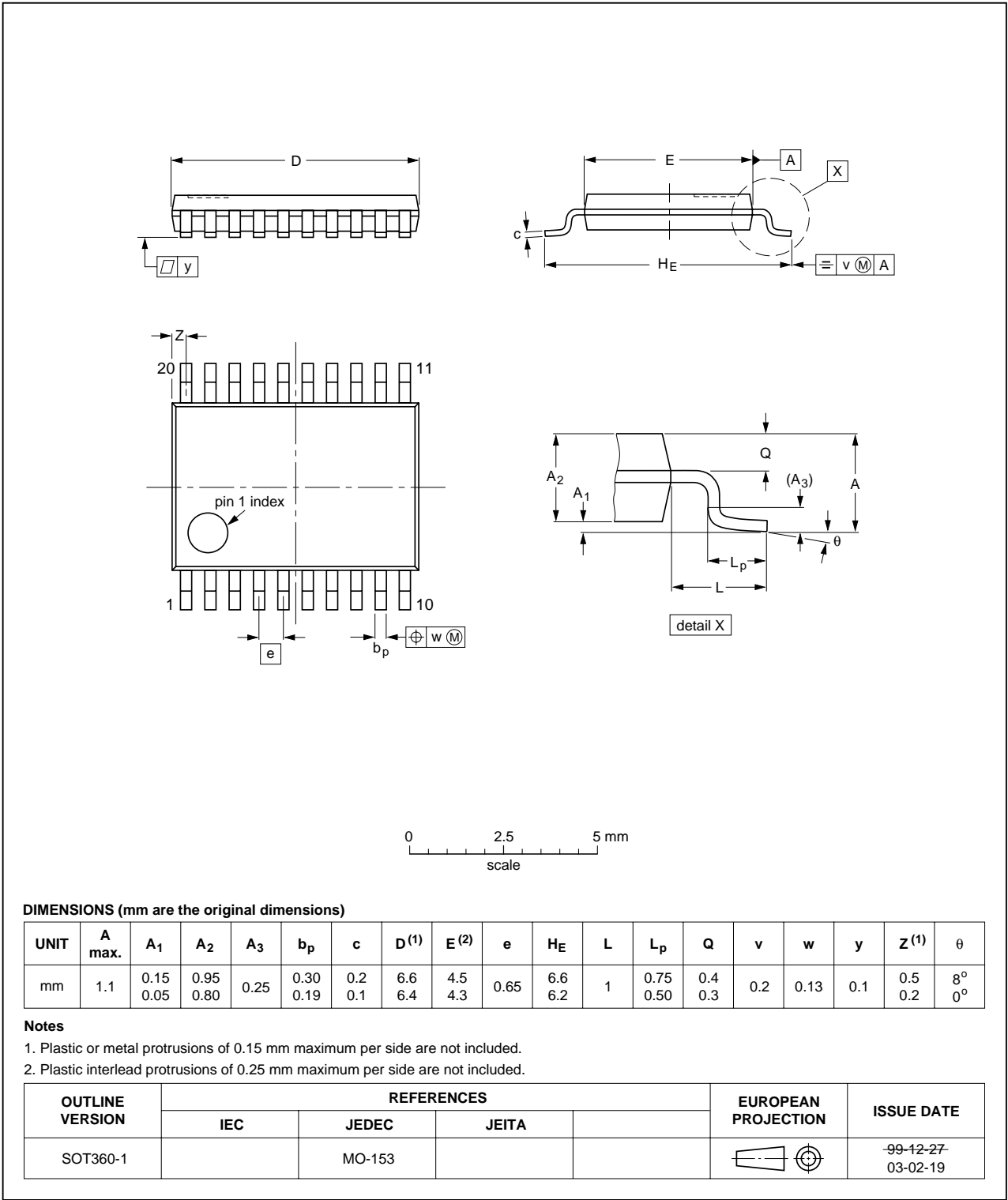


Fig 15. TSSOP20 (SOT360-1).

15. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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18. Licenses

Purchase of Philips I²C components



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

17. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors

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