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Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I ² C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc921fdh-512

5. Pinning information

5.1 Pinning

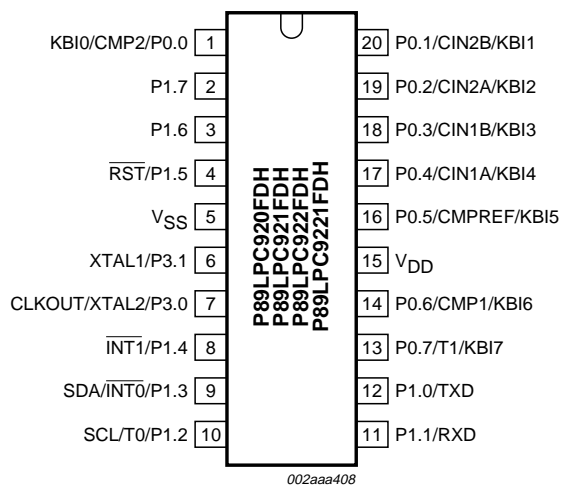


Fig 2. TSSOP20 pin configuration.

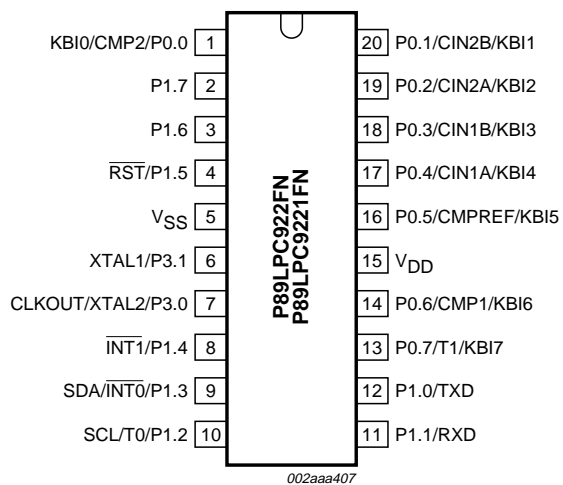


Fig 3. DIP20 pin configuration.

5.2 Pin description

Table 3: Pin description

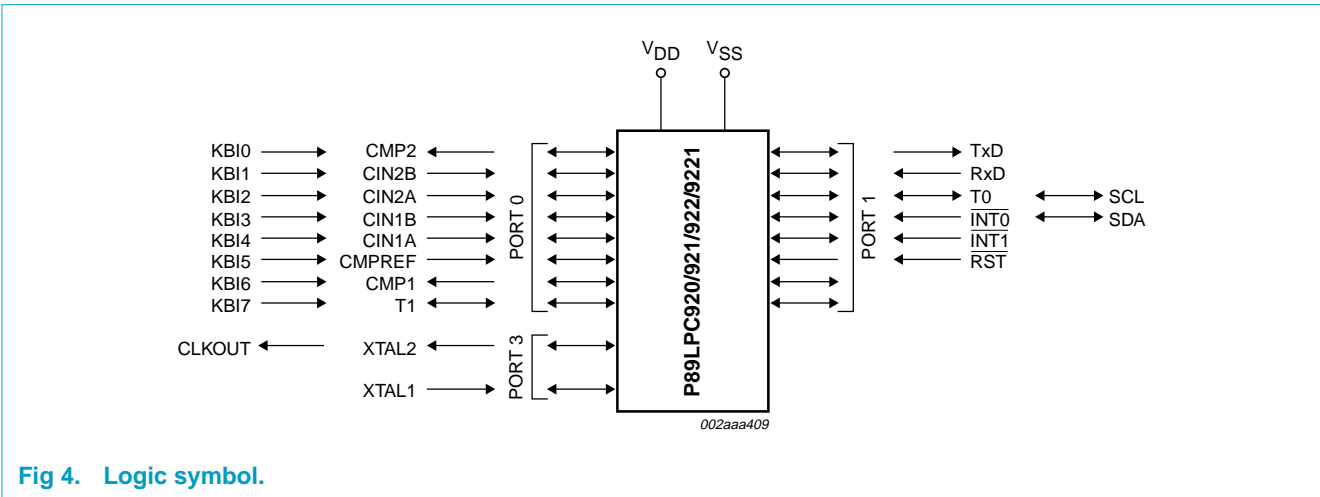
Symbol	Pin	Type	Description
P0.0 to P0.7		I/O	<p>Port 0: Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 “Port configurations” and Table 8 “DC electrical characteristics” for details.</p> <p>The Keypad Interrupt feature operates with Port 0 pins.</p> <p>All pins have Schmitt triggered inputs.</p> <p>Port 0 also provides various special functions as described below:</p>
1		I/O	P0.0 — Port 0 bit 0.
		O	CMP2 — Comparator 2 output.
		I	KBI0 — Keyboard input 0.
20		I/O	P0.1 — Port 0 bit 1.
		I	CIN2B — Comparator 2 positive input B.
		I	KBI1 — Keyboard input 1.
19		I/O	P0.2 — Port 0 bit 2.
		I	CIN2A — Comparator 2 positive input A.
		I	KBI2 — Keyboard input 2.
18		I/O	P0.3 — Port 0 bit 3. High current source (P89LPC9221).
		I	CIN1B — Comparator 1 positive input B.
		I	KBI3 — Keyboard input 3.
17		I/O	P0.4 — Port 0 bit 4. High current source (P89LPC9221).
		I	CIN1A — Comparator 1 positive input A.
		I	KBI4 — Keyboard input 4.
16		I/O	P0.5 — Port 0 bit 5. High current source (P89LPC9221).
		I	CMPREF — Comparator reference (negative) input.
		I	KBI5 — Keyboard input 5.
14		I/O	P0.6 — Port 0 bit 6. High current source (P89LPC9221).
		O	CMP1 — Comparator 1 output.
		I	KBI6 — Keyboard input 6.
13		I/O	P0.7 — Port 0 bit 7. High current source (P89LPC9221).
		I/O	T1 — Timer/counter 1 external count input or overflow output.
		I	KBI7 — Keyboard input 7.

Table 3: Pin description...continued

Symbol	Pin	Type	Description
P3.0 to P3.1		I/O	<p>Port 3: Port 3 is an 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 8 "DC electrical characteristics" for details.</p> <p>All pins have Schmitt triggered inputs.</p> <p>Port 3 also provides various special functions as described below:</p>
	7	I/O	P3.0 — Port 3 bit 0.
		O	XTAL2 — Output from the oscillator amplifier (when a crystal oscillator option is selected via the FLASH configuration).
		O	CLKOUT — CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the real time clock/system timer.
	6	I/O	P3.1 — Port 3 bit 1.
		I	XTAL1 — Input to the oscillator circuit and internal clock generator circuits (when selected via the FLASH configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, and if XTAL1/XTAL2 are not used to generate the clock for the real time clock/system timer.
V _{SS}	5	I	Ground: 0 V reference.
V _{DD}	15	I	Power Supply: This is the power supply voltage for normal operation as well as Idle and Power down modes.

[1] Input/Output for P1.0-P1.4, P1.6, P1.7. Input for P1.5.

6. Logic symbol



7. Special function registers

Remark: Special Function Registers (SFRs) accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can **only** be written and read as follows:
 - '-' Unless otherwise specified, **must** be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
 - '0' **must** be written with '0', and will return a '0' when read.
 - '1' **must** be written with '1', and will return a '1' when read.

Table 4: Special function registers

* indicates SFRs that are bit addressable.

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB				LSB				Hex	Binary
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	00000000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-	DPS	00 ^[1]	000000x0
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	00000000
BRGR0 ^[2]	Baud rate generator rate LOW	BEH									00	00000000
BRGR1 ^[2]	Baud rate generator rate HIGH	BFH									00	00000000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00	xxxxxx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	OE1	CO1	CMF1	00 ^[1]	xx000000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00 ^[1]	xx000000
DIVM	CPU clock divide-by-M control	95H									00	00000000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer HIGH	83H									00	00000000
DPL	Data pointer LOW	82H									00	00000000
FMADRH	Program Flash address HIGH	E7H									00	00000000
FMADRL	Program Flash address LOW	E6H									00	00000000
FMCON	Program Flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	01110000
	Program Flash control (Write)	E4H	FMCMD. 7	FMCMD. 6	FMCMD. 5	FMCMD. 4	FMCMD. 3	FMCMD. 2	FMCMD. 1	FMCMD. 0		
FMDATA	Program Flash data	E5H									00	00000000
I2ADR	I ² C slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	00000000
		Bit address	DF	DE	DD	DC	DB	DA	D9	D8		
I2CON*	I ² C control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x00000x0
I2DAT	I ² C data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register HIGH	DDH									00	00000000

8. Functional description

Remark: Please refer to the *P89LPC920/921/922/9221 User's Manual* for a more detailed functional description.

8.1 Enhanced CPU

The P89LPC920/921/922/9221 uses an enhanced 80C51 CPU which runs at 6 times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

8.2 Clocks

8.2.1 Clock definitions

The P89LPC920/921/922/9221 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see [Figure 5](#)) and can also be optionally divided to a slower frequency (see [Section 8.7 “CPU Clock \(CCLK\) modification: DIVM register”](#)).

Note: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output.

PCLK — Clock for the various peripheral devices and is CCLK/2

8.2.2 CPU clock (OSCCLK)

The P89LPC920/921/922/9221 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the FLASH is programmed and include an on-chip watchdog oscillator, an on-chip RC oscillator, an oscillator using an external crystal, or an external clock source. The crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 12 MHz.

8.2.3 Low speed oscillator option

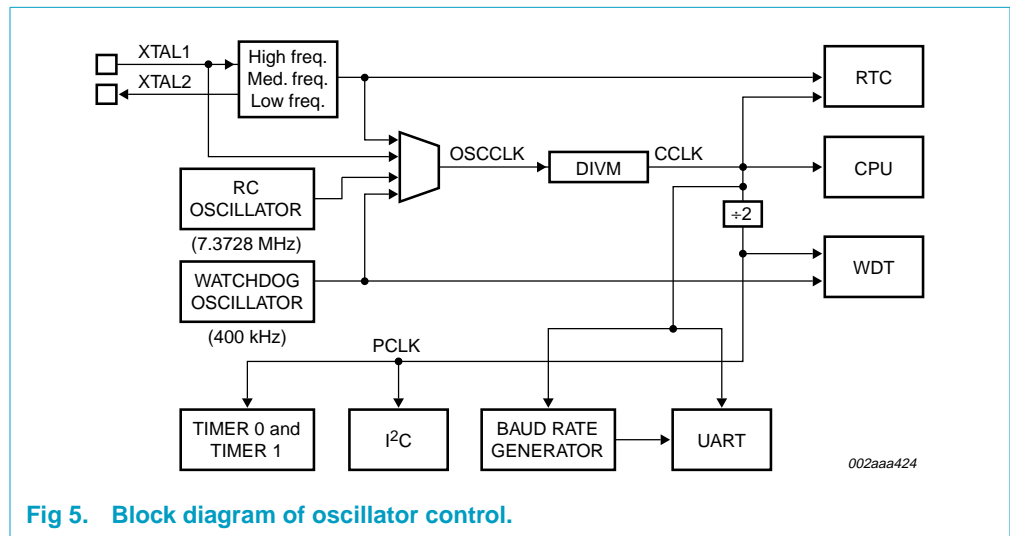
This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

8.2.4 Medium speed oscillator option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

8.2.5 High speed oscillator option

This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below**



P1.2 (SCL/T0) and P1.3 (SDA/ $\overline{\text{INT0}}$) may only be configured to be either input-only or open-drain.

8.12.2 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC920/921/922/9221 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD} , causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.12.3 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic '0'. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD} .

An open-drain port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.12.4 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt-triggered input that also has a glitch suppression circuit.

8.12.5 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic '1'. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt-triggered input that also has a glitch suppression circuit. The P89LPC9221 device has high source current on eight pins in push-pull mode. See [Table 8 "DC electrical characteristics"](#).

8.12.6 Port 0 analog functions

The P89LPC920/921/922/9221 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high impedance) mode as described in [Section 8.12.4](#).

Digital inputs on Port 0 may be disabled through the use of the PT0AD register, bits 1:5. On any reset, PT0AD1:5 defaults to '0's to enable digital functions.

8.12.7 Additional port features

After power-up, all pins are in Input-Only mode. **Please note that this is different from the LPC76x series of devices.**

- After power-up, all I/O pins except P1.5, may be configured by software.
- Pin P1.5 is input only. Pins P1.2 and P1.3 and are configurable for either input-only or open-drain.

Every output on the P89LPC920/921/922/9221 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to [Table 8 “DC electrical characteristics”](#) for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

8.13 Power monitoring functions

The P89LPC920/921/922/9221 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on Detect and Brownout detect.

8.13.1 Brownout detection

The Brownout detect function determines if the power supply voltage drops below a certain level. The default operation is for a Brownout detection to cause a processor reset, however it may alternatively be configured to generate an interrupt.

Brownout detection may be enabled or disabled in software.

If Brownout detection is enabled, the brownout condition occurs when V_{DD} falls below the brownout trip voltage, V_{BO} (see [Table 8 “DC electrical characteristics”](#)), and is negated when V_{DD} rises above V_{BO} . If the P89LPC920/921/922/9221 device is to operate with a power supply that can be below 2.7 V, BOE should be left in the unprogrammed state so that the device can operate at 2.4 V, otherwise continuous brownout reset may prevent the device from operating.

For correct activation of Brownout detect, the V_{DD} rise and fall times must be observed. Please see [Table 8 “DC electrical characteristics”](#) for specifications.

8.13.2 Power-on detection

The Power-on Detect has a function similar to the Brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where Brownout detect can work. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

8.14 Power reduction modes

The P89LPC920/921/922/9221 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and total Power-down mode.

8.16.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

8.16.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

8.16.5 Mode 6

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

8.16.6 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

8.17 Real-Time clock/system timer

The P89LPC920/921/922/9221 has a simple Real-Time clock that allows a user to continue running an accurate timer while the rest of the device is powered-down. The Real-Time clock can be a wake-up or an interrupt source. The Real-Time clock is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all '0's, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator, provided that the XTAL oscillator is not being used as the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source. Only power-on reset will reset the Real-Time clock and its associated SFRs to the default state.

8.18 UART

The P89LPC920/921/922/9221 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC920/921/922/9221 does include an independent Baud Rate Generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in 4 modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16.

8.18.1 Mode 0

Serial data enters and exits through Rx/D. Tx/D outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $\frac{1}{16}$ of the CPU clock frequency.

8.18.7 Break detect

Break detect is reported in the status register (SSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device and force the device into ISP mode.

8.18.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = '0'), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = '0').

8.18.9 Transmit interrupts with double buffering enabled (Modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the Tx interrupt is generated when the double buffer is ready to receive new data.

8.18.10 The 9th bit (bit 8) in double buffering (Modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the Tx interrupt.

If double buffering is enabled, TB8 **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

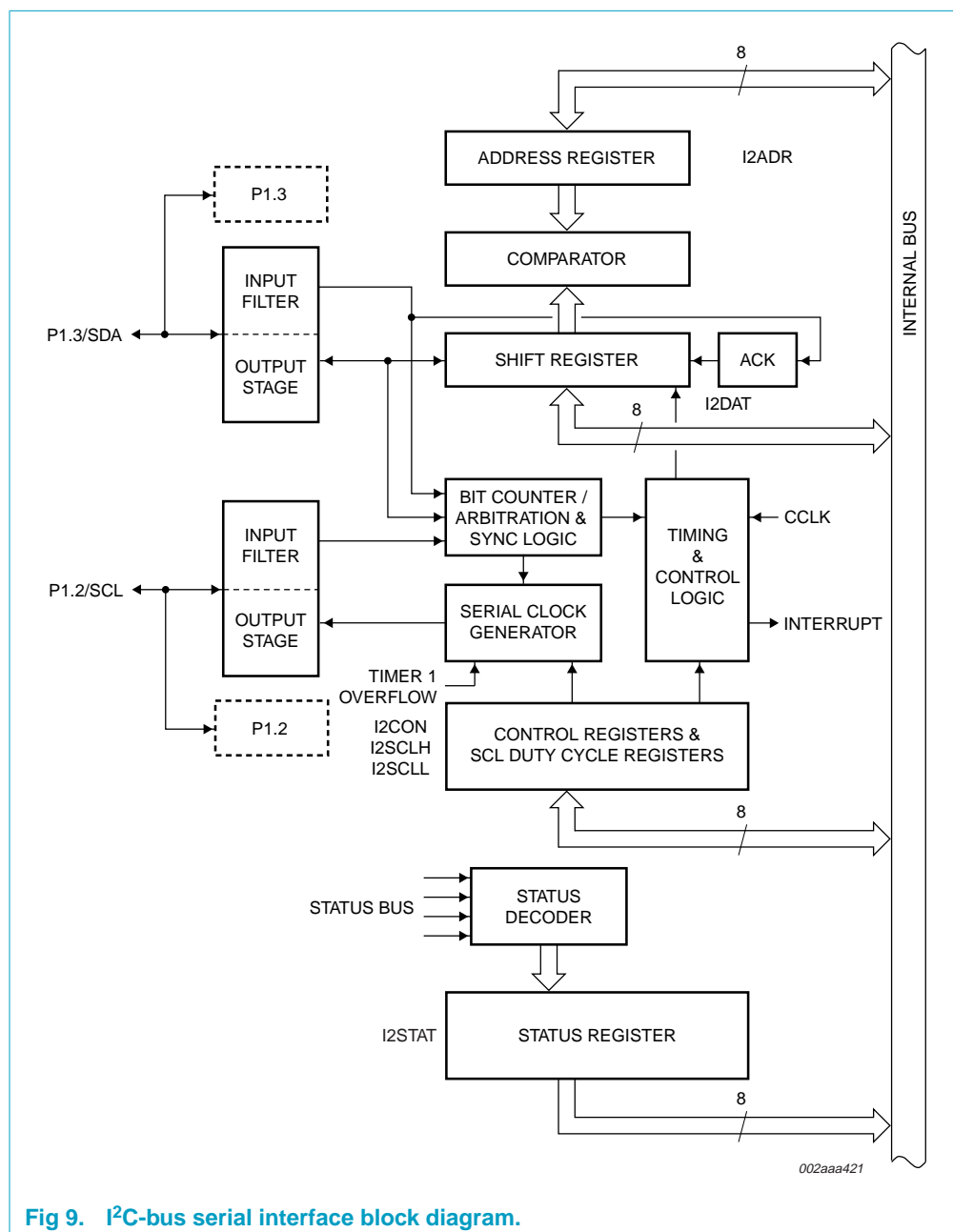


Fig 9. I²C-bus serial interface block diagram.

8.20.2 Comparator interrupt

Each comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The two comparators use one common interrupt vector. If both comparators enable interrupts, after entering the interrupt service routine, the user needs to read the flags to determine which comparator caused the interrupt.

8.20.3 Comparators and power reduction modes

Either or both comparators may remain enabled when Power-down or Idle mode is activated, but both comparators are disabled automatically in Total Power-down mode. If a comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the oscillator stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparators via PCONA.5, or put the device in Total Power-down mode.

8.21 Keypad interrupt (KBI)

The Keypad Interrupt function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

The Keypad Interrupt Mask Register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to define equal or not-equal for the comparison.

In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake up the CPU from Idle or Power-down modes. This feature is particularly useful in handheld, battery-powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the flag and cause an interrupt, the pattern on Port 0 must be held longer than 6 CCLKs.

Flash programming and erasing: There are three methods of erasing or programming of the Flash memory that may be used. First, the Flash may be programmed or erased in the end-user application by calling low-level routines through a common entry point. Second, the on-chip ISP boot loader may be invoked. This ISP boot loader will, in turn, call low-level routines through the same common entry point that can be used by the end-user application. Third, the Flash may be programmed or erased using the parallel method by using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead this device provides a 32-bit CRC result on either a sector or the entire 2 kB/4 kB/8 kB of user code space.

Boot ROM: When the microcontroller programs its own Flash memory, all of the low-level details are handled by code that is contained in a Boot ROM that is separate from the Flash memory. A user program simply calls the common entry point in the Boot ROM with appropriate parameters to accomplish the desired operation. The Boot ROM include operations such as erase sector, erase page, program page, CRC, program security bit, etc. The Boot ROM occupies the program memory space at the top of the address space from FF00H to FFFFH, thereby not conflicting with the user program memory space.

Power-on reset code execution: The P89LPC920/921/922/9221 contains two special Flash elements: the Boot Vector and the Boot Status Bit. Following reset, the P89LPC920/921/922/9221 examines the contents of the Boot Status Bit. If the Boot Status Bit is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Boot Status Bit is set to a one, the contents of the Boot Vector is used as the high byte of the execution address and the low byte is set to 00H. The factory default setting is 1FH for the P89LPC9221 and P89LPC922, and corresponds to the address 1F00H for the default ISP boot loader. The factory default setting is 0FH for the P89LPC921 and corresponds to the address 0F00H for the default ISP boot loader. The factory default setting for the LPC920 is 07H and corresponds to the address 0700H. This boot loader is pre-programmed at the factory into this address space and can be erased by the user. **Users who wish to use this loader should take precautions to avoid erasing the 1 kB sector from 1C00H to 1FFFH in the P89LPC922/9221 or the 1 kB sector from 0C00H to 0FFFH in the P89LPC921, or the 1 kB sector from 0400H to 07FFH in the P89LPC920. Instead, the page erase function can be used to erase the eight 64-byte pages which comprise the lower 512 bytes of the sector.** A custom boot loader can be written with the Boot Vector set to the custom boot loader, if desired.

Hardware activation of the boot loader: The boot loader can also be executed by forcing the device into ISP mode during a power-on sequence (see the *P89LPC920/921/922/9221 User's Manual* for specific information). This has the same effect as having a non-zero Boot Status Bit. This allows an application to be built that will normally execute user code but can be manually forced into ISP operation. If the factory default setting for the Boot Vector is changed, it will no longer point to the factory pre-programmed ISP boot loader code. If this happens, the only way it is possible to change the contents of the Boot Vector is through the parallel programming method, provided that the end user application does not contain a customized loader that provides for erasing and reprogramming of the Boot Vector

10. Static characteristics

Table 8: DC electrical characteristics

$V_{DD} = 2.4\text{ V to }3.6\text{ V}$ unless otherwise specified.

$T_{amb} = -40\text{ °C to }+85\text{ °C}$ for industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$I_{DD(oper)}$	power supply current, operating	3.6 V; 12 MHz	[2] -	9	15	mA
		3.6 V; 18 MHz	[2] -	11.5	20	mA
$I_{DD(idle)}$	power supply current, Idle mode	3.6 V; 12 MHz	[2] -	3.25	5	mA
		3.6 V; 18 MHz	[2] -	5	7	mA
$I_{DD(PD)}$	power supply current, Power-down mode, voltage comparators powered-down	3.6 V	[2] -	55	80	μA
$I_{DD(TPD)}$	power supply current, Total Power-down mode	3.6 V	[2] -	1	5	μA
$(dV_{DD}/dt)_r$	V_{DD} rise rate		-	-	2	mV/μs
$(dV_{DD}/dt)_f$	V_{DD} fall rate		-	-	50	mV/μs
V_{POR}	Power-on reset detect voltage		-	-	0.2	V
V_{RAM}	RAM keep-alive voltage		1.5	-	-	V
$V_{th(HL)}$	negative-going threshold voltage	except SCL, SDA	$0.22V_{DD}$	$0.4V_{DD}$	-	V
V_{IL}	LOW-level input voltage	SCL, SDA only	-0.5	-	$0.3V_{DD}$	V
$V_{th(LH)}$	positive-going threshold voltage	except SCL, SDA	-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{IH}	HIGH-level input voltage	SCL, SDA only	$0.7V_{DD}$	-	5.5	V
V_{hys}	hysteresis voltage	Port 1	-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage; all ports, all modes except Hi-Z ^[3]	$I_{OL} = 20\text{ mA}$	-	0.6	1.0	V
		$I_{OL} = 3.2\text{ mA}$	-	0.2	0.3	V
V_{OH}	HIGH-level output voltage	$I_{OH} = -20\text{ mA}$; push-pull mode P0.3 to P0.7, P1.4, P1.6, P1.7	$0.8V_{DD}$	-	-	V
		$I_{OH} = -3.2\text{ mA}$; push-pull mode, all other ports	$V_{DD} - 0.7$	$V_{DD} - 0.4$	-	V
		$I_{OH} = -20\text{ μA}$; quasi-bidirectional mode, all ports	$V_{DD} - 0.3$	$V_{DD} - 0.2$	-	V
C_{ig}	input/output pin capacitance		[4] -	-	15	pF
I_{IL}	logical 0 input current, all ports	$V_{IN} = 0.4\text{ V}$	[5] -	-	-80	μA
I_{LI}	input leakage current, all ports	$V_{IN} = V_{IL}$ or V_{IH}	[6] -	-	±10	μA
I_{TL}	logical 1-to-0 transition current, all ports	$V_{IN} = 2.0\text{ V}$ at $V_{DD} = 3.6\text{ V}$	[7], [8] -30	-	-450	μA
R_{RST}	internal reset pull-up resistor		10	-	30	kΩ

Table 10: AC characteristics $V_{DD} = 3.0\text{ V}$ to 3.6 V unless otherwise specified. $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ for industrial, unless otherwise specified.^[1]

Symbol	Parameter	Conditions	Variable clock		$f_{osc} = 18\text{ MHz}$		Unit
			Min	Max	Min	Max	
f_{RCOSC}	internal RC oscillator frequency (nominal $f = 7.3728\text{ MHz}$)	trimmed to $\pm 1\%$ at $T_{amb} = 25\text{ }^{\circ}\text{C}$	7.189	7.557	7.189	7.557	MHz
f_{WDOSC}	internal Watchdog oscillator frequency (nominal $f = 400\text{ kHz}$)		320	520	320	520	kHz
f_{osc}	oscillator frequency	^[2]	0	18	-	-	MHz
t_{CLCL}	clock cycle	see Figure 13	55	-	-	-	ns
f_{CLKP}	CLKLP active frequency		0	8	-	-	MHz
Glitch filter							
	glitch rejection, P1.5/ $\overline{\text{RST}}$ pin		-	50	-	50	ns
	signal acceptance, P1.5/ $\overline{\text{RST}}$ pin		125	-	125	-	ns
	glitch rejection, any pin except P1.5/ $\overline{\text{RST}}$		-	15	-	15	ns
	signal acceptance, any pin except P1.5/ $\overline{\text{RST}}$		50	-	50	-	ns
External clock							
t_{CHCX}	HIGH time	see Figure 13	22	$t_{CLCL} - t_{CLCX}$	22	-	ns
t_{CLCX}	LOW time	see Figure 13	22	$t_{CLCL} - t_{CHCX}$	22	-	ns
t_{CLCH}	rise time	see Figure 13	-	5	-	5	ns
t_{CHCL}	fall time	see Figure 13	-	5	-	5	ns
Shift register (UART mode 0)							
t_{XLXL}	serial port clock cycle time		16 t_{CLCL}	-	888	-	ns
t_{QVXH}	output data set-up to clock rising edge		13 t_{CLCL}	-	722	-	ns
t_{XHGX}	output data hold after clock rising edge		-	$t_{CLCL} + 20$	-	75	ns
t_{XHDX}	input data hold after clock rising edge		-	0	-	0	ns
t_{DVXH}	input data valid to clock rising edge		150	-	150	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified. Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

[2] When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.

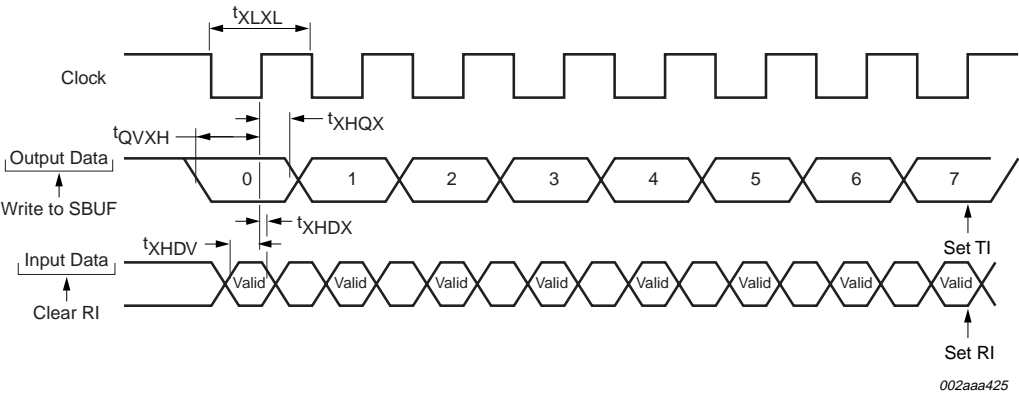


Fig 12. Shift register mode timing.

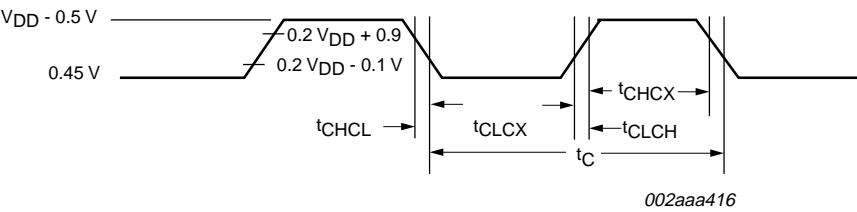


Fig 13. External clock timing.

Table 11: AC characteristics, ISP entry mode
 $V_{DD} = 2.4\text{ V to }3.6\text{ V}$, unless otherwise specified.
 $T_{amb} = -40^{\circ}\text{C to }+85^{\circ}\text{C}$ for industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VR}	$\overline{\text{RST}}$ delay from V_{DD} active		50	-	-	μs
t_{RH}	$\overline{\text{RST}}$ HIGH time		1	-	32	μs
t_{RL}	$\overline{\text{RST}}$ LOW time		1	-	-	μs

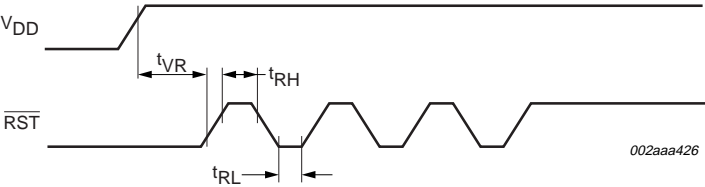


Fig 14. ISP entry waveform.

12. Comparator electrical characteristics

Table 12: Comparator electrical characteristics

$V_{DD} = 2.4\text{ V to }3.6\text{ V}$, unless otherwise specified.

$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ for industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IO}	offset voltage comparator inputs		-	-	± 20	mV
V_{CR}	common mode range comparator inputs		0	-	$V_{DD} - 0.3$	V
CMRR	common mode rejection ratio		[1] -	-	-50	dB
	response time		-	250	500	ns
	comparator enable to output valid		-	-	10	μs
I_{IL}	input leakage current, comparator	$0 < V_{IN} < V_{DD}$	-	-	± 10	μA

[1] This parameter is characterized, but not tested in production.

13. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

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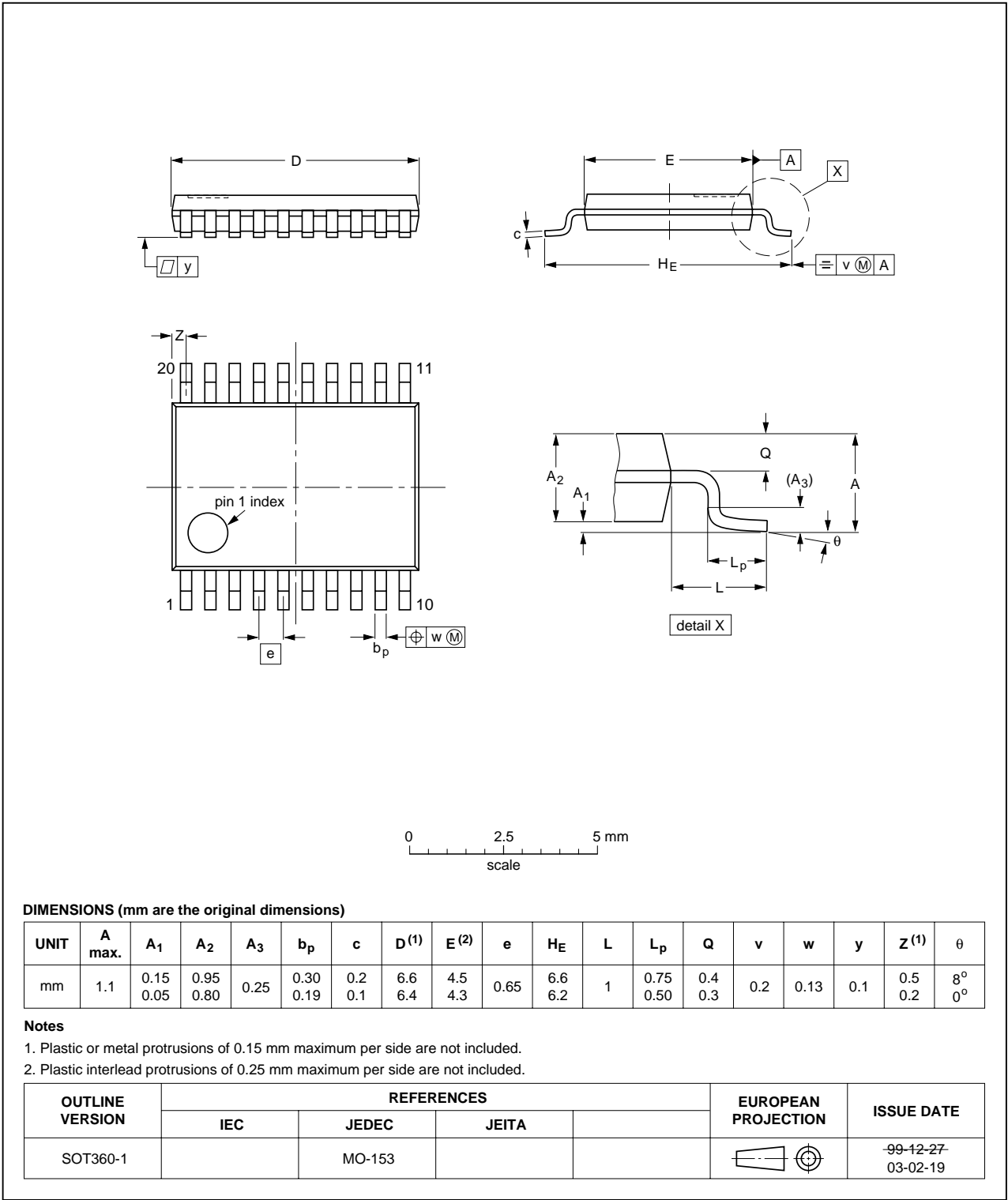


Fig 15. TSSOP20 (SOT360-1).

14. Revision history

Table 13: Revision history

Rev	Date	CPCN	Description
08	20041215	-	Product data (9397 750 14469) Modification: <ul style="list-style-type: none">• Added 18 MHz information.
07	20041203	-	Product data (9397 750 14251)
06	20031121	-	Product data (9397 750 12285); ECN 853-2403 01-A14557 of 18 November 2003
05	20031007	-	Product data (9397 750 12121); ECN 853-2403 30391 of 30 September 2003
04	20030909	-	Product data (9397 750 11945); ECN 853-2403 30305 of 5 September 2003
03	20030811	-	Preliminary data (9397 750 11786)
02	20030522	-	Objective data (9397 750 11532)
01	20030505	-	Preliminary data (9397 750 11387)