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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I <sup>2</sup> C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc921fdh-518">https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc921fdh-518</a>

## 4. Block diagram

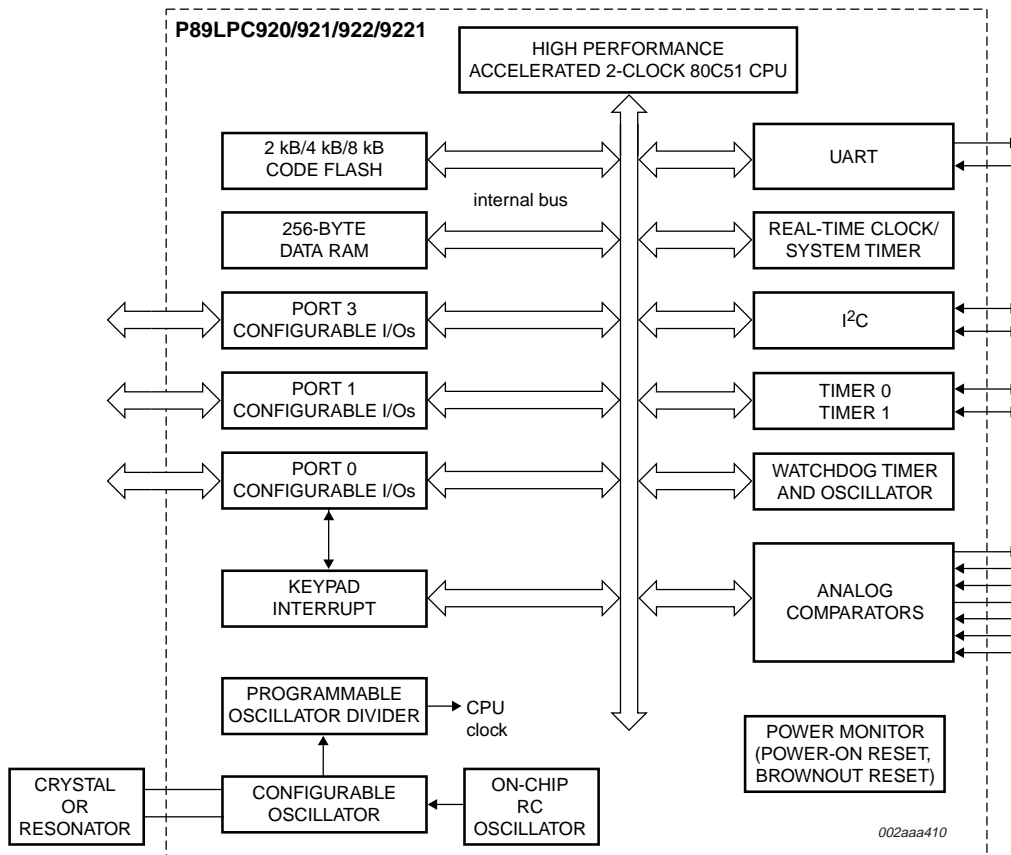


Fig 1. Block diagram.

## 5.2 Pin description

Table 3: Pin description

Symbol	Pin	Type	Description
P0.0 to P0.7		I/O	<p><b>Port 0:</b> Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to <a href="#">Section 8.12.1 “Port configurations”</a> and <a href="#">Table 8 “DC electrical characteristics”</a> for details.</p> <p>The Keypad Interrupt feature operates with Port 0 pins.</p> <p>All pins have Schmitt triggered inputs.</p> <p>Port 0 also provides various special functions as described below:</p>
1		I/O	<b>P0.0</b> — Port 0 bit 0.
		O	<b>CMP2</b> — Comparator 2 output.
		I	<b>KBI0</b> — Keyboard input 0.
20		I/O	<b>P0.1</b> — Port 0 bit 1.
		I	<b>CIN2B</b> — Comparator 2 positive input B.
		I	<b>KBI1</b> — Keyboard input 1.
19		I/O	<b>P0.2</b> — Port 0 bit 2.
		I	<b>CIN2A</b> — Comparator 2 positive input A.
		I	<b>KBI2</b> — Keyboard input 2.
18		I/O	<b>P0.3</b> — Port 0 bit 3. <b>High current source (P89LPC9221).</b>
		I	<b>CIN1B</b> — Comparator 1 positive input B.
		I	<b>KBI3</b> — Keyboard input 3.
17		I/O	<b>P0.4</b> — Port 0 bit 4. <b>High current source (P89LPC9221).</b>
		I	<b>CIN1A</b> — Comparator 1 positive input A.
		I	<b>KBI4</b> — Keyboard input 4.
16		I/O	<b>P0.5</b> — Port 0 bit 5. <b>High current source (P89LPC9221).</b>
		I	<b>CMPREF</b> — Comparator reference (negative) input.
		I	<b>KBI5</b> — Keyboard input 5.
14		I/O	<b>P0.6</b> — Port 0 bit 6. <b>High current source (P89LPC9221).</b>
		O	<b>CMP1</b> — Comparator 1 output.
		I	<b>KBI6</b> — Keyboard input 6.
13		I/O	<b>P0.7</b> — Port 0 bit 7. <b>High current source (P89LPC9221).</b>
		I/O	<b>T1</b> — Timer/counter 1 external count input or overflow output.
		I	<b>KBI7</b> — Keyboard input 7.

## 7. Special function registers

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**Remark:** Special Function Registers (SFRs) accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can **only** be written and read as follows:
  - '-' Unless otherwise specified, **must** be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' **must** be written with '0', and will return a '0' when read.
  - '1' **must** be written with '1', and will return a '1' when read.

**Table 4: Special function registers**

\* indicates SFRs that are bit addressable.

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB				LSB				Hex	Binary
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	00000000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-	DPS	00 <sup>[1]</sup>	000000x0
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	00000000
BRGR0 <sup>[2]</sup>	Baud rate generator rate LOW	BEH									00	00000000
BRGR1 <sup>[2]</sup>	Baud rate generator rate HIGH	BFH									00	00000000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00	xxxxxx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	OE1	CO1	CMF1	00 <sup>[1]</sup>	xx000000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00 <sup>[1]</sup>	xx000000
DIVM	CPU clock divide-by-M control	95H									00	00000000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer HIGH	83H									00	00000000
DPL	Data pointer LOW	82H									00	00000000
FMADRH	Program Flash address HIGH	E7H									00	00000000
FMADRL	Program Flash address LOW	E6H									00	00000000
FMCON	Program Flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	01110000
	Program Flash control (Write)	E4H	FMCMD. 7	FMCMD. 6	FMCMD. 5	FMCMD. 4	FMCMD. 3	FMCMD. 2	FMCMD. 1	FMCMD. 0		
FMDATA	Program Flash data	E5H									00	00000000
I2ADR	I <sup>2</sup> C slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	00000000
		Bit address	DF	DE	DD	DC	DB	DA	D9	D8		
I2CON*	I <sup>2</sup> C control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x00000x0
I2DAT	I <sup>2</sup> C data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register HIGH	DDH									00	00000000

**Table 4: Special function registers...continued**

\* indicates SFRs that are bit addressable.

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB								Hex	Binary
I2SCLL	Serial clock generator/SCL duty cycle register LOW	DCH									00	00000000
I2STAT	I <sup>2</sup> C status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0	0	F8	11111000
Bit address			AF	AE	AD	AC	AB	AA	A9	A8		
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	EX1	ET0	EX0	00 <sup>[1]</sup>	00000000
Bit address			EF	EE	ED	EC	EB	EA	E9	E8		
IEN1*	Interrupt enable 1	E8H	-	EST	-	-	-	EC	EKBI	EI2C	00 <sup>[1]</sup>	00x00000
Bit address			BF	BE	BD	BC	BB	BA	B9	B8		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	PX1	PT0	PX0	00 <sup>[1]</sup>	x0000000
IP0H	Interrupt priority 0 HIGH	B7H	-	PWDRT H	PBOH	PSH/ PSRH	PT1H	PX1H	PT0H	PX0H	00 <sup>[1]</sup>	x0000000
Bit address			FF	FE	FD	FC	FB	FA	F9	F8		
IP1*	Interrupt priority 1	F8H	-	PST	-	-	-	PC	PKBI	PI2C	00 <sup>[1]</sup>	00x00000
IP1H	Interrupt priority 1 HIGH	F7H	-	PSTH	-	-	-	PCH	PKBIH	PI2CH	00 <sup>[1]</sup>	00x00000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN _SEL	KBIF	00 <sup>[1]</sup>	xxxxxx00
KBMASK	Keypad interrupt mask register	86H									00	00000000
KBPATN	Keypad pattern register	93H									FF	11111111
Bit address			87	86	85	84	83	82	81	80		
P0*	Port 0	80H	T1/KB7	CMP1 /KB6	CMPREF /KB5	CIN1A /KB4	CIN1B /KB3	CIN2A /KB2	CIN2B /KB1	CMP2 /KB0		<sup>[1]</sup>
Bit address			97	96	95	94	93	92	91	90		
P1*	Port 1	90H	-	-	RST	INT1	INT0/ SDA	T0/SCL	RXD	TXD		<sup>[1]</sup>
Bit address			B7	B6	B5	B4	B3	B2	B1	B0		
P3*	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2		<sup>[1]</sup>
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF	11111111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00	00000000
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3 <sup>[1]</sup>	11x1xx11

## 8. Functional description

**Remark:** Please refer to the *P89LPC920/921/922/9221 User's Manual* for a more detailed functional description.

### 8.1 Enhanced CPU

The P89LPC920/921/922/9221 uses an enhanced 80C51 CPU which runs at 6 times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

### 8.2 Clocks

#### 8.2.1 Clock definitions

The P89LPC920/921/922/9221 device has several internal clocks as defined below:

**OSCCLK** — Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see Figure 5) and can also be optionally divided to a slower frequency (see Section 8.7 “CPU Clock (CCLK) modification: DIVM register”).

**Note:**  $f_{osc}$  is defined as the OSCCLK frequency.

**CCLK** — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

**RCCLK** — The internal 7.373 MHz RC oscillator output.

**PCLK** — Clock for the various peripheral devices and is CCLK/2

#### 8.2.2 CPU clock (OSCCLK)

The P89LPC920/921/922/9221 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the FLASH is programmed and include an on-chip watchdog oscillator, an on-chip RC oscillator, an oscillator using an external crystal, or an external clock source. The crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 12 MHz.

#### 8.2.3 Low speed oscillator option

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

#### 8.2.4 Medium speed oscillator option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

#### 8.2.5 High speed oscillator option

This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until  $V_{DD}$  has reached its specified level. When system power is removed  $V_{DD}$  will fall below**

**8.16.3 Mode 2**

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

**8.16.4 Mode 3**

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

**8.16.5 Mode 6**

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

**8.16.6 Timer overflow toggle output**

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

**8.17 Real-Time clock/system timer**

The P89LPC920/921/922/9221 has a simple Real-Time clock that allows a user to continue running an accurate timer while the rest of the device is powered-down. The Real-Time clock can be a wake-up or an interrupt source. The Real-Time clock is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all '0's, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator, provided that the XTAL oscillator is not being used as the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source. Only power-on reset will reset the Real-Time clock and its associated SFRs to the default state.

**8.18 UART**

The P89LPC920/921/922/9221 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC920/921/922/9221 does include an independent Baud Rate Generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in 4 modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16.

**8.18.1 Mode 0**

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at  $\frac{1}{16}$  of the CPU clock frequency.



### 8.18.2 Mode 1

10 bits are transmitted (through TxD) or received (through RxD): a start bit (logical '0'), 8 data bits (LSB first), and a stop bit (logical '1'). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in [Section 8.18.5 "Baud rate generator and selection"](#)).

### 8.18.3 Mode 2

11 bits are transmitted (through TxD) or received (through RxD): start bit (logical '0'), 8 data bits (LSB first), a programmable 9<sup>th</sup> data bit, and a stop bit (logical '1'). When data is transmitted, the 9<sup>th</sup> data bit (TB8 in SCON) can be assigned the value of '0' or '1'. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9<sup>th</sup> data bit goes into RB8 in Special Function Register SCON, while the stop bit is not saved. The baud rate is programmable to either  $\frac{1}{16}$  or  $\frac{1}{32}$  of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

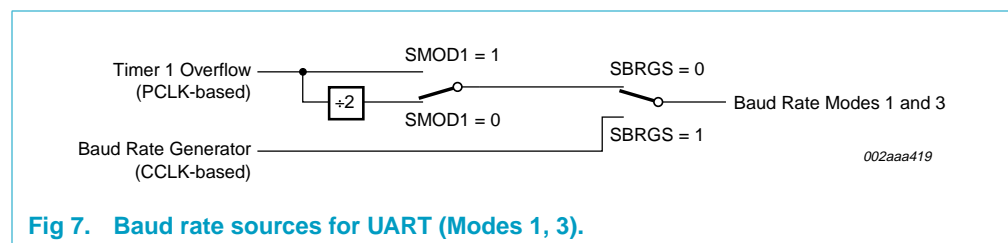
### 8.18.4 Mode 3

11 bits are transmitted (through TxD) or received (through RxD): a start bit (logical '0'), 8 data bits (LSB first), a programmable 9<sup>th</sup> data bit, and a stop bit (logical '1'). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in [Section 8.18.5 "Baud rate generator and selection"](#)).

### 8.18.5 Baud rate generator and selection

The P89LPC920/921/922/9221 enhanced UART has an independent Baud Rate Generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1 and BRGR0 SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1 but is much more accurate. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UART can use either Timer 1 or the baud rate generator output (see [Figure 7](#)). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is set. The independent Baud Rate Generator uses OSCCLK.



**Fig 7. Baud rate sources for UART (Modes 1, 3).**

### 8.18.6 Framing error

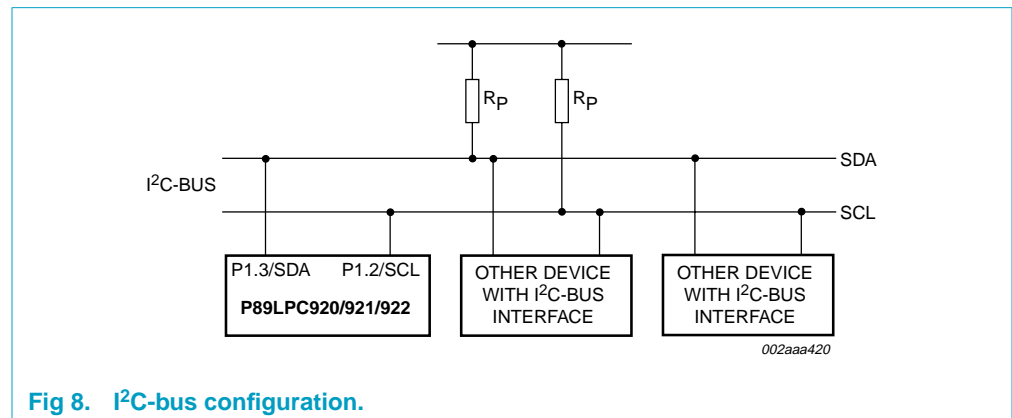
Framing error is reported in the status register (SSTAT). In addition, if SMOD0 (PCON.6) is '1', framing errors can be made available in SCON.7 respectively. If SMOD0 is '0', SCON.7 is SM0. It is recommended that SM0 and SM1 (SCON.7:6) are set up when SMOD0 is '0'.

### 8.19 I<sup>2</sup>C-bus serial interface

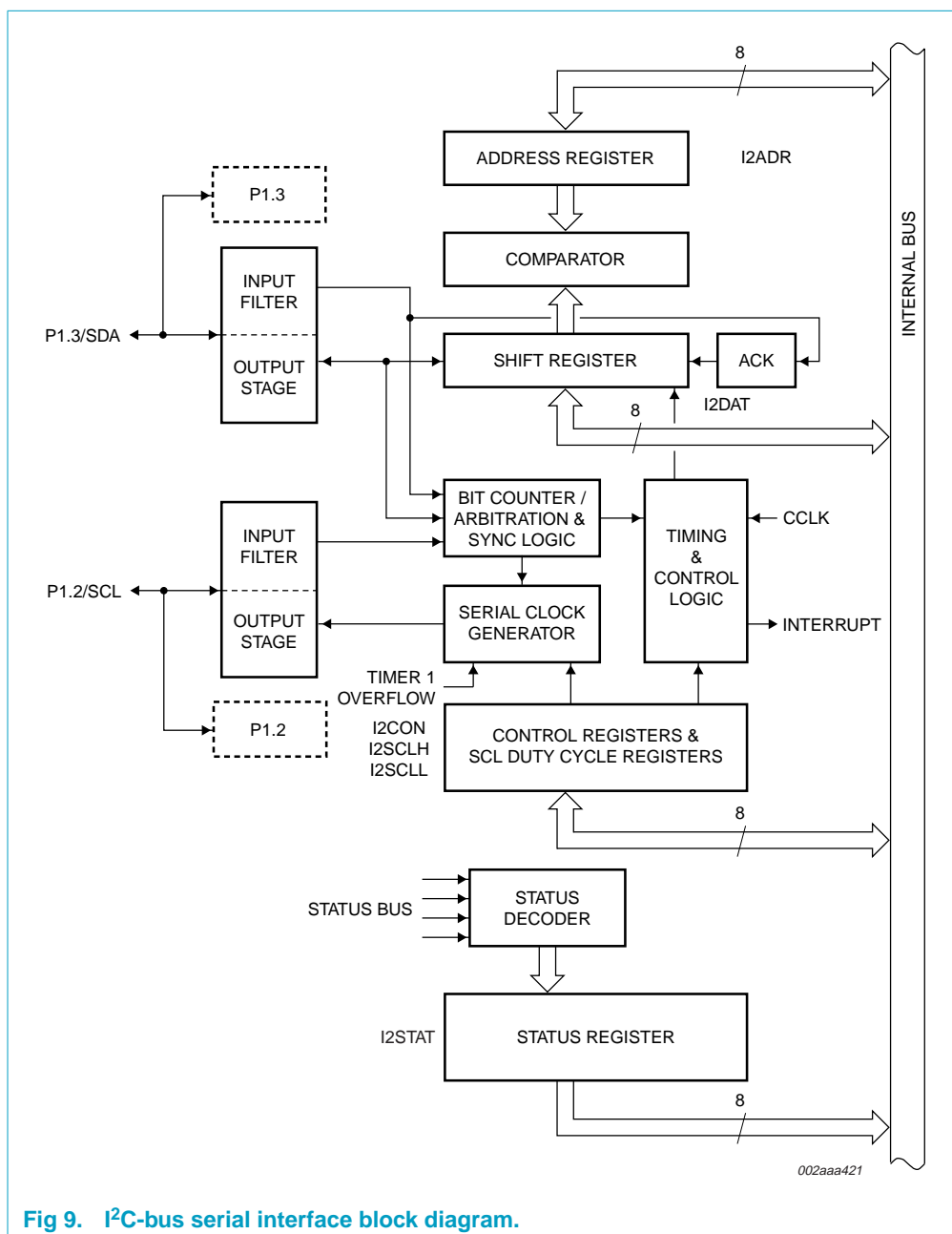
I<sup>2</sup>C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between masters and slaves
- Multimaster bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I<sup>2</sup>C-bus may be used for test and diagnostic purposes.

A typical I<sup>2</sup>C-bus configuration is shown in **Figure 8**. The P89LPC920/921/922/9221 device provides a byte-oriented I<sup>2</sup>C-bus interface that supports data transfers up to 400 kHz.



**Fig 8. I<sup>2</sup>C-bus configuration.**



**Fig 9. I²C-bus serial interface block diagram.**

## 8.20 Analog comparators

Two analog comparators are provided on the P89LPC920/921/922/9221. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logical one (which may be read in a register and/or routed to a pin) when the positive input (one of two selectable pins) is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes.

The overall connections to both comparators are shown in Figure 10. The comparators function to  $V_{DD} = 2.4$  V.

When each comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 microseconds. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

When a comparator is disabled the comparator's output, COx, goes HIGH. If the comparator output was LOW and then is disabled, the resulting transition of the comparator output from a LOW to HIGH state will set the comparator flag, CMFx. This will cause an interrupt if the comparator interrupt is enabled. The user should therefore disable the comparator interrupt prior to disabling the comparator. Additionally, the user should clear the comparator flag, CMFx, after disabling the comparator.

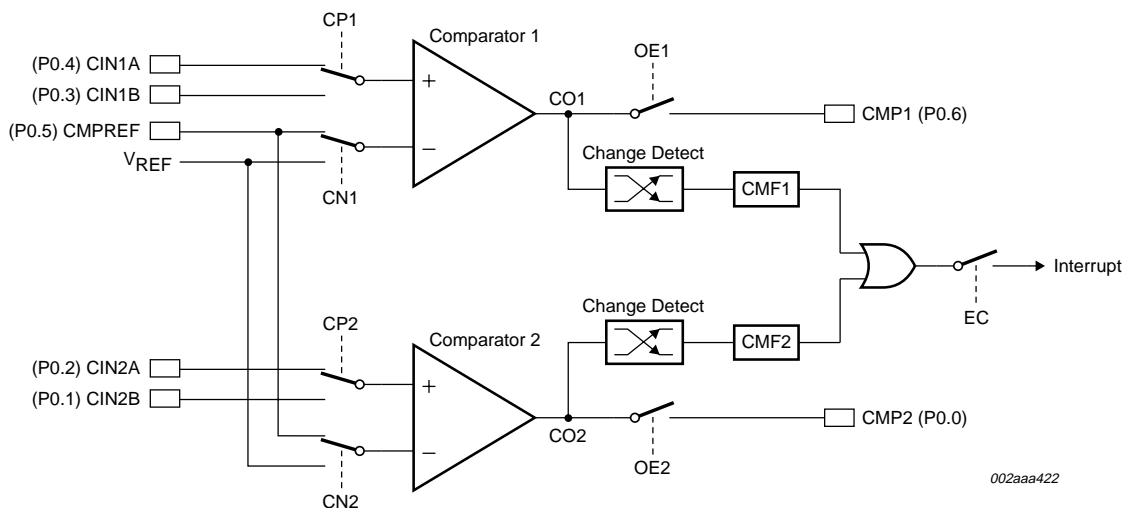


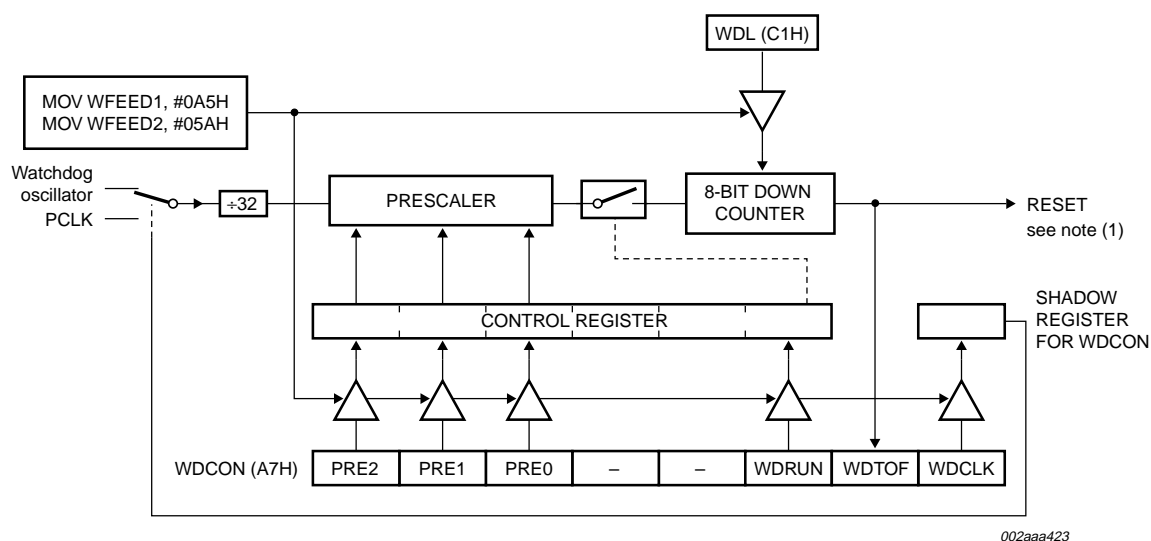
Fig 10. Comparator input and output connections.

### 8.20.1 Internal reference voltage

An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as  $V_{REF}$ , is  $1.23\text{ V} \pm 10\%$ .

## 8.22 Watchdog timer

The Watchdog timer causes a system reset when it underflows as a result of a failure to feed the timer prior to the timer reaching its terminal count. It consists of a programmable 12-bit prescaler, and an 8-bit down counter. The down counter is decremented by a tap taken from the prescaler. The clock source for the prescaler is either the PCLK or the nominal 400 kHz Watchdog oscillator. The Watchdog timer can only be reset by a power-on reset. When the watchdog feature is disabled, it can be used as an interval timer and may generate an interrupt. Figure 11 shows the Watchdog timer in watchdog mode. Feeding the watchdog requires a two-byte sequence. If PCLK is selected as the watchdog clock and the CPU is powered-down, the watchdog is disabled. The Watchdog timer has a time-out period that ranges from a few  $\mu$ s to a few seconds. Please refer to the *P89LPC920/921/922/9221 User's Manual* for more details.



(1) Watchdog reset can also be caused by an invalid feed sequence, or by writing to WDCON not immediately followed by a feed sequence.

Fig 11. Watchdog timer in watchdog mode (WDTE = '1').

## 8.23 Additional features

### 8.23.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

### 8.23.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic '0' so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

## 9. Limiting values

**Table 7: Limiting values**<sup>[1]</sup>

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T <sub>amb(bias)</sub>	operating bias ambient temperature		−55	+125	°C
T <sub>stg</sub>	storage temperature range		−65	+150	°C
V <sub>xtal</sub>	voltage on XTAL1, XTAL2 pin to V <sub>SS</sub>		-	V <sub>DD</sub> + 0.5	V
V <sub>n</sub>	voltage on any other pin to V <sub>SS</sub>		−0.5	+5.5	V
I <sub>OH(I/O)</sub>	HIGH-level output current per I/O pin, P89LPC9221	P0.3 to P0.7, P1.4, P1.6, P1.7	-	20	mA
		all other I/O pins	-	8	mA
	HIGH-level output current per I/O pin, P89LPC920/921/922		-	8	mA
I <sub>OL(I/O)</sub>	LOW-level output current per I/O pin		-	20	mA
I <sub>I/O(tot)(max)</sub>	maximum total I/O current, P89LPC9221		-	160	mA
	maximum total I/O current, P89LPC920/921/922		-	80	mA
P <sub>tot(pack)</sub>	total power dissipation per package	based on package heat transfer, not device power consumption	-	1.5	W

[1] The following applies to Limiting values:

- Stresses above those listed under [Table 7](#) may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in [Table 8 “DC electrical characteristics”](#), [Table 9 “AC characteristics”](#) and [Table 10 “AC characteristics”](#) of this specification are not implied.
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
- Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V<sub>SS</sub> unless otherwise noted.

**Table 8:** DC electrical characteristics...continued $V_{DD} = 2.4 \text{ V}$  to  $3.6 \text{ V}$  unless otherwise specified. $T_{amb} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  for industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$V_{BO}$	brownout trip voltage with BOV = '0', BOPD = '1'	$2.4 \text{ V} < V_{DD} < 3.6 \text{ V}$	2.40	-	2.70	V
$V_{REF}$	bandgap reference voltage		1.11	1.23	1.34	V
$TC_{(V_{REF})}$	bandgap temperature coefficient		-	10	20	ppm/ $^\circ\text{C}$

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] The  $I_{DD(oper)}$ ,  $I_{DD(idle)}$ , and  $I_{DD(PD)}$  specifications are measured using an external clock with the following functions disabled: comparators, brownout detect, and Watchdog timer.

[3] See Table 7 "Limiting values<sup>[1]</sup>" on page 35 for steady state (non-transient) limits on  $I_{OL}$  or  $I_{OH}$ . If  $I_{OL}/I_{OH}$  exceeds the test condition,  $V_{OL}/V_{OH}$  may exceed the related specification.

[4] Pin capacitance is characterized but not tested.

[5] Measured with port in quasi-bidirectional mode.

[6] Measured with port in high-impedance mode.

[7] Ports in quasi-bidirectional mode with weak pull-up (applies to all port pins with pull-ups). Does not apply to open-drain pins.

[8] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from '1' to '0'. This current is highest when  $V_{IN}$  is approximately 2 V.

## 11. Dynamic characteristics

**Table 9: AC characteristics**

$V_{DD} = 2.4\text{ V}$  to  $3.6\text{ V}$  unless otherwise specified.

$T_{amb} = -40\text{ °C}$  to  $+85\text{ °C}$  for industrial, unless otherwise specified.<sup>[1]</sup>

Symbol	Parameter	Conditions	Variable clock		$f_{osc} = 12\text{ MHz}$		Unit
			Min	Max	Min	Max	
$f_{RCOSC}$	internal RC oscillator frequency (nominal $f = 7.3728\text{ MHz}$ )	trimmed to $\pm 1\%$ at $T_{amb} = 25\text{ °C}$	7.189	7.557	7.189	7.557	MHz
$f_{WDOSC}$	internal Watchdog oscillator frequency (nominal $f = 400\text{ kHz}$ )		320	520	320	520	kHz
$f_{osc}$	oscillator frequency		0	12	-	-	MHz
$t_{CLCL}$	clock cycle	see Figure 13	83	-	-	-	ns
$f_{CLKP}$	CLKLP active frequency		0	8	-	-	MHz
<b>Glitch filter</b>							
	glitch rejection, P1.5/ $\overline{RST}$ pin		-	50	-	50	ns
	signal acceptance, P1.5/ $\overline{RST}$ pin		125	-	125	-	ns
	glitch rejection, any pin except P1.5/ $\overline{RST}$		-	15	-	15	ns
	signal acceptance, any pin except P1.5/ $\overline{RST}$		50	-	50	-	ns
<b>External clock</b>							
$t_{CHCX}$	HIGH time	see Figure 13	33	$t_{CLCL} - t_{CLCX}$	33	-	ns
$t_{CLCX}$	LOW time	see Figure 13	33	$t_{CLCL} - t_{CHCX}$	33	-	ns
$t_{CLCH}$	rise time	see Figure 13	-	8	-	8	ns
$t_{CHCL}$	fall time	see Figure 13	-	8	-	8	ns
<b>Shift register (UART mode 0)</b>							
$t_{XLXL}$	serial port clock cycle time		$16\ t_{CLCL}$	-	1333	-	ns
$t_{QVXH}$	output data set-up to clock rising edge		$13\ t_{CLCL}$	-	1083	-	ns
$t_{XHGX}$	output data hold after clock rising edge		-	$t_{CLCL} + 20$	-	103	ns
$t_{XHDX}$	input data hold after clock rising edge		-	0	-	0	ns
$t_{DVXH}$	input data valid to clock rising edge		150	-	150	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified. Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.



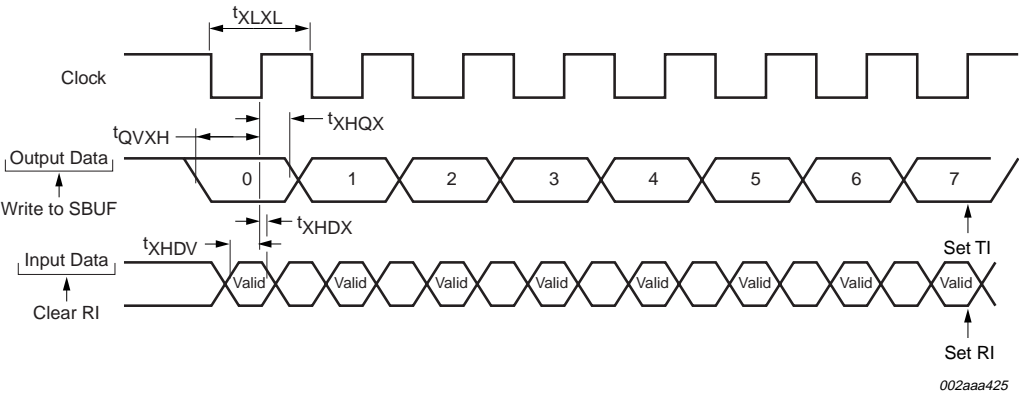


Fig 12. Shift register mode timing.

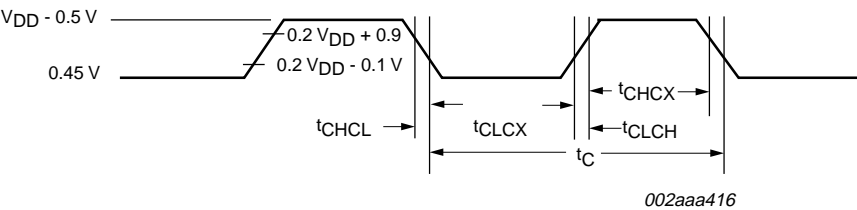


Fig 13. External clock timing.

Table 11: AC characteristics, ISP entry mode  
 $V_{DD} = 2.4 V$  to  $3.6 V$ , unless otherwise specified.  
 $T_{amb} = -40^{\circ}C$  to  $+85^{\circ}C$  for industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{VR}$	RST delay from $V_{DD}$ active		50	-	-	$\mu s$
$t_{RH}$	RST HIGH time		1	-	32	$\mu s$
$t_{RL}$	RST LOW time		1	-	-	$\mu s$

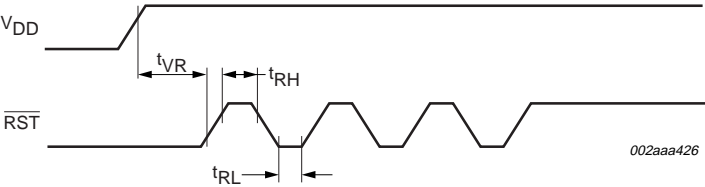


Fig 14. ISP entry waveform.

## 12. Comparator electrical characteristics

**Table 12: Comparator electrical characteristics**

$V_{DD} = 2.4\text{ V to }3.6\text{ V}$ , unless otherwise specified.

$T_{amb} = -40\text{ °C to }+85\text{ °C}$  for industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IO}$	offset voltage comparator inputs		-	-	$\pm 20$	mV
$V_{CR}$	common mode range comparator inputs		0	-	$V_{DD} - 0.3$	V
CMRR	common mode rejection ratio		[1] -	-	-50	dB
	response time		-	250	500	ns
	comparator enable to output valid		-	-	10	$\mu\text{s}$
$I_{IL}$	input leakage current, comparator	$0 < V_{IN} < V_{DD}$	-	-	$\pm 10$	$\mu\text{A}$

[1] This parameter is characterized, but not tested in production.

## 14. Revision history

Table 13: Revision history

Rev	Date	CPCN	Description
08	20041215	-	<b>Product data (9397 750 14469)</b> Modification: <ul style="list-style-type: none"><li>• Added 18 MHz information.</li></ul>
07	20041203	-	<b>Product data (9397 750 14251)</b>
06	20031121	-	<b>Product data (9397 750 12285); ECN 853-2403 01-A14557 of 18 November 2003</b>
05	20031007	-	<b>Product data (9397 750 12121); ECN 853-2403 30391 of 30 September 2003</b>
04	20030909	-	<b>Product data (9397 750 11945); ECN 853-2403 30305 of 5 September 2003</b>
03	20030811	-	<b>Preliminary data (9397 750 11786)</b>
02	20030522	-	<b>Objective data (9397 750 11532)</b>
01	20030505	-	<b>Preliminary data (9397 750 11387)</b>

## 15. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2][3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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