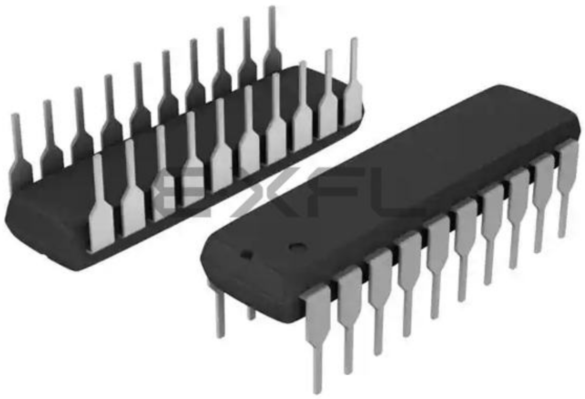


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-DIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc921fn-112

2.2 Additional features

- 15 I/O pins minimum. Up to 18 I/O pins while using on-chip oscillator and reset options.
- 20-pin TSSOP and DIP packages.
- A high performance 80C51 CPU provides instruction cycle times of 111 ns to 222 ns for all instructions except multiply and divide when executing at 18 MHz. This is six times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.
- In-Application Programming of the Flash code memory. This allows changing the code in a running application.
- Serial Flash programming allows simple in-circuit production coding. Flash security bits prevent reading of sensitive application programs.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog prescaler is selectable from eight values.
- Low voltage reset (Brownout detect) allows a graceful system shutdown when power fails. May optionally be configured as an interrupt.
- Idle and two different Power-down reduced power modes. Improved wake-up from Power-down mode (a low interrupt input starts execution). Typical Power-down current is 1 μA (total Power-down with voltage comparators disabled).
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets. A software reset function is also available.
- Oscillator Fail Detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Programmable port output configuration options:
  - quasi-bidirectional,
  - open drain,
  - push-pull,
  - input-only.
- Port 'input pattern match' detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- LED drive capability (20 mA) on all port pins. A maximum limit is specified for the entire chip (160 mA for the P89LPC9221; 80 mA for the P89LPC920/921/922).
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC920/921/922/9221 when internal reset option is selected.
- Four interrupt priority levels.
- Eight keypad interrupt inputs, plus two additional external interrupt inputs.
- Second data pointer.
- Schmitt trigger port inputs.
- Emulation support.

3. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
P89LPC920FDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
P89LPC921FDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
P89LPC922FDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
P89LPC922FN	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
P89LPC9221FN	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
P89LPC9221FDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

3.1 Ordering options

Table 2: Part options

Type number	Flash memory	Temperature range	Frequency
P89LPC920FDH	2 kB	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC921FDH	4 kB	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC922FDH	8 kB	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC922FN	8 kB	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC9221FN	8 kB	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC9221FDH	8 kB	–40 °C to +85 °C	0 MHz to 18 MHz

5.2 Pin description

Table 3: Pin description

Symbol	Pin	Type	Description
P0.0 to P0.7		I/O	**Port 0:** Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 8 "DC electrical characteristics" for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
	1	I/O	**P0.0 —** Port 0 bit 0.
		O	**CMP2 —** Comparator 2 output.
		I	**KBI0 —** Keyboard input 0.
	20	I/O	**P0.1 —** Port 0 bit 1.
		I	**CIN2B —** Comparator 2 positive input B.
		I	**KBI1 —** Keyboard input 1.
	19	I/O	**P0.2 —** Port 0 bit 2.
		I	**CIN2A —** Comparator 2 positive input A.
		I	**KBI2 —** Keyboard input 2.
	18	I/O	**P0.3 —** Port 0 bit 3. **High current source (P89LPC9221).**
		I	**CIN1B —** Comparator 1 positive input B.
		I	**KBI3 —** Keyboard input 3.
	17	I/O	**P0.4 —** Port 0 bit 4. **High current source (P89LPC9221).**
		I	**CIN1A —** Comparator 1 positive input A.
		I	**KBI4 —** Keyboard input 4.
	16	I/O	**P0.5 —** Port 0 bit 5. **High current source (P89LPC9221).**
		I	**CMPREF —** Comparator reference (negative) input.
		I	**KBI5 —** Keyboard input 5.
	14	I/O	**P0.6 —** Port 0 bit 6. **High current source (P89LPC9221).**
		O	**CMP1 —** Comparator 1 output.
		I	**KBI6 —** Keyboard input 6.
	13	I/O	**P0.7 —** Port 0 bit 7. **High current source (P89LPC9221).**
		I/O	**T1 —** Timer/counter 1 external count input or overflow output.
		I	**KBI7 —** Keyboard input 7.

Table 3: Pin description *…continued*

Symbol	Pin	Type	Description
P3.0 to P3.1		I/O	**Port 3:** Port 3 is an 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 8 "DC electrical characteristics" for details. All pins have Schmitt triggered inputs. Port 3 also provides various special functions as described below:
	7	I/O	**P3.0 —** Port 3 bit 0.
		O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the FLASH configuration.
		O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the real time clock/system timer.
	6	I/O	**P3.1 —** Port 3 bit 1.
		I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the FLASH configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the real time clock/system timer.
V_{SS}	5	I	**Ground:** 0 V reference.
V_{DD}	15	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power down modes.

[1] Input/Output for P1.0-P1.4, P1.6, P1.7. Input for P1.5.

6. Logic symbol

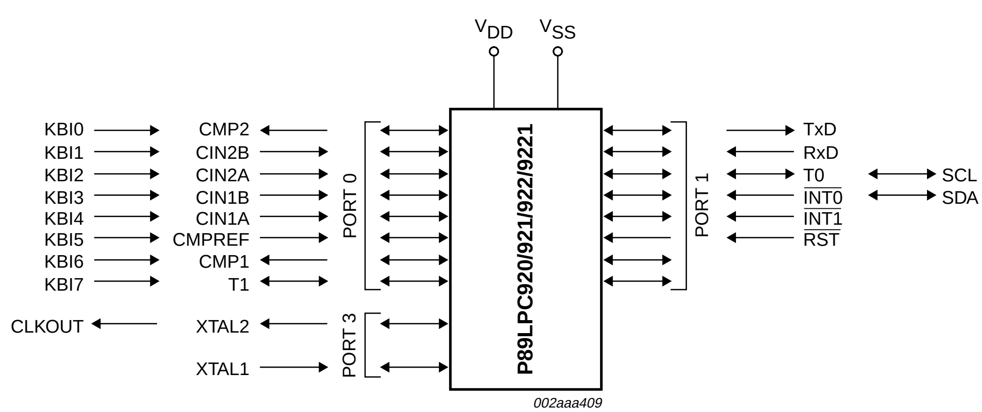


Fig 4. Logic symbol.

Table 4: Special function registers...*continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00[1]	00x0xx00
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03[1]	xxxxxx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00[1]	xxxxxx00
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	00000000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	-	I2PD	-	SPD	-	00[1]	00000000
		Bit address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00H	00000000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00H	xx00000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX		[3]
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[1][6]	
RTCH	Real-time clock register HIGH	D2H									00[6]	00000000
RTCL	Real-time clock register LOW	D3H									00[6]	00000000
SADDR	Serial port address register	A9H									00	00000000
SADEN	Serial port address enable	B9H									00	00000000
SBUF	Serial Port data buffer register	99H									xx	xxxxxxxx
		Bit address	**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	00000000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	00000000
SP	Stack pointer	81H									07	00000111
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0xxx0
		Bit address	**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	00000000
TH0	Timer 0 HIGH	8CH									00	00000000
TH1	Timer 1 HIGH	8DH									00	00000000
TL0	Timer 0 LOW	8AH									00	00000000
TL1	Timer 1 LOW	8BH									00	00000000
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	00000000

Table 4: Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
TRIM	Internal oscillator trim register	96H	-	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[5] [6]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[4] [6]	
WDL	Watchdog load	C1H									FF	11111111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] All ports are in input only (high impedance) state after power-up.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is ‘0’. If any are written while BRGEN = 1, the result is unpredictable.

[3] The RSTSRC register reflects the cause of the P89LPC920/921/922/9221 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx110000.

[4] After reset, the value is 111001x1, i.e., PRE2-PRE0 are all ‘1’, WDRUN = 1 and WDCLK = 1. WDTOF bit is ‘1’ after watchdog reset and is ‘0’ after power-on reset. Other resets will not affect WDTOF.

[5] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6] The only reset source that affects these SFRs is power-on reset.

8. Functional description

Remark: Please refer to the *P89LPC920/921/922/9221 User's Manual* for a more detailed functional description.

8.1 Enhanced CPU

The P89LPC920/921/922/9221 uses an enhanced 80C51 CPU which runs at 6 times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

8.2 Clocks

8.2.1 Clock definitions

The P89LPC920/921/922/9221 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see Figure 5) and can also be optionally divided to a slower frequency (see Section 8.7 "CPU Clock (CCLK) modification: DIVM register").

Note: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output.

PCLK — Clock for the various peripheral devices and is CCLK/2

8.2.2 CPU clock (OSCCLK)

The P89LPC920/921/922/9221 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the FLASH is programmed and include an on-chip watchdog oscillator, an on-chip RC oscillator, an oscillator using an external crystal, or an external clock source. The crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 12 MHz.

8.2.3 Low speed oscillator option

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

8.2.4 Medium speed oscillator option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

8.2.5 High speed oscillator option

This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below**

the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.

8.2.6 Clock output

The P89LPC920/921/922/9221 supports a user-selectable clock output function on the XTAL2/CLKOUT pin when crystal oscillator is not being used. This condition occurs if another clock source has been selected (on-chip RC oscillator, watchdog oscillator, external clock input on X1) and if the Real-Time clock is not using the crystal oscillator as its clock source. This allows external devices to synchronize to the P89LPC920/921/922/9221. This output is enabled by the ENCLK bit in the TRIM register. The frequency of this clock output is $\frac{1}{2}$ that of the CCLK. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power.

8.3 On-chip RC oscillator option

The P89LPC920/921/922/9221 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory pre-programmed value to adjust the oscillator frequency to 7.373 MHz, ±1% at room temperature. End-user applications can write to the Trim register to adjust the on-chip RC oscillator to other frequencies.

8.4 Watchdog oscillator option

The watchdog has a separate oscillator which has a frequency of 400 kHz. This oscillator can be used to save power when a high clock frequency is not needed.

8.5 External clock input option

In this configuration, the processor clock is derived from an external source driving the XTAL1/P3.1 pin. The rate may be from 0 Hz up to 12 MHz. The XTAL2/P3.0 pin may be used as a standard port pin or a clock output. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**

8.6 CPU Clock (CCLK) wake-up delay

The P89LPC920/921/922/9221 has an internal wake-up timer that delays the clock until it stabilizes depending to the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 992 OSCCLK cycles plus 60 to 100 µs. If the clock source is either the internal RC oscillator, watchdog oscillator, or external clock, the delay is 224 OSCCLK cycles plus 60 to 100 µs.

8.7 CPU Clock (CCLK) modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

8.8 Low power select

The P89LPC920/921/922/9221 is designed to run at 18 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to ‘1’ to lower the power consumption further. On any reset, CLKLP is ‘0’ allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

8.9 Memory organization

The various P89LPC920/921/922/9221 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00h:7Fh) accessed via direct or indirect addressing, using instruction other than MOVX and MOVC. All or part of the Stack may be in this area.

- IDATA

  Indirect Data. 256 bytes of internal data memory space (00h:FFh) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC920/921/922/9221 has 2 kB/4 kB/8 kB of on-chip Code memory.

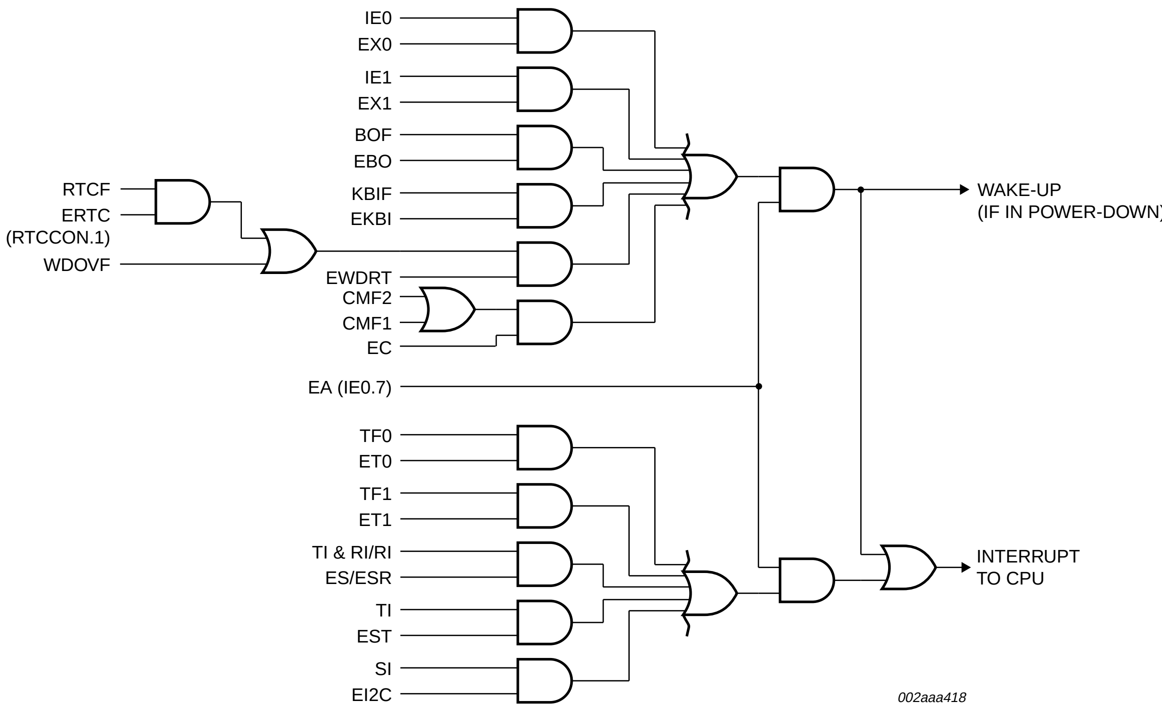


Fig 6. Interrupt sources, interrupt enables, and power-down wake-up sources.

8.12 I/O ports

The P89LPC920/921/922/9221 has three I/O ports: Port 0, Port 1, and Port 3. Ports 0 and 1 are 8-bit ports, and Port 3 is a 2-bit port. The exact number of I/O pins available depend upon the clock and reset options chosen, as shown in Table 6.

Table 6: Number of I/O pins available

Clock source	Reset option	Number of I/O pins (20-pin package)
On-chip oscillator or watchdog oscillator	No external reset (except during power-up)	18
	External $\overline{RST}$ pin supported[1]	17
External clock input	No external reset (except during power-up)	17
	External $\overline{RST}$ pin supported[1]	16
Low/medium/high speed oscillator (external crystal or resonator)	No external reset (except during power-up)	16
	External $\overline{RST}$ pin supported[1]	15

[1] Required for operation above 12 MHz.

8.12.1 Port configurations

All but three I/O port pins on the P89LPC920/921/922/9221 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

P1.5 ($\overline{RST}$) can only be an input and cannot be configured.

8.12.7 Additional port features

After power-up, all pins are in Input-Only mode. **Please note that this is different from the LPC76x series of devices.**

- After power-up, all I/O pins except P1.5, may be configured by software.
- Pin P1.5 is input only. Pins P1.2 and P1.3 and are configurable for either input-only or open-drain.

Every output on the P89LPC920/921/922/9221 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to Table 8 “DC electrical characteristics” for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

8.13 Power monitoring functions

The P89LPC920/921/922/9221 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on Detect and Brownout detect.

8.13.1 Brownout detection

The Brownout detect function determines if the power supply voltage drops below a certain level. The default operation is for a Brownout detection to cause a processor reset, however it may alternatively be configured to generate an interrupt.

Brownout detection may be enabled or disabled in software.

If Brownout detection is enabled, the brownout condition occurs when V_{DD} falls below the brownout trip voltage, V_{BO} (see Table 8 “DC electrical characteristics”), and is negated when V_{DD} rises above V_{BO}. If the P89LPC920/921/922/9221 device is to operate with a power supply that can be below 2.7 V, BOE should be left in the unprogrammed state so that the device can operate at 2.4 V, otherwise continuous brownout reset may prevent the device from operating.

For correct activation of Brownout detect, the V_{DD} rise and fall times must be observed. Please see Table 8 “DC electrical characteristics” for specifications.

8.13.2 Power-on detection

The Power-on Detect has a function similar to the Brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where Brownout detect can work. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

8.14 Power reduction modes

The P89LPC920/921/922/9221 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and total Power-down mode.

8.14.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

8.14.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC920/921/922/9221 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the RAM keep-alive voltage V_{RAM}. This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{RAM}, therefore it is highly recommended to wake up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during Power-down. These include: Brownout detect, Watchdog Timer, Comparators (note that Comparators can be powered-down separately), and Real-Time Clock (RTC)/System Timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock AND the RTC is enabled.

8.14.3 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock the RTC during Power-down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the Real-Time Clock running during Power-down.

8.15 Reset

The P1.5/$\overline{RST}$ pin can function as either an active-LOW reset input or as a digital input, P1.5. The RPE (Reset Pin Enable) bit in UCFG1, when set to ‘1’, enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, the RPE selection is overridden and this pin will always function as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this input will function either as an external reset input or as a digital input as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit.

Remark: During a power cycle, V_{DD} must fall below V_{POR} (see Table 8 “DC electrical characteristics” on page 36) before power is reapplied, in order to ensure a power-on reset.

Reset can be triggered from the following sources:

8.19 I²C-bus serial interface

I²C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between masters and slaves
- Multimaster bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I²C-bus may be used for test and diagnostic purposes.

A typical I²C-bus configuration is shown in Figure 8. The P89LPC920/921/922/9221 device provides a byte-oriented I²C-bus interface that supports data transfers up to 400 kHz.

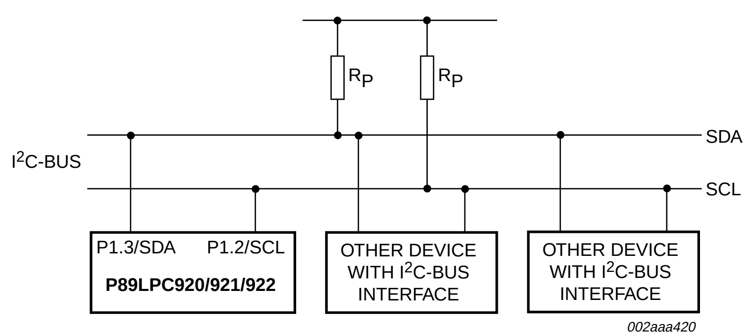


Fig 8. I²C-bus configuration.

8.24 Flash program memory

8.24.1 General description

The P89LPC920/921/922/9221 Flash memory provides in-circuit electrical erasure and programming. The Flash can be read, erased, or written as bytes. The Sector and Page Erase functions can erase any Flash sector (1 kB) or page (64 bytes). The Chip Erase operation will erase the entire program memory. In-System Programming and standard parallel programming are both available. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC920/921/922/9221 Flash reliably stores memory contents even after 10,000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC920/921/922/9221 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms.

8.24.2 Features

- Parallel programming with industry-standard commercial programmers.
- In-Circuit serial Programming (ICP) with industry-standard commercial programmers.
- IAP-Lite allows individual and multiple bytes of code memory to be used for data storage and programmed under control of the end application.
- Internal fixed boot ROM, containing low-level In-Application Programming (IAP) routines that can be called from the end application (in addition to IAP-Lite).
- Default serial loader providing In-System Programming (ISP) via the serial port, located in upper end of user program memory.
- Boot vector allows user-provided Flash loader code to reside anywhere in the Flash memory space, providing flexibility to the user.
- Programming and erase over the full operating voltage range.
- Read/Programming/Erase using ISP/IAP/IAP-Lite.
- Any flash program or erase operation in 2 ms.
- Programmable security for the code in the Flash for each sector.
- >100,000 typical erase/program cycles for each byte.
- 10 year minimum data retention.

8.24.3 ISP and IAP capabilities of the P89LPC920/921/922/9221

Flash organization: The P89LPC920/921/922/9221 program memory consists of two/four/eight 1 kB sectors. Each sector can be further divided into 64-byte pages. In addition to sector erase, page erase, and byte erase, a 64-byte page register is included which allows from 1 to 64 bytes of a given page to be programmed at the same time, substantially reducing overall programming time. An In-Application Programming (IAP) interface is provided to allow the end user's application to erase and reprogram the user code memory. In addition, erasing and reprogramming of user-programmable bytes including UCFG1, the Boot Status Bit and the Boot Vector are supported. As shipped from the factory, the upper 512 bytes of user code space contains a serial In-System Programming (ISP) routine allowing for the device to be programmed in circuit through the serial port.

Table 8: DC electrical characteristics...*continued*

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.

T_{amb} = –40 °C to +85 °C for industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{BO}	brownout trip voltage with BOV = '0', BOPD = '1'	2.4 V < V_{DD} < 3.6 V	2.40	-	2.70	V
V_{REF}	bandgap reference voltage		1.11	1.23	1.34	V
$TC_{(VREF)}$	bandgap temperature coefficient		-	10	20	ppm/°C

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] The $I_{DD(oper)}$, $I_{DD(idle)}$, and $I_{DD(PD)}$ specifications are measured using an external clock with the following functions disabled: comparators, brownout detect, and Watchdog timer.

[3] See Table 7 "Limiting values[1]" on page 35 for steady state (non-transient) limits on I_{OL} or I_{OH}. If I_{OL}/I_{OH} exceeds the test condition, V_{OL}/V_{OH} may exceed the related specification.

[4] Pin capacitance is characterized but not tested.

[5] Measured with port in quasi-bidirectional mode.

[6] Measured with port in high-impedance mode.

[7] Ports in quasi-bidirectional mode with weak pull-up (applies to all port pins with pull-ups). Does not apply to open-drain pins.

[8] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from '1' to '0'. This current is highest when V_{IN} is approximately 2 V.

Table 10: AC characteristics

V_{DD} = 3.0 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
f_{RCOSC}	internal RC oscillator frequency (nominal f = 7.3728 MHz)	trimmed to ±1% at T_{amb} = 25 °C	7.189	7.557	7.189	7.557	MHz
f_{WDOSC}	internal Watchdog oscillator frequency (nominal f = 400 kHz)		320	520	320	520	kHz
f_{osc}	oscillator frequency	[2]	0	18	-	-	MHz
t_{CLCL}	clock cycle	see Figure 13	55	-	-	-	ns
f_{CLKP}	CLKLP active frequency		0	8	-	-	MHz
Glitch filter							
	glitch rejection, P1.5/$\overline{RST}$ pin		-	50	-	50	ns
	signal acceptance, P1.5/$\overline{RST}$ pin		125	-	125	-	ns
	glitch rejection, any pin except P1.5/$\overline{RST}$		-	15	-	15	ns
	signal acceptance, any pin except P1.5/$\overline{RST}$		50	-	50	-	ns
External clock							
t_{CHCX}	HIGH time	see Figure 13	22	$t_{CLCL} - t_{CLCX}$	22	-	ns
t_{CLCX}	LOW time	see Figure 13	22	$t_{CLCL} - t_{CHCX}$	22	-	ns
t_{CLCH}	rise time	see Figure 13	-	5	-	5	ns
t_{CHCL}	fall time	see Figure 13	-	5	-	5	ns
Shift register (UART mode 0)							
t_{XLXL}	serial port clock cycle time		16 t_{CLCL}	-	888	-	ns
t_{QVXH}	output data set-up to clock rising edge		13 t_{CLCL}	-	722	-	ns
t_{XHQX}	output data hold after clock rising edge		-	t_{CLCL} + 20	-	75	ns
t_{XHDX}	input data hold after clock rising edge		-	0	-	0	ns
t_{DVXH}	input data valid to clock rising edge		150	-	150	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified. Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

[2] When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.

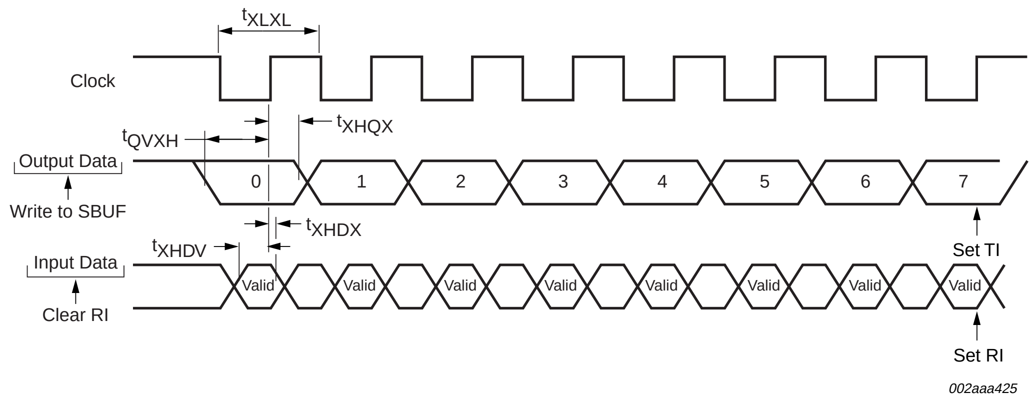


Fig 12. Shift register mode timing.

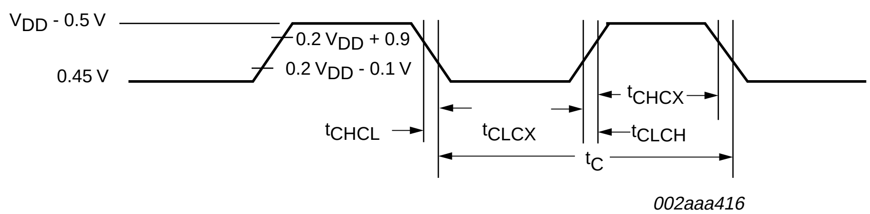


Fig 13. External clock timing.

Table 11: AC characteristics, ISP entry mode

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VR}	$\overline{RST}$ delay from V_{DD} active		50	-	-	µs
t_{RH}	$\overline{RST}$ HIGH time		1	-	32	µs
t_{RL}	$\overline{RST}$ LOW time		1	-	-	µs

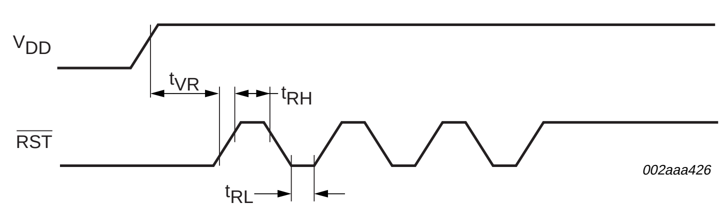
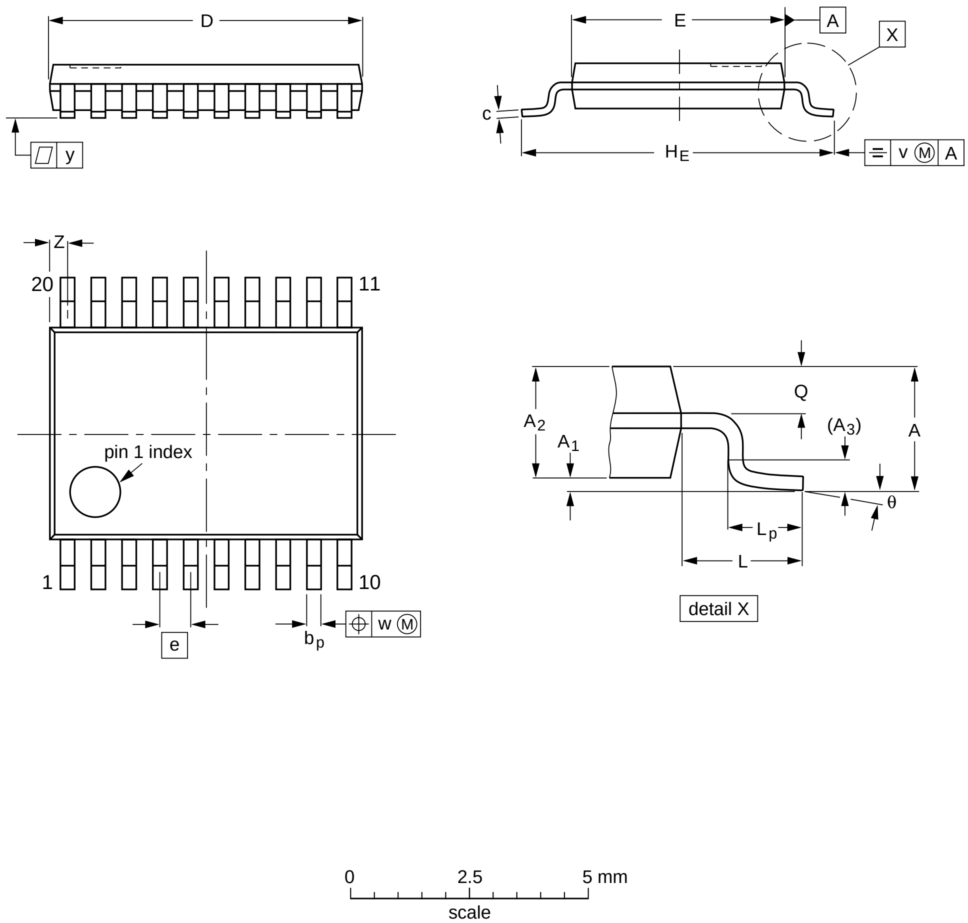


Fig 14. ISP entry waveform.

13. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 15. TSSOP20 (SOT360-1).

14. Revision history

Table 13: Revision history

Rev	Date	CPCN	Description
08	20041215	-	**Product data (9397 750 14469)** Modification: • Added 18 MHz information.
07	20041203	-	**Product data (9397 750 14251)**
06	20031121	-	**Product data (9397 750 12285); ECN 853-2403 01-A14557 of 18 November 2003**
05	20031007	-	**Product data (9397 750 12121); ECN 853-2403 30391 of 30 September 2003**
04	20030909	-	**Product data (9397 750 11945); ECN 853-2403 30305 of 5 September 2003**
03	20030811	-	**Preliminary data (9397 750 11786)**
02	20030522	-	**Objective data (9397 750 11532)**
01	20030505	-	**Preliminary data (9397 750 11387)**

Contents

1 General description . . . 1
2 Features . . . 1
2.1 Principal features . . . 1
2.2 Additional features . . . 2
3 Ordering information . . . 3
3.1 Ordering options . . . 3
4 Block diagram . . . 4
5 Pinning information . . . 5
5.1 Pinning . . . 5
5.2 Pin description . . . 6
6 Logic symbol . . . 8
7 Special function registers . . . 9
8 Functional description . . . 14
8.1 Enhanced CPU . . . 14
8.2 Clocks . . . 14
8.2.1 Clock definitions . . . 14
8.2.2 CPU clock (OSCCLK) . . . 14
8.2.3 Low speed oscillator option . . . 14
8.2.4 Medium speed oscillator option . . . 14
8.2.5 High speed oscillator option . . . 14
8.2.6 Clock output . . . 15
8.3 On-chip RC oscillator option . . . 15
8.4 Watchdog oscillator option . . . 15
8.5 External clock input option . . . 15
8.6 CPU Clock (CCLK) wake-up delay . . . 17
8.7 CPU Clock (CCLK) modification: DIVM register . . . 17
8.8 Low power select . . . 17
8.9 Memory organization . . . 17
8.10 Data RAM arrangement . . . 18
8.11 Interrupts . . . 18
8.11.1 External interrupt inputs . . . 18
8.12 I/O ports . . . 19
8.12.1 Port configurations . . . 19
8.12.2 Quasi-bidirectional output configuration . . . 20
8.12.3 Open-drain output configuration . . . 20
8.12.4 Input-only configuration . . . 20
8.12.5 Push-pull output configuration . . . 20
8.12.6 Port 0 analog functions . . . 20
8.12.7 Additional port features . . . 21
8.13 Power monitoring functions . . . 21
8.13.1 Brownout detection . . . 21
8.13.2 Power-on detection . . . 21
8.14 Power reduction modes . . . 21
8.14.1 Idle mode . . . 22
8.14.2 Power-down mode . . . 22
8.14.3 Total Power-down mode . . . 22
8.15 Reset . . . 22
8.15.1 Reset vector . . . 23
8.16 Timers/counters 0 and 1 . . . 23
8.16.1 Mode 0 . . . 23
8.16.2 Mode 1 . . . 23
8.16.3 Mode 2 . . . 24
8.16.4 Mode 3 . . . 24
8.16.5 Mode 6 . . . 24
8.16.6 Timer overflow toggle output . . . 24
8.17 Real-Time clock/system timer . . . 24
8.18 UART . . . 24
8.18.1 Mode 0 . . . 24
8.18.2 Mode 1 . . . 25
8.18.3 Mode 2 . . . 25
8.18.4 Mode 3 . . . 25
8.18.5 Baud rate generator and selection . . . 25
8.18.6 Framing error . . . 25
8.18.7 Break detect . . . 26
8.18.8 Double buffering . . . 26
8.18.9 Transmit interrupts with double buffering enabled (Modes 1, 2 and 3) . . . 26
8.18.10 The 9th bit (bit 8) in double buffering (Modes 1, 2 and 3) . . . 26
8.19 I^{2}C-bus serial interface . . . 27
8.20 Analog comparators . . . 29
8.20.1 Internal reference voltage . . . 29
8.20.2 Comparator interrupt . . . 30
8.20.3 Comparators and power reduction modes . . . 30
8.21 Keypad interrupt (KBI) . . . 30
8.22 Watchdog timer . . . 31
8.23 Additional features . . . 31
8.23.1 Software reset . . . 31
8.23.2 Dual data pointers . . . 31
8.24 Flash program memory . . . 32
8.24.1 General description . . . 32
8.24.2 Features . . . 32
8.24.3 ISP and IAP capabilities of the P89LPC920/921/922/9221 . . . 32
8.25 User configuration bytes . . . 34
8.26 User sector security bytes . . . 34
9 Limiting values . . . 35
10 Static characteristics . . . 36
11 Dynamic characteristics . . . 38
12 Comparator electrical characteristics . . . 41
13 Package outline . . . 42
14 Revision history . . . 44
15 Data sheet status . . . 45
16 Definitions . . . 45
17 Disclaimers . . . 45
18 Licenses . . . 45

Date of release: 15 December 2004 **Document order number: 9397 750 14469**

PHILIPS

Let's make things better.