Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc9221fdh-512

3. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
P89LPC920FDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
P89LPC921FDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
P89LPC922FDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
P89LPC922FN	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
P89LPC9221FN	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
P89LPC9221FDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

3.1 Ordering options

Table 2: Part options

Type number	Flash memory	Temperature range	Frequency
P89LPC920FDH	2 kB	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC921FDH	4 kB	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC922FDH	8 kB	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC922FN	8 kB	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC9221FN	8 kB	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC9221FDH	8 kB	–40 °C to +85 °C	0 MHz to 18 MHz

5.2 Pin description

Table 3: Pin description

Symbol	Pin	Type	Description
P0.0 to P0.7		I/O	**Port 0:** Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 “Port configurations” and Table 8 “DC electrical characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
	1	I/O	**P0.0 —** Port 0 bit 0.
		O	**CMP2 —** Comparator 2 output.
		I	**KBI0 —** Keyboard input 0.
	20	I/O	**P0.1 —** Port 0 bit 1.
		I	**CIN2B —** Comparator 2 positive input B.
		I	**KBI1 —** Keyboard input 1.
	19	I/O	**P0.2 —** Port 0 bit 2.
		I	**CIN2A —** Comparator 2 positive input A.
		I	**KBI2 —** Keyboard input 2.
	18	I/O	**P0.3 —** Port 0 bit 3. **High current source (P89LPC9221).**
		I	**CIN1B —** Comparator 1 positive input B.
		I	**KBI3 —** Keyboard input 3.
	17	I/O	**P0.4 —** Port 0 bit 4. **High current source (P89LPC9221).**
		I	**CIN1A —** Comparator 1 positive input A.
		I	**KBI4 —** Keyboard input 4.
	16	I/O	**P0.5 —** Port 0 bit 5. **High current source (P89LPC9221).**
		I	**CMPREF —** Comparator reference (negative) input.
		I	**KBI5 —** Keyboard input 5.
	14	I/O	**P0.6 —** Port 0 bit 6. **High current source (P89LPC9221).**
		O	**CMP1 —** Comparator 1 output.
		I	**KBI6 —** Keyboard input 6.
	13	I/O	**P0.7 —** Port 0 bit 7. **High current source (P89LPC9221).**
		I/O	**T1 —** Timer/counter 1 external count input or overflow output.
		I	**KBI7 —** Keyboard input 7.

Table 3: Pin description...*continued*

Symbol	Pin	Type	Description
P1.0 to P1.7		I/O, I [1]	**Port 1:** Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.12.1 "Port configurations" and Table 8 "DC electrical characteristics" for details. P1.2 - P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
	12	I/O	**P1.0 —** Port 1 bit 0.
		O	**TXD —** Transmitter output for the serial port.
	11	I/O	**P1.1 —** Port 1 bit 1.
		I	**RXD —** Receiver input for the serial port.
	10	I/O	**P1.2 —** Port 1 bit 2 (open-drain when used as output).
		I/O	**T0 —** Timer/counter 0 external count input or overflow output (open-drain when used as output).
		I/O	**SCL —** I^2C serial clock input/output.
	9	I/O	**P1.3 —** Port 1 bit 3 (open-drain when used as output).
		I	**$\overline{\text{INT0}}$ —** External interrupt 0 input.
		I/O	**SDA —** I^2C serial data input/output.
	8	I/O	**P1.4 —** Port 1 bit 4. **High current source (P89LPC9221).**
		I	**$\overline{\text{INT1}}$ —** External interrupt 1 input.
	4	I	**P1.5 —** Port 1 bit 5 (input only).
		I	**$\overline{\text{RST}}$ —** External Reset input (if selected via FLASH configuration). A LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**
	3	I/O	**P1.6 —** Port 1 bit 6. **High current source (P89LPC9221).**
	2	I/O	**P1.7 —** Port 1 bit 7. **High current source (P89LPC9221).**

Table 3: Pin description...*continued*

Symbol	Pin	Type	Description
P3.0 to P3.1		I/O	**Port 3:** Port 3 is an 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 8 "DC electrical characteristics" for details. All pins have Schmitt triggered inputs. Port 3 also provides various special functions as described below:
	7	I/O	**P3.0 —** Port 3 bit 0.
		O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the FLASH configuration.
		O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the real time clock/system timer.
	6	I/O	**P3.1 —** Port 3 bit 1.
		I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the FLASH configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the real time clock/system timer.
V_{SS}	5	I	**Ground:** 0 V reference.
V_{DD}	15	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power down modes.

[1] Input/Output for P1.0-P1.4, P1.6, P1.7. Input for P1.5.

6. Logic symbol

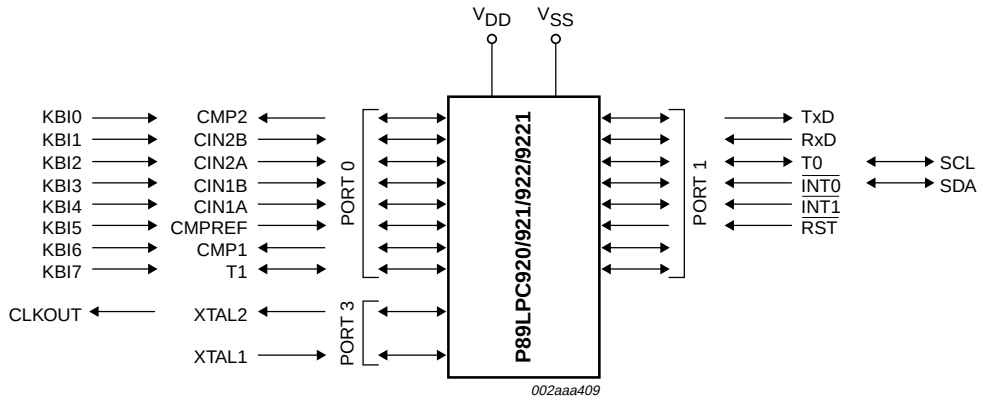


Fig 4. Logic symbol.

Table 4: Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00[1]	00x0xx00
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03[1]	xxxxxx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00[1]	xxxxxx00
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	00000000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	-	I2PD	-	SPD	-	00[1]	00000000
	Bit address		**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00H	00000000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00H	xx00000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX		[3]
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[1][6]	
RTCH	Real-time clock register HIGH	D2H									00[6]	00000000
RTCL	Real-time clock register LOW	D3H									00[6]	00000000
SADDR	Serial port address register	A9H									00	00000000
SADEN	Serial port address enable	B9H									00	00000000
SBUF	Serial Port data buffer register	99H									xx	xxxxxxxx
	Bit address		**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	00000000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	00000000
SP	Stack pointer	81H									07	00000111
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0xxx0
	Bit address		**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	00000000
TH0	Timer 0 HIGH	8CH									00	00000000
TH1	Timer 1 HIGH	8DH									00	00000000
TL0	Timer 0 LOW	8AH									00	00000000
TL1	Timer 1 LOW	8BH									00	00000000
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	00000000

9397 750 14469

8.6 CPU Clock (CCLK) wake-up delay

The P89LPC920/921/922/9221 has an internal wake-up timer that delays the clock until it stabilizes depending to the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 992 OSCCLK cycles plus 60 to 100 μs. If the clock source is either the internal RC oscillator, watchdog oscillator, or external clock, the delay is 224 OSCCLK cycles plus 60 to 100 μs.

8.7 CPU Clock (CCLK) modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

8.8 Low power select

The P89LPC920/921/922/9221 is designed to run at 18 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to ‘1’ to lower the power consumption further. On any reset, CLKLP is ‘0’ allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

8.9 Memory organization

The various P89LPC920/921/922/9221 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00h:7Fh) accessed via direct or indirect addressing, using instruction other than MOVX and MOVC. All or part of the Stack may be in this area.

- IDATA

  Indirect Data. 256 bytes of internal data memory space (00h:FFh) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC920/921/922/9221 has 2 kB/4 kB/8 kB of on-chip Code memory.

8.10 Data RAM arrangement

The 256 bytes of on-chip RAM are organized as shown in Table 5.

Table 5: On-chip data memory usages

Type	Data RAM	Size (bytes)
DATA	Memory that can be addressed directly and indirectly	128
IDATA	Memory that can be addressed indirectly	256

8.11 Interrupts

The P89LPC920/921/922/9221 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources. The P89LPC920/921/922/9221 supports 12 interrupt sources: external interrupts 0 and 1, timers 0 and 1, serial port Tx, serial port Rx, combined serial port Rx/Tx, brownout detect, watchdog/real-time clock, I^2C, keyboard, and comparators 1 and 2.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1, and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

8.11.1 External interrupt inputs

The P89LPC920/921/922/9221 has two external interrupt inputs as well as the Keypad Interrupt function. The two interrupt inputs are identical to those present on the standard 80C51 microcontrollers.

These external interrupts can be programmed to be level-triggered or edge-triggered by setting or clearing bit IT1 or IT0 in Register TCON.

In edge-triggered mode if successive samples of the $\overline{\text{INTn}}$ pin show a HIGH in one cycle and a LOW in the next cycle, the interrupt request flag IEn in TCON is set, causing an interrupt request.

If an external interrupt is enabled when the P89LPC920/921/922/9221 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 8.14 “Power reduction modes” for details.

P1.2 (SCL/T0) and P1.3 (SDA/$\overline{INT0}$) may only be configured to be either input-only or open-drain.

8.12.2 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC920/921/922/9221 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.12.3 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic ‘0’. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

An open-drain port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.12.4 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt-triggered input that also has a glitch suppression circuit.

8.12.5 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic ‘1’. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt-triggered input that also has a glitch suppression circuit. The P89LPC9221 device has high source current on eight pins in push-pull mode. See Table 8 “DC electrical characteristics”.

8.12.6 Port 0 analog functions

The P89LPC920/921/922/9221 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high impedance) mode as described in Section 8.12.4.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register, bits 1:5. On any reset, PT0AD1:5 defaults to ‘0’s to enable digital functions.

- External reset pin (during power-up or if user configured via UCFG1). This option must be used for an oscillator frequency above 12 MHz);
- Power-on detect;
- Brownout detect;
- Watchdog Timer;
- Software reset;
- UART break character detect reset.

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a '0' to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

8.15.1 Reset vector

Following reset, the P89LPC920/921/922/9221 will fetch instructions from either address 0000h or the Boot address. The Boot address is formed by using the Boot Vector as the high byte of the address and the low byte of the address = 00h.

The Boot address will be used if a UART break reset occurs, or the non-volatile Boot Status bit (BOOTSTAT.0) = 1, or the device is forced into ISP mode during power-on (see *P89LPC920/921/922/9221 User's Manual*). Otherwise, instructions will be fetched from address 0000H.

8.16 Timers/counters 0 and 1

The P89LPC920/921/922/9221 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. Both can be configured to operate either as timers or event counter. An option to automatically toggle the T0 and/or T1 pins upon timer overflow has been added.

In the 'Timer' function, the register is incremented every machine cycle.

In the 'Counter' function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once during every machine cycle.

Timer 0 and Timer 1 have five operating modes (modes 0, 1, 2, 3 and 6). Modes 0, 1, 2 and 6 are the same for both Timers/Counters. Mode 3 is different.

8.16.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

8.16.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

8.16.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

8.16.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

8.16.5 Mode 6

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

8.16.6 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

8.17 Real-Time clock/system timer

The P89LPC920/921/922/9221 has a simple Real-Time clock that allows a user to continue running an accurate timer while the rest of the device is powered-down. The Real-Time clock can be a wake-up or an interrupt source. The Real-Time clock is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all ‘0’s, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator, provided that the XTAL oscillator is not being used as the CPU clock. If the XTAL oscillator is used as the CPU clock, then the RTC will use CCLK as its clock source. Only power-on reset will reset the Real-Time clock and its associated SFRs to the default state.

8.18 UART

The P89LPC920/921/922/9221 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC920/921/922/9221 does include an independent Baud Rate Generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options.The UART can be operated in 4 modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16.

8.18.1 Mode 0

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $^{1}/_{16}$ of the CPU clock frequency.

8.18.2 Mode 1

10 bits are transmitted (through TxD) or received (through RxD): a start bit (logical ‘0’), 8 data bits (LSB first), and a stop bit (logical ‘1’). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 8.18.5 “Baud rate generator and selection”).

8.18.3 Mode 2

11 bits are transmitted (through TxD) or received (through RxD): start bit (logical ‘0’), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical ‘1’). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of ‘0’ or ‘1’. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is not saved. The baud rate is programmable to either $^{1}/_{16}$ or $^{1}/_{32}$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

8.18.4 Mode 3

11 bits are transmitted (through TxD) or received (through RxD): a start bit (logical ‘0’), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical ‘1’). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 8.18.5 “Baud rate generator and selection”).

8.18.5 Baud rate generator and selection

The P89LPC920/921/922/9221 enhanced UART has an independent Baud Rate Generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1 and BRGR0 SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1 but is much more accurate. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UART can use either Timer 1 or the baud rate generator output (see Figure 7). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is set. The independent Baud Rate Generator uses OSCCLK.

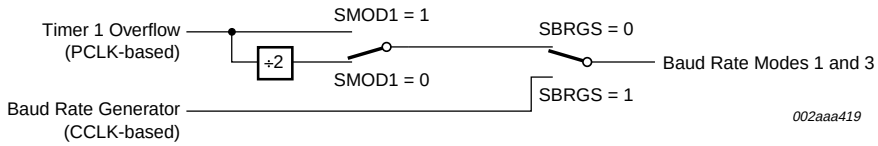


Fig 7. Baud rate sources for UART (Modes 1, 3).

8.18.6 Framing error

Framing error is reported in the status register (SSTAT). In addition, if SMOD0 (PCON.6) is ‘1’, framing errors can be made available in SCON.7 respectively. If SMOD0 is ‘0’, SCON.7 is SM0. It is recommended that SM0 and SM1 (SCON.7:6) are set up when SMOD0 is ‘0’.

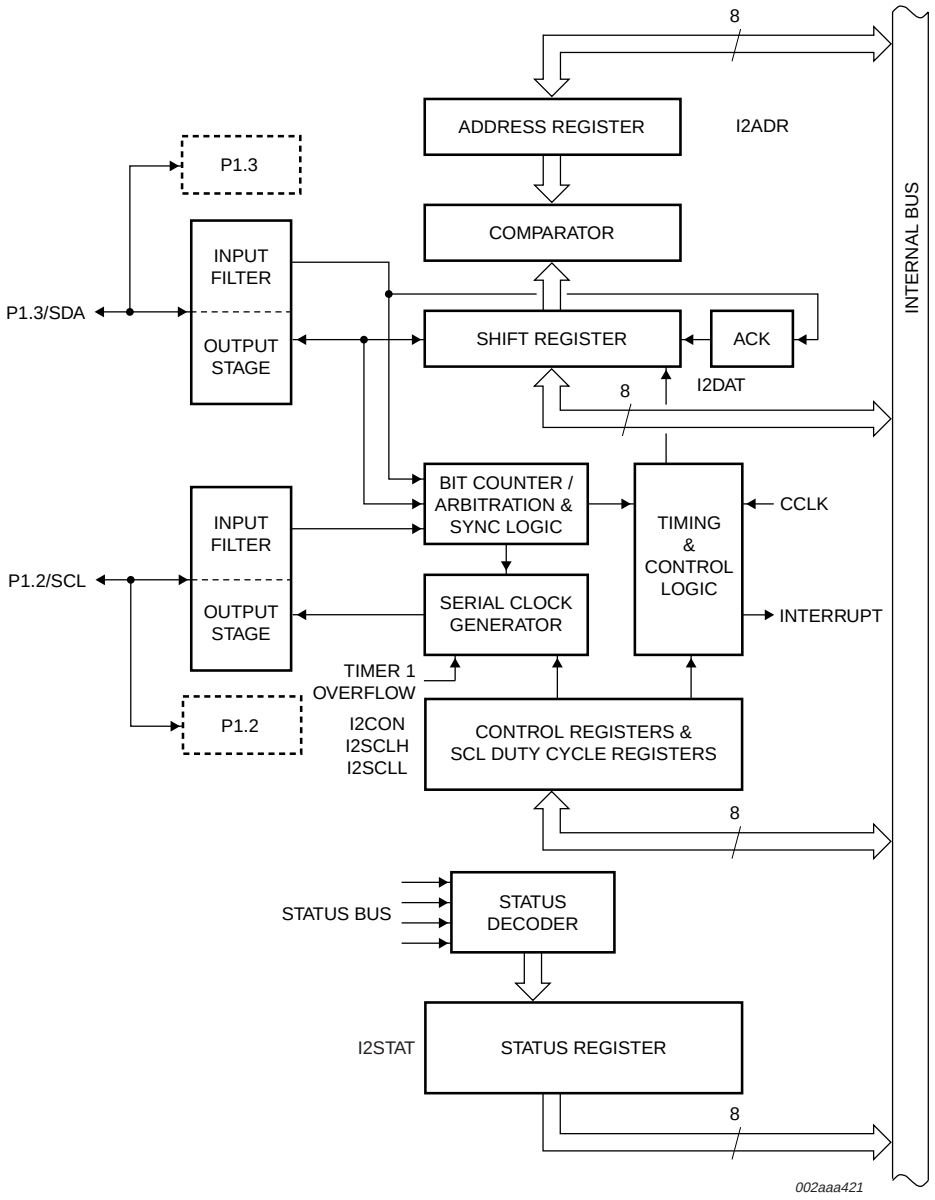
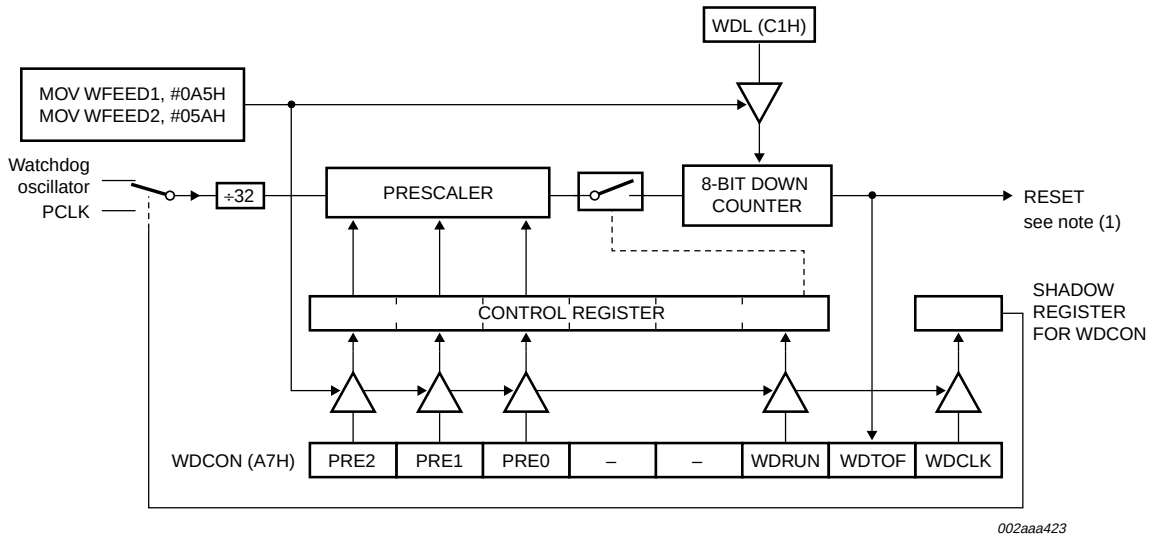


Fig 9. I^2C-bus serial interface block diagram.

8.22 Watchdog timer

The Watchdog timer causes a system reset when it underflows as a result of a failure to feed the timer prior to the timer reaching its terminal count. It consists of a programmable 12-bit prescaler, and an 8-bit down counter. The down counter is decremented by a tap taken from the prescaler. The clock source for the prescaler is either the PCLK or the nominal 400 kHz Watchdog oscillator. The Watchdog timer can only be reset by a power-on reset. When the watchdog feature is disabled, it can be used as an interval timer and may generate an interrupt. Figure 11 shows the Watchdog timer in watchdog mode. Feeding the watchdog requires a two-byte sequence. If PCLK is selected as the watchdog clock and the CPU is powered-down, the watchdog is disabled. The Watchdog timer has a time-out period that ranges from a few µs to a few seconds. Please refer to the *P89LPC920/921/922/9221* User's Manual for more details.



(1) Watchdog reset can also be caused by an invalid feed sequence, or by writing to WDCON not immediately followed by a feed sequence.

Fig 11. Watchdog timer in watchdog mode (WDTE = '1').

8.23 Additional features

8.23.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

8.23.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic '0' so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

8.24 Flash program memory

8.24.1 General description

The P89LPC920/921/922/9221 Flash memory provides in-circuit electrical erasure and programming. The Flash can be read, erased, or written as bytes. The Sector and Page Erase functions can erase any Flash sector (1 kB) or page (64 bytes). The Chip Erase operation will erase the entire program memory. In-System Programming and standard parallel programming are both available. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC920/921/922/9221 Flash reliably stores memory contents even after 10,000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC920/921/922/9221 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms.

8.24.2 Features

- Parallel programming with industry-standard commercial programmers.
- In-Circuit serial Programming (ICP) with industry-standard commercial programmers.
- IAP-Lite allows individual and multiple bytes of code memory to be used for data storage and programmed under control of the end application.
- Internal fixed boot ROM, containing low-level In-Application Programming (IAP) routines that can be called from the end application (in addition to IAP-Lite).
- Default serial loader providing In-System Programming (ISP) via the serial port, located in upper end of user program memory.
- Boot vector allows user-provided Flash loader code to reside anywhere in the Flash memory space, providing flexibility to the user.
- Programming and erase over the full operating voltage range.
- Read/Programming/Erase using ISP/IAP/IAP-Lite.
- Any flash program or erase operation in 2 ms.
- Programmable security for the code in the Flash for each sector.
- >100,000 typical erase/program cycles for each byte.
- 10 year minimum data retention.

8.24.3 ISP and IAP capabilities of the P89LPC920/921/922/9221

Flash organization: The P89LPC920/921/922/9221 program memory consists of two/four/eight 1 kB sectors. Each sector can be further divided into 64-byte pages. In addition to sector erase, page erase, and byte erase, a 64-byte page register is included which allows from 1 to 64 bytes of a given page to be programmed at the same time, substantially reducing overall programming time. An In-Application Programming (IAP) interface is provided to allow the end user's application to erase and reprogram the user code memory. In addition, erasing and reprogramming of user-programmable bytes including UCFG1, the Boot Status Bit and the Boot Vector are supported. As shipped from the factory, the upper 512 bytes of user code space contains a serial In-System Programming (ISP) routine allowing for the device to be programmed in circuit through the serial port.

Flash programming and erasing: There are three methods of erasing or programming of the Flash memory that may be used. First, the Flash may be programmed or erased in the end-user application by calling low-level routines through a common entry point. Second, the on-chip ISP boot loader may be invoked. This ISP boot loader will, in turn, call low-level routines through the same common entry point that can be used by the end-user application. Third, the Flash may be programmed or erased using the parallel method by using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead this device provides a 32-bit CRC result on either a sector or the entire 2 kB/4 kB/8 kB of user code space.

Boot ROM: When the microcontroller programs its own Flash memory, all of the low-level details are handled by code that is contained in a Boot ROM that is separate from the Flash memory. A user program simply calls the common entry point in the Boot ROM with appropriate parameters to accomplish the desired operation. The Boot ROM include operations such as erase sector, erase page, program page, CRC, program security bit, etc. The Boot ROM occupies the program memory space at the top of the address space from FF00H to FEFFH, thereby not conflicting with the user program memory space.

Power-on reset code execution: The P89LPC920/921/922/9221 contains two special Flash elements: the Boot Vector and the Boot Status Bit. Following reset, the P89LPC920/921/922/9221 examines the contents of the Boot Status Bit. If the Boot Status Bit is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Boot Status Bit is set to a one, the contents of the Boot Vector is used as the high byte of the execution address and the low byte is set to 00H. The factory default setting is 1FH for the P89LPC9221 and P89LPC922, and corresponds to the address 1F00H for the default ISP boot loader. The factory default setting is 0FH for the P89LPC921 and corresponds to the address 0F00H for the default ISP boot loader. The factory default setting for the LPC920 is 07H and corresponds to the address 0700H. This boot loader is pre-programmed at the factory into this address space and can be erased by the user. **Users who wish to use this loader should take precautions to avoid erasing the 1 kB sector from 1C00H to 1FFFH in the P89LPC922/9221 or the 1 kB sector from 0C00H to 0FFFH in the P89LPC921, or the 1 kB sector from 0400H to 07FFH in the P89LPC920. Instead, the page erase function can be used to erase the eight 64-byte pages which comprise the lower 512 bytes of the sector.** A custom boot loader can be written with the Boot Vector set to the custom boot loader, if desired.

Hardware activation of the boot loader: The boot loader can also be executed by forcing the device into ISP mode during a power-on sequence (see the *P89LPC920/921/922/9221 User's Manual* for specific information). This has the same effect as having a non-zero Boot Status Bit. This allows an application to be built that will normally execute user code but can be manually forced into ISP operation. If the factory default setting for the Boot Vector is changed, it will no longer point to the factory pre-programmed ISP boot loader code. If this happens, the only way it is possible to change the contents of the Boot Vector is through the parallel programming method, provided that the end user application does not contain a customized loader that provides for erasing and reprogramming of the Boot Vector

and Boot Status Bit. After programming the Flash, the Boot Status Bit should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

In-System Programming (ISP): In-System Programming is performed without removing the microcontroller from the system. The In-System Programming facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the P89LPC920/921/922/9221 through the serial port. This firmware is provided by Philips and embedded within each P89LPC920/921/922/9221 device. The Philips In-System Programming facility has made in-system programming in an embedded application possible with a minimum of additional expense in components and circuit board area. The ISP function uses five pins (V_{DD}, V_{SS}, TXD, RXD, and $\overline{RST}$). Only a small connector needs to be available to interface your application to an external circuit in order to use this feature. Please see the *P89LPC920/921/922/9221 User's Manual* for additional details.

In-Application Programming (IAP): Several In-Application Programming (IAP) calls are available for use by an application program to permit selective erasing and programming of Flash sectors, pages, security bits, configuration bytes, and device identification. All calls are made through a common interface, PGM_MTP. The programming functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FF00H. Please see the *P89LPC920/921/922/9221 User's Manual* for additional details.

In-Circuit Programming (ICP): In-Circuit Programming is a method intended to allow commercial programmers to program and erase these devices without removing the microcontroller from the system. The In-Circuit Programming facility consists of a series of internal hardware resources to facilitate remote programming of the P89LPC920/921/922/9221 through a two-wire serial interface. Philips has made in-circuit programming in an embedded application possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins (V_{DD}, V_{SS}, P0.5, P0.4, and $\overline{RST}$). Only a small connector needs to be available to interface your application to an external programmer in order to use this feature.

8.25 User configuration bytes

A number of user-configurable features of the P89LPC920/921/922/9221 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the Flash byte UCFG1. Please see the *P89LPC920/921/922/9221 User's Manual* for additional details.

8.26 User sector security bytes

There are two/four/eight User Sector Security Bytes, each corresponding to one sector. Please see the *P89LPC920/921/922/9221 User's Manual* for additional details.

10. Static characteristics

Table 8: DC electrical characteristics

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(oper)}$	power supply current, operating	3.6 V; 12 MHz	[2]	-	9	15	mA
		3.6 V; 18 MHz	[2]	-	11.5	20	mA
$I_{DD(idle)}$	power supply current, Idle mode	3.6 V; 12 MHz	[2]	-	3.25	5	mA
		3.6 V; 18 MHz	[2]	-	5	7	mA
$I_{DD(PD)}$	power supply current, Power-down mode, voltage comparators powered-down	3.6 V	[2]	-	55	80	µA
$I_{DD(TPD)}$	power supply current, Total Power-down mode	3.6 V	[2]	-	1	5	µA
$(dV_{DD}/dt)_r$	V_{DD} rise rate			-	-	2	mV/µs
$(dV_{DD}/dt)_f$	V_{DD} fall rate			-	-	50	mV/µs
V_{POR}	Power-on reset detect voltage			-	-	0.2	V
V_{RAM}	RAM keep-alive voltage			1.5	-	-	V
$V_{th(HL)}$	negative-going threshold voltage	except SCL, SDA		$0.22V_{DD}$	$0.4V_{DD}$	-	V
V_{IL}	LOW-level input voltage	SCL, SDA only		–0.5	-	$0.3V_{DD}$	V
$V_{th(LH)}$	positive-going threshold voltage	except SCL, SDA		-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{IH}	HIGH-level input voltage	SCL, SDA only		$0.7V_{DD}$	-	5.5	V
V_{hys}	hysteresis voltage	Port 1		-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage; all ports, all modes except Hi-Z[3]	I_{OL} = 20 mA		-	0.6	1.0	V
		I_{OL} = 3.2 mA		-	0.2	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –20 mA; push-pull mode P0.3 to P0.7, P1.4, P1.6, P1.7		$0.8V_{DD}$	-	-	V
		I_{OH} = –3.2 mA; push-pull mode, all other ports		V_{DD} – 0.7	V_{DD} – 0.4	-	V
		I_{OH} = –20 µA; quasi-bidirectional mode, all ports		V_{DD} – 0.3	V_{DD} – 0.2	-	V
C_{ig}	input/output pin capacitance		[4]	-	-	15	pF
I_{IL}	logical 0 input current, all ports	V_{IN} = 0.4 V	[5]	-	-	–80	µA
I_{LI}	input leakage current, all ports	V_{IN} = V_{IL} or V_{IH}	[6]	-	-	±10	µA
I_{TL}	logical 1-to-0 transition current, all ports	V_{IN} = 2.0 V at V_{DD} = 3.6 V	[7], [8]	–30	-	–450	µA
R_{RST}	internal reset pull-up resistor			10	-	30	kΩ

11. Dynamic characteristics

Table 9: AC characteristics

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
f_{RCOSC}	internal RC oscillator frequency (nominal f = 7.3728 MHz)	trimmed to ±1% at T_{amb} = 25 °C	7.189	7.557	7.189	7.557	MHz
f_{WDOSC}	internal Watchdog oscillator frequency (nominal f = 400 kHz)		320	520	320	520	kHz
f_{osc}	oscillator frequency		0	12	-	-	MHz
t_{CLCL}	clock cycle	see Figure 13	83	-	-	-	ns
f_{CLKP}	CLKLP active frequency		0	8	-	-	MHz
Glitch filter							
	glitch rejection, P1.5/$\overline{RST}$ pin		-	50	-	50	ns
	signal acceptance, P1.5/$\overline{RST}$ pin		125	-	125	-	ns
	glitch rejection, any pin except P1.5/$\overline{RST}$		-	15	-	15	ns
	signal acceptance, any pin except P1.5/$\overline{RST}$		50	-	50	-	ns
External clock							
t_{CHCX}	HIGH time	see Figure 13	33	$t_{CLCL} - t_{CLCX}$	33	-	ns
t_{CLCX}	LOW time	see Figure 13	33	$t_{CLCL} - t_{CHCX}$	33	-	ns
t_{CLCH}	rise time	see Figure 13	-	8	-	8	ns
t_{CHCL}	fall time	see Figure 13	-	8	-	8	ns
Shift register (UART mode 0)							
t_{XLXL}	serial port clock cycle time		16 t_{CLCL}	-	1333	-	ns
t_{QVXH}	output data set-up to clock rising edge		13 t_{CLCL}	-	1083	-	ns
t_{XHQX}	output data hold after clock rising edge		-	t_{CLCL} + 20	-	103	ns
t_{XHDX}	input data hold after clock rising edge		-	0	-	0	ns
t_{DVXH}	input data valid to clock rising edge		150	-	150	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified. Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

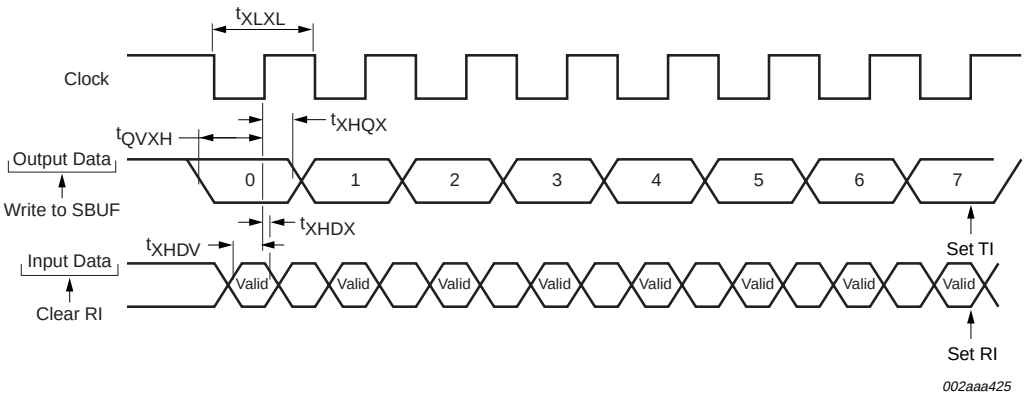


Fig 12. Shift register mode timing.

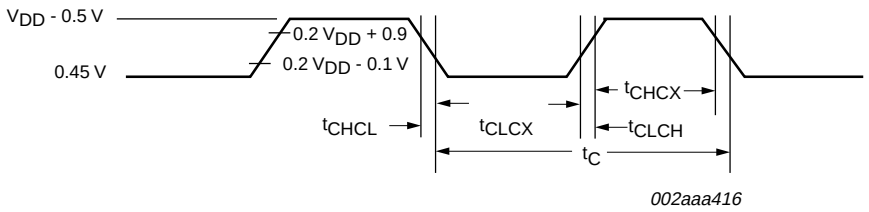


Fig 13. External clock timing.

Table 11: AC characteristics, ISP entry mode

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VR}	$\overline{RST}$ delay from V_{DD} active		50	-	-	µs
t_{RH}	$\overline{RST}$ HIGH time		1	-	32	µs
t_{RL}	$\overline{RST}$ LOW time		1	-	-	µs

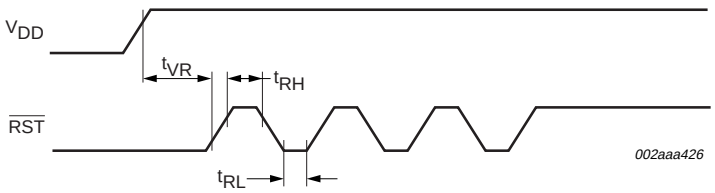


Fig 14. ISP entry waveform.

Contents

Date of release: 15 December 2004 **Document order number: 9397 750 14469**