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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Discontinued at Digi-Key
Module/Board Type	MPU Core
Core Processor	Zynq UltraScale+ XCZU2EG-1SFVC784E
Co-Processor	-
Speed	-
Flash Size	128MB
RAM Size	2GB
Connector Type	B2B
Size / Dimension	2.99" x 2.05" (76mm x 52mm)
Operating Temperature	0°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0803-01-02eg-1ea

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2.2 Block Diagram

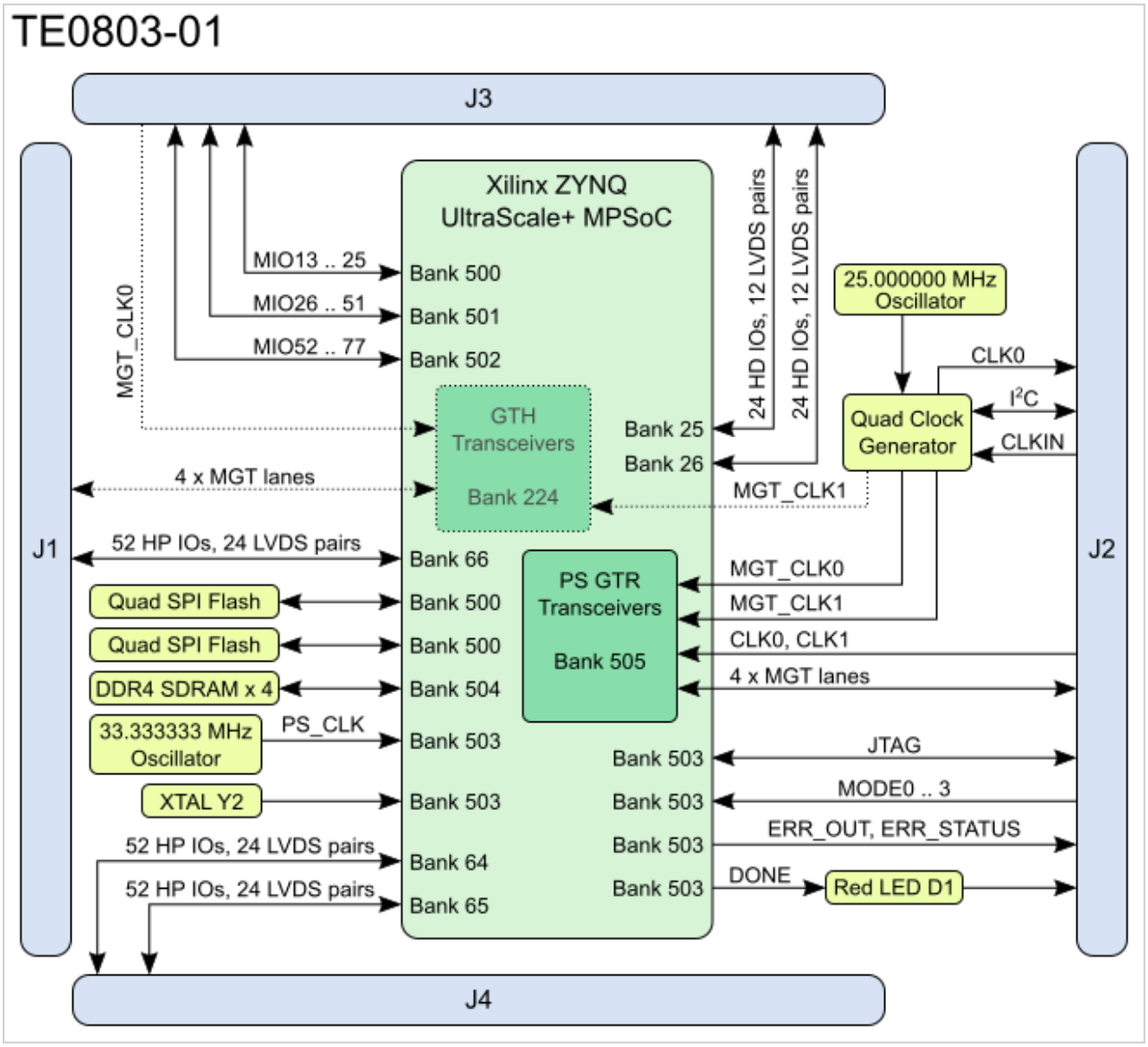


Figure 1: TE0803-01 Block Diagram

2.3 Main Components

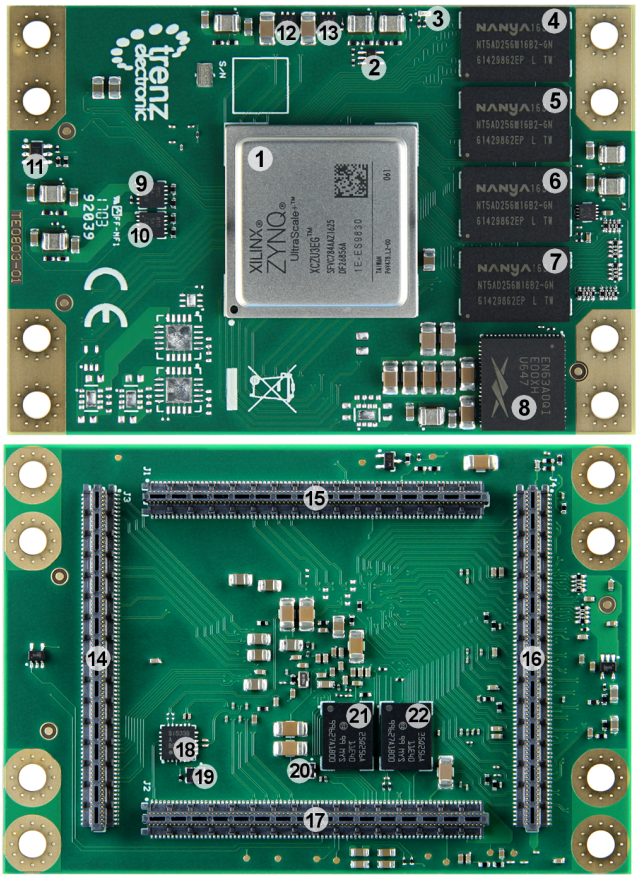


Figure 2: TE0803-01 MPSoC module

1. Xilinx ZYNQ UltraScale+ MPSoC, U1
2. 2-Input AND Gate, U39
3. Red LED (DONE), D1
4. 256Mx16 DDR4-2400 SDRAM, U12
5. 256Mx16 DDR4-2400 SDRAM, U9
6. 256Mx16 DDR4-2400 SDRAM, U2
7. 256Mx16 DDR4-2400 SDRAM, U3
8. 12A PowerSoC DC-DC converter, U4
9. 1.5A LDO DC-DC converter, U10
10. 1.5A LDO DC-DC converter, U8
11. Voltage monitor circuit, U41
12. 0.35A LDO DC-DC converter, U26
13. 0.35A LDO DC-DC converter, U27
14. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J3
15. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J1
16. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J4
17. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J2
18. 4-channel programmable PLL clock generator, U5
19. Low-power programmable oscillator @ 25.000000 MHz, U5
20. Low-power programmable oscillator @ 33.333333 MHz (PS_CLK), U32
21. 256 Mbit serial NOR Flash memory, U7
22. 256 Mbit serial NOR Flash memory, U17

2.4 Initial Delivery State

Storage device name	Content	Notes
SPI Flash main array	Not programmed	-
eFUSE Security	Not programmed	-
Si5338A programmable PLL NVM OTP	Not programmed	-

Table 1: Initial Delivery State of the flash memories

3 Signals, Interfaces and Pins

3.1 Board to Board (B2B) connectors

The TE0803 MPSoC SoM has four Board to Board (B2B) connectors with 160 contacts per connector.

Each connector has a specific arrangement of the signal-pins, which are grouped together in categories related to their functionalities and to their belonging to particular units of the Zynq UltraScale+ MPSoC like I/O-banks, interfaces and Gigabit transceivers
or to the on-board peripherals.

Following table lists the I/O-bank signals, which are routed from the MPSoC's PL and PS banks as LVDS pairs or single ended I/O's to the B2B connectors.

Bank	Type	B2B Connector	Schematic Names / Connector Pins	I/O Signal Count	LVDS Pairs Count	VCCO Bank Voltage	Notes
25[1)]	HD	J3	B25_L1_P ... B25_L12_P B25_L1_N ... B25_L12_N	24 I/O's	12	VCCO25 pins J3-15, J3-16	VCCO max. 3.3V usable as single-ended I/O's
26[2)]	HD	J3	B26_L1_P ... B26_L12_P B26_L1_N ... B26_L12_N	24 I/O's	12	VCCO26 pins J3-43, J3-44	VCCO max. 3.3V usable as single-ended I/O's
64	HP	J4	B64_L1_P ... B64_L24_P B64_L1_N ... B64_L24_N B64_T0 ... B64_T3	52 I/O's	24	VCCO64 pins J4-58, J4-106	VCCO max. 1.8V usable as single-ended I/O's
65	HP	J4	B65_L1_P ... B65_L24_P B65_L1_N ... B65_L24_N B65_T0 ... B65_T3	52 I/O's	24	VCCO65 pins J4-69, J4-105	VCCO max. 1.8V usable as single-ended I/O's
66	HP	J1	B66_L1_P ... B66_L24_P B66_L1_N ... B66_L24_N B66_T0 ... B66_T3	52 I/O's	24	VCCO66 pins J1-90, J1-120	VCCO max. 1.8V usable as single-ended I/O's
500	MIO	J3	MIO13 ... MIO25	13 I/O's	-	PS_1V8	user configurable I/O's on B2B

Bank	Type	B2B Connector	Schematic Names / Connector Pins	I/O Signal Count	LVDS Pairs Count	VCCO Bank Voltage	Notes
501	MIO	J3	MIO26 ... MIO51	26 I/O's	-	PS_1V8	user configurable I/O's on B2B
502	MIO	J3	MIO52 ... MIO77	26 I/O's	-	PS_1V8	user configurable I/O's on B2B

Table 2: B2B connector pin-outs of available PL and PS banks of the TE0803-01 SoM

1) Bank 25 at XC**ZU2** / XC**ZU3**, else Bank 45 at XC**ZU4** / XC**ZU5**

2) Bank 26 at XC**ZU2** / XC**ZU3**, else Bank 46 at XC**ZU4** / XC**ZU5**

All MIO banks are powered from on-module DC-DC power rail. All PL I/O banks have separate VCCO input pins in the B2B connectors, valid VCCO should be supplied from the carrier board.

For detailed information about the B2B pin-out, please refer to the Pin-out table.

The configuration of the I/O's MIO13 - MIO77 are depending on the base-board peripherals connected to these pins.

3.2 MGT Lanes

The B2B connectors J1 and J2 provide also access to the MGT banks of the Zynq UltraScale+ MPSoC. There are 8 high-speed data lanes (Xilinx GTH / GTR transceiver) available composed as differential signaling pairs for both directions (RX/TX).

The MGT banks have also clock input-pins which are exposed to the B2B connectors J2 and J3. Following MGT lanes are available on the B2B connectors:

MIO	U7 Pin	Pin Name	MIO	U17 Pin	Pin Name
0	B2	CLK	7	C2	CS#
1	D2	DO/IO1	8	D3	DI/IO0
2	C4	WP#/IO2	9	D2	DO/IO1
3	D4	HOLD#/IO3	10	C4	WP#/IO2
4	D3	DI/IO0	11	D4	HOLD#/IO3
5	C2	CS#	12	B2	CLK

Table 7: MIO pin assignment of the Quad SPI Flash memory ICs

4 Boot Process

The boot source of the Zynq UltraScale+ MPSoC can be selected via 4 dedicated pins, which generate a 4-bit code to select the boot mode. The pins are accessible on B2B connector J2:

Boot Mode Pin	B2B Pin
PS_MODE0	J2-109
PS_MODE1	J2-107
PS_MODE2	J2-105
PS_MODE3	J2-103

Table 8: Boot mode pins on B2B connector J2

Following boot modes are possible on the TE0803 UltraScale+ MPSoC module by generating the corresponding 4-bit code with pins 'PS_MODE0' ... 'PS_MODE3' (little-endian alignment):

Boot Mode	Mode Pins [3:0]	MIO Location	Description
JTAG	0x0	JTAG	Dedicated PS interface.
QSPI32	0x2	MIO[12:0]	Configured on module with dual QSPI Flash Memory. 32-bit addressing. Supports single and dual parallel configurations. Stack and dual stack is not supported.
SD0	0x3	MIO[25:13]	Supports SD 2.0.
SD1	0x5	MIO[51:38]	Supports SD 2.0.
eMMC_18	0x6	MIO[22:13]	Supports eMMC 4.5 at 1.8V.
USB 0	0x7	MIO[52:63]	Supports USB 2.0 and USB 3.0.
PJTAG_0	0x8	MIO[29:26]	PS JTAG connection 0 option.
SD1-LS	0xE	MIO[51:39]	Supports SD 3.0 with a required SD 3.0 compliant level shifter.

Table 9: Selectable boot modes by dedicated boot mode pins

For functional details see ug1085 - Zynq UltraScale+ TRM (Boot Modes Section).

Signal	B2B Connector pin	Function
PLL_SCL / PLL_SDA	J2-90 / J2-92	I^2C interface, external pull-ups needed for SCL/SDA line. I^2C address in current configuration: 1110000b

Table 12: B2B connector pin-out of Si5338A control interface

> ⚠ Si5338A OTP ROM is not programmed by default at delivery, so it is customers responsibility to either configure Si5338A during FSBL or then use Silicon Labs programmer and burn the OTP ROM with customer fixed clock setup.

Si5338A OTP can only be programmed two times, as different user configurations may require different setup, TE0803 is normally shipped with blank OTP.
Refer to Si5338A datasheet for more information.

5.4 Clocking

The TE0803-01 SoM is equipped with two on-board oscillators to provide the Zynq MPSoC's PS configuration bank 503 with reference clock signals.

Clock	Frequency	Bank 503 Pin	Connected to
PS_CLK	33.333333 MHz	R16	MEMS oscillator, U32
PS_PAD (RTC)	32.768 kHz	N17/N18	Quartz crystal, Y2

Table 13: Reference clock-signals to PS configuration bank 503

5.5 On-board LEDs

LED	Color	Connected to	Description and Notes
D1	Red	DONE signal (PS Configuration Bank 503)	This LED goes ON when power has been applied to the module and stays ON until MPSoC's programmable logic is configured properly.

Table 14: LED's description

6 Power and Power-On Sequence

6.1 Power Consumption

The maximum power consumption of a module mainly depends on the design which is running on the FPGA.

Xilinx provide a power estimator excel sheets to calculate power consumption. It's also possible to evaluate the power consumption of the developed design with Vivado. See also Trenz Electronic Wiki FAQ.

Power Input Pin	Typical Current
DCDCIN	TBD*
LP_DCDC	TBD*
PL_DCIN	TBD*
PS_BATT	TBD*

Table 15: Maximum current of power supplies. *To Be Determined soon with reference design setup.

Power supply with minimum current capability of 3A for system startup is recommended. For the lowest power consumption and highest efficiency of on board DC/DC regulators it is recommended to powering the module from one single 3.3V supply. Except 'PS_BATT', all input power supplies have a nominal value of 3.3V. Although the input power supplies can be powered up in any order, it is recommended to power them up simultaneously.

The TE0803 module equipped with the Xilinx Zynq UltraScale+ MPSoC delivers a heterogeneous multi-processing system with integrated programmable logic and independently operable elements and is designed to meet embedded system power management requirement by advanced power management features. This features allow to offset the power and heat constraints against overall performance and operational efficiency.

This features allowing highly flexible power management are achieved by establishing Power Domains for power isolation. The Zynq UltraScale+ MPSoC has multiple power domains, whereby each power domain requires its own particular external DC-DC converters.

The Processing System contains three Power Domains:

- Battery Power Domain (BBRAM and RTC)
- Full-Power Domain (Application Processing Unit, DDR Controller, Graphics Processing Unit and High-Speed Connectivity)
- Low-Power Domain (Real-Time Processing Unit, Security and Configuration Unit, Platform Management Unit, System Monitor and General Connectivity)

The fourth Power Domain is for the Programmable Logic (PL). If individual Power Domain control is not required, power rails can be shared between domains.

On the TE0803 SoM, following Power Domains can be powered up individually with power rails available on the B2B connectors:

- Full-Power Domain, supplied by power rail **'DCDCIN'**
- Low-Power Domain, supplied by power rail **'LP_DCDC'**
- Programmable Logic, supplied by power rail **'PL_DCIN'**
- Battery Power Domain, supplied by power rail **'PS_BATT'**

Each Power Domain has its own "Enabling"- and "Power Good"-signals. The power rail **'GT_DCDC'** is only necessary for variants of the TE0803 module with the Xilinx Zynq UltraScale+ ZU4CG or ZU4EV MPSoC to generate the voltages for the available Xilinx GTH unit.

6.2 Power Distribution Dependencies

The power rails 'DCDCIN', 'LP_DCDC', 'PL_DCIN', 'PS_BATT' have to be powered up on the assigned pins of the B2B connectors as listed on the section "Power Rails". Except 'PS_BATT' (see section "Recommended Operation Conditions"), all power-rails can be powered up, with 3.3V power sources, also shared, if Power Domain control is not required.

There are following dependencies how the initial voltages of the power rails on the B2B connectors are distributed to the on-board DC-DC converters, which power up further DC-DC converters and the particular on-board voltages:

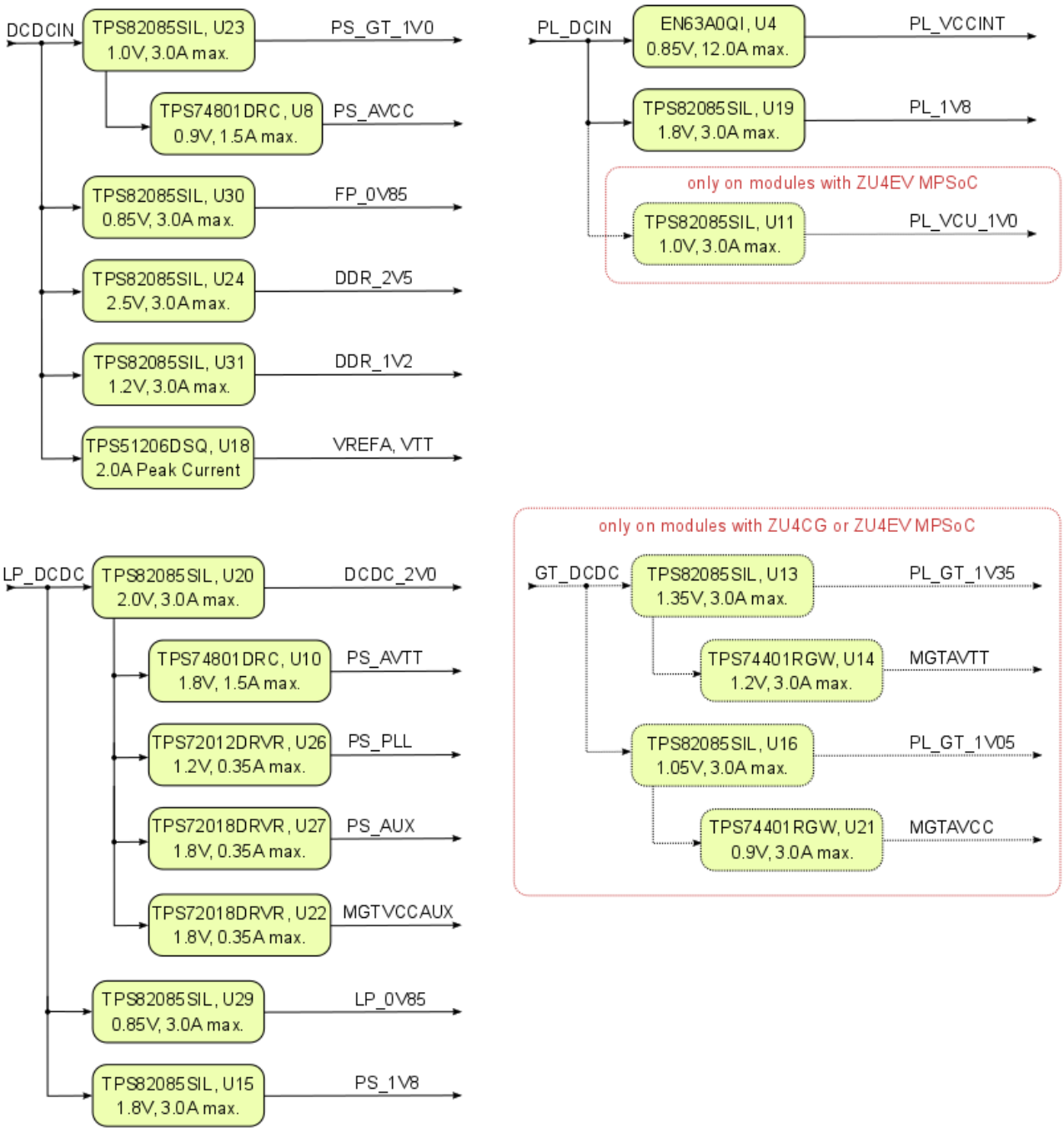


Figure 3: Power Distribution Diagram

Current rating of Samtec Razor Beam LP Terminal/Socket Strip ST5/SS5 B2B connectors is 1.5 A per pin (1 pin powered per row).

6.3 Power-On Sequence Diagram

The TE0803 SoM meets the recommended criteria to power up the Xilinx Zynq UltraScale+ MPSoC properly by keeping a specific sequence of enabling the on-board DC-DC converters dedicated to the particular Power Domains and powering up the on-board voltages.

The on-board voltages of the TE0803 SoM will be powered-up in order of a determined sequence by activating the above-mentioned power rails and the Enable-Signals of the DC-DC converters. The on-board voltages will be powered up at three steps.

1. Low-Power Domain (LPD)
2. Programmable Logic (PL) and Full-Power Domain (FPD)
3. PS GTR transceiver and DDR memory (additionally GTH transceiver at modules with ZU5EV MPSoC)

Hence, those three power instances will be powered up consecutively and the Power-Good-Signals of the previous instance has to be asserted.

Following diagram clarifies the sequence of enabling the three power instances utilizing the DC-DC converter control signals ('Enable', 'Power-Good'), which will power-up in descending order as listed in the blocks of the diagram.

EN_PL	J2-101	max PL_DCIN	Left floating for logic high (drive to GND for logic low)	PG_PL	J2-104	External pull-up needed (max. voltage 'GT_DCDC'), Max. sink current 1 mA	TPS82085SIL / NC7S08P5X datasheet
EN_DDR	J2-112	DCDCIN	NC7S08P5X data sheet	PG_DDR	J2-114	4K7, pulled up to DCDCIN	-
EN_PSGT	J2-84	DCDCIN	NC7S08P5X data sheet	PG_PSGT	J2-82	External pull-up needed (max. 5.5V), Max. sink current 1 mA	TPS74801 datasheet
EN_GT_R	J2-95	GT_DCDC	NC7S08P5X data sheet	PG_GT_R	J2-91	External pull-up needed (max. 5.5V), Max. sink current 1 mA	TPS74401 datasheet
-	-	-	-	PG_VCU_1V0	J2-97	External pull-up needed (max. 5.5V), Max. sink current 1 mA	TPS82085SIL datasheet

Table 16: Recommended operation conditions of DC-DC converter control signals

To avoid any damage to the MPSoC module, check for stabilized on-board voltages in steady state before powering up the MPSoC's I/O bank voltages VCCOx. All I/O's should be tri-stated during power-on sequence.

Core voltages and main supply voltages have to reach stable state and their "Power Good" signals have to be asserted before other voltages like bank I/O voltages (VCCOx) can be powered up.

It is important that all PS and PL I/Os are tri-stated at power-on until the "Power Good" signals are high, meaning that all on-module voltages have become stable and module is properly powered up.

See Xilinx datasheet DS925 for additional information. User should also check related base board documentation when intending base board design for TE0803 SoM.

6.5 Voltage Monitor Circuit

The voltages 'LP_DCDC' and 'LP_0V85' are monitored by the voltage monitor circuit U41, which generates the POR_B reset signal at Power-On. A manual reset is also possible by driving the MR-pin (J2-83) to GND. Leave this pin unconnected or connect to VDD (LP_DCDC) when unused.

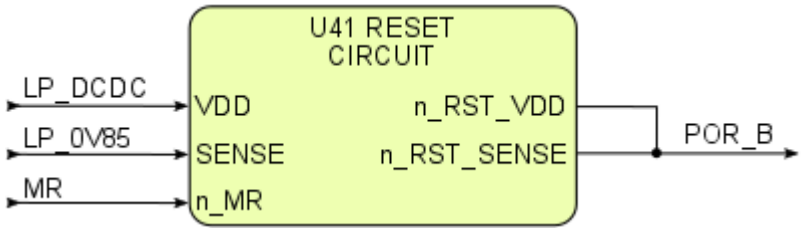


Figure 5: Voltage monitor circuit

6.6 Power Rails

Voltages on B2B Connectors	B2B J1 Pin	B2B J2 Pin	B2B J3 Pin	B2B J4 Pin	Input / Output	Note
PL_DCIN	J1-151, J1-153, J1-157, J1-159	-	-	-	Input	-
DCDCIN	-	J2-154, J2-156, J2-158, J2-160, J2-153, J2-155, J2-157, J2-159	-	-	Input	-
LP_DCDC	-	J2-138, J2-140, J2-142, J2-144	-	-	Input	-
PS_BATT	-	J2-125	-	-	Input	-
GT_DCDC	-	-	J3-157, J3-158, J3-159, J3-160	-	Input	-
PS_1V8	-	J2-99	J3-148	-	Output	Internal voltage level 1.8V nominal output
PL_1V8	J1-91, J1-121	-	-	-	Output	Internal voltage level 1.8V nominal output
DDR_1V2	-	J2-135	-	-	Output	Internal voltage level 1.2V nominal output

Table 17: Power rails of the MPSoC module on accessible connectors

6.7 Bank Voltages

Bank	Type	Schematic Name / B2B Connector Pins	Voltage	Reference Input Voltage	Voltage Range
25	HD	VCCO25, pins J3-15, J3-16	User	-	Max. 3.3V
26	HD	VCCO26, pins J3-43, J3-44	User	-	Max. 3.3V

7 B2B connectors

5.2 x 7.6 cm UltraSoM+ modules use four Samtec Razor Beam LP Terminal Strip (ST5) on the bottom side.

- 4x REF-192552-02 (160-pins)
  - ST5 Mates with SS5

5.2 x 7.6 cm UltraSoM+ carrier use four Samtec Razor Beam LP Socket Strip (SS5) on the top side.

- 4x REF192552-01 (160-pins)
  - SS5 Mates with ST5

7.1 Features

- Board-to-Board Connector 160-pins, 80 contacts per row
- Ultrafine .0197" (0.50 mm) pitch
- Narrow body design saves space on board
- Lead style -03.5
- Samtec 28+ Gbps Solution
- Mates with: ST5
- Insulator Material: Liquid Crystal Polymer, schwarz
- Operating Temperature Range: -55°C bis +125°C
- Lead-Free Solderable: Yes
- RoHS Konform: Yes

7.2 Connector Stacking height

When using the standard type on baseboard and module, the mating height is 5 mm.

Other mating heights are possible by using connectors with a different height:

Order number	REF number	Samtec Number	Type	Contribution to stacking height	Comment
27219	REF192552-01	SS5-80-3.50-L-D-K-TR	Baseboard connector	3.5mm	Standard connector used on modules
27018	REF-189545-02	SS5-80-3.00-L-D-K-TR	Baseboard connector	3 mm	Assembly option on request
27220	REF-192552-02	ST5-80-1.50-L-D-P-TR	Module connector	1.5 mm	Standard connector used on modules
27017	REF-189545-01	ST5-80-1.00-L-D-P-TR	Module connector	1 mm	Assembly option on request

The module can be manufactured using other connectors upon request.

7.3 Current Rating

Current rating of Samtec Razor Beam LP Terminal/Socket Strip ST5/SS5 B2B connectors is 1.5 A per pin (1 pin powered per row).

9 Technical Specifications

9.1 Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes / Reference Document
PL_DCIN	-0.3	7	V	TPS82085SIL / EN63A0QI data sheet
DCDCIN	-0.3	7	V	TPS82085SIL / TPS51206PSQ data sheet
LP_DCDC	-0.3	4	V	TPS3106K33DBVR data sheet
GT_DCDC	-0.3	7	V	TPS82085SIL data sheet
PS_BATT	-0.5	2	V	Xilinx DS925 data sheet
VCCO for HD I/O banks	-0.5	3.4	V	Xilinx DS925 data sheet
VCCO for HP I/O banks	-0.5	2	V	Xilinx DS925 data sheet
VREF	-0.5	2	V	Xilinx DS925 data sheet
I/O input voltage for HD I/O banks	-0.55	VCCO + 0.55	V	Xilinx DS925 data sheet
I/O input voltage for HP I/O banks	-0.55	VCCO + 0.55	V	Xilinx DS925 data sheet
PS I/O input voltage (MIO pins)	-0.5	VCCO_PSIO + 0.55	V	Xilinx DS925 data sheet, VCCO_PSIO 1.8V nominally
Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage	-0.5	1.2	V	Xilinx DS925 data sheet
Voltage on input pins of NC7S08P5X 2-Input AND Gate	-0.5	VCC + 0.5	V	NC7S08P5X data sheet, see schematic for VCC
Voltage on input pins (nMR) of TPS3106K33DBVR Voltage Monitor, U41	-0.3	VDD + 0.3	V	TPS3106 data sheet, VDD = LP_DCDC
"Enable"-signals on TPS82085SIL ('EN_LPD')	-0.3	7	V	TPS82085SIL data sheet
Storage temperature (ambient)	-40	100	°C	ROHM Semiconductor SML-P11 Series data sheet

⚠ Assembly variants for higher storage temperature range are available on request.

9.2 Recommended Operating Conditions

Parameter	Min	Max	Unit	Notes / Reference Document
PL_DCIN	2.5	6	V	EN63A0QI / TPS82085SIL data sheet

Parameter	Min	Max	Unit	Notes / Reference Document
DCDCIN	3.1	6	V	TPS82085SIL / TPS51206PSQ data sheet
LP_DCDC	2.5	3.6	V	TPS82085SIL / TPS3106K33DBVR data sheet
GT_DCDC	2.5	6	V	TPS82085SIL data sheet
PS_BATT	1.2	1.5	V	Xilinx DS925 data sheet
VCCO for HD I/O banks	1.14	3.4	V	Xilinx DS925 data sheet
VCCO for HP I/O banks	0.95	1.9	V	Xilinx DS925 data sheet
I/O input voltage for HD I/O banks.	-0.2	VCCO + 0.2	V	Xilinx DS925 data sheet
I/O input voltage for HP I/O banks	-0.2	VCCO + 0.2	V	Xilinx DS925 data sheet
PS I/O input voltage (MIO pins)	-0.2	VCCO_PSIO + 0.2	V	Xilinx DS925 data sheet, VCCO_PSIO 1.8V nominally
Voltage on input pins of NC7S08P5X 2-Input AND Gate	0	VCC	V	NC7S08P5X data sheet, see schematic for connected VCCs
Voltage on input pins (MR) of TPS3106K33DBVR Voltage Monitor, U41	0	VDD	V	TPS3106 data sheet, VDD = LP_DCDC

⚠ Please check Xilinx datasheet DS925 for complete list of absolute maximum and recommended operating ratings.

9.3 Operating Temperature Ranges

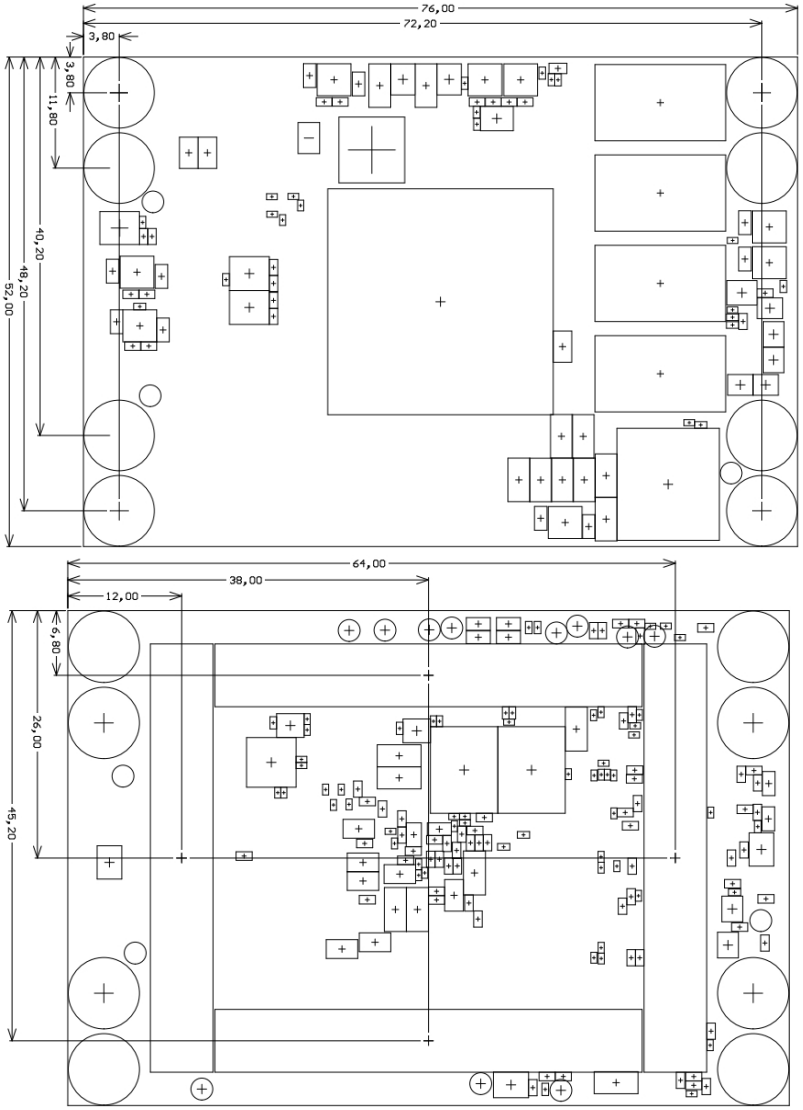
Extended grade: 0°C to +100°C.

The module operating temperature range depends also on customer design and cooling solution. Please contact us for options.

9.4 Physical Dimensions

- Module size: 52 mm × 76 mm. Please download the assembly diagram for exact numbers
- Mating height with standard connectors: 4mm
- PCB thickness: 1.6mm
- Highest part on PCB: approx. 3mm. Please download the step model for exact numbers

All dimensions are given in millimeters.



any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.