Trenz Electronic GmbH - TE0803-01-03CG-1EA Datasheet

Welcome to E-XFL.COM

Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Discontinued at Digi-Key
Module/Board Type	MPU Core
Core Processor	Zynq UltraScale+ XCZU3CG-1SFVC784E
Co-Processor	-
Speed	-
Flash Size	128MB
RAM Size	2GB
Connector Type	B2B
Size / Dimension	2.99" x 2.05" (76mm x 52mm)
Operating Temperature	0°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0803-01-03cg-1ea

1 Table of Contents

2 Overview

Refer to "https://shop.trenz-electronic.de/en/Download/?path=Trenz_Electronic/TE0803" for downloadable version of this manual and the rest of available documentation.The Trenz Electronic TE0803 is an industrial-grade MPSoC SoM integrating a Xilinx Zynq UltraScale+, max. 8 GByte DDR4 SDRAM with 64-Bit width data bus connection, max. 512 MByte SPI Boot Flash memory for configuration and operation, up to 8 Gigabit transceivers and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/O's is provided via rugged high-speed stacking connections.

All this in a compact 5.2 x 7.6 cm form factor, at the most competitive price

2.1 Key Features

- Xilinx Zynq UltraScale+ MPSoC 784 pin package (options: ZU2CG, ZU2EG, ZU3CG, ZU3EG, ZU4CG, ZU4EV)
- Memory
  - 64-Bit DDR4, 8 GByte maximum
  - Dual SPI boot Flash in parallel, 512 MByte maximum
- User I/O
  - 65 x MIO, 48 x HD (all), 156 x HP (3 banks)
  - Serial transceiver: 4 x GTR (+ 4 x GTH transceiver with ZU4CG or ZU4EV MPSoC)
  - Transceiver clocks inputs and outputs
  - PLL clock generator inputs and outputs
- Size: 52 x 76 mm, 3 mm mounting holes for skyline heat spreader
- B2B connectors: 4 x 160 pin
- Si5338A - 4 output PLL
- All power supplies on board, single 3.3V power source required
  - LP, FP, PL separately controlled power domains
- Support for all boot modes (except NAND) and scenarios
- Support for any combination of PS connected peripherals

2.3 Main Components

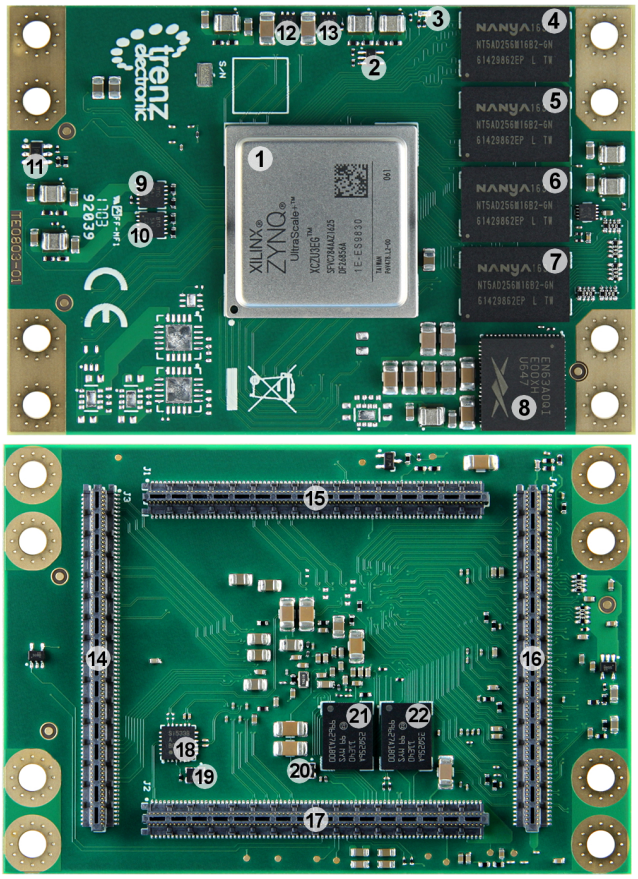


Figure 2: TE0803-01 MPSoC module

1. Xilinx ZYNQ UltraScale+ MPSoC, U1
2. 2-Input AND Gate, U39
3. Red LED (DONE), D1
4. 256Mx16 DDR4-2400 SDRAM, U12
5. 256Mx16 DDR4-2400 SDRAM, U9
6. 256Mx16 DDR4-2400 SDRAM, U2
7. 256Mx16 DDR4-2400 SDRAM, U3
8. 12A PowerSoC DC-DC converter, U4
9. 1.5A LDO DC-DC converter, U10
10. 1.5A LDO DC-DC converter, U8
11. Voltage monitor circuit, U41
12. 0.35A LDO DC-DC converter, U26
13. 0.35A LDO DC-DC converter, U27
14. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J3
15. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J1
16. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J4
17. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J2
18. 4-channel programmable PLL clock generator, U5
19. Low-power programmable oscillator @ 25.000000 MHz, U5
20. Low-power programmable oscillator @ 33.333333 MHz (PS_CLK), U32
21. 256 Mbit serial NOR Flash memory, U7
22. 256 Mbit serial NOR Flash memory, U17

Bank	Type	B2B Connector	Schematic Names / Connector Pins	I/O Signal Count	LVDS Pairs Count	VCCO Bank Voltage	Notes
501	MIO	J3	MIO26 ... MIO51	26 I/O's	-	PS_1V8	user configurable I/O's on B2B
502	MIO	J3	MIO52 ... MIO77	26 I/O's	-	PS_1V8	user configurable I/O's on B2B

Table 2: B2B connector pin-outs of available PL and PS banks of the TE0803-01 SoM

1) Bank 25 at XC**ZU2** / XC**ZU3**, else Bank 45 at XC**ZU4** / XC**ZU5**

2) Bank 26 at XC**ZU2** / XC**ZU3**, else Bank 46 at XC**ZU4** / XC**ZU5**

All MIO banks are powered from on-module DC-DC power rail. All PL I/O banks have separate VCCO input pins in the B2B connectors, valid VCCO should be supplied from the carrier board.

For detailed information about the B2B pin-out, please refer to the Pin-out table.

The configuration of the I/O's MIO13 - MIO77 are depending on the base-board peripherals connected to these pins.

3.2 MGT Lanes

The B2B connectors J1 and J2 provide also access to the MGT banks of the Zynq UltraScale+ MPSoC. There are 8 high-speed data lanes (Xilinx GTH / GTR transceiver) available composed as differential signaling pairs for both directions (RX/TX).

The MGT banks have also clock input-pins which are exposed to the B2B connectors J2 and J3. Following MGT lanes are available on the B2B connectors:

Bank	Type	B2B Connector	Count of MGT Lanes	Schematic Names / Connector Pins	MGT Bank's Reference Clock Inputs
224 [1]	GTH	J1	4 GTH lanes (4 RX / 4TX)	B224_RX3_P, B224_RX3_N, pins J1-51, J1-53 B224_TX3_P, B224_TX3_N, pins J1-50, J1-52 B224_RX2_P, B224_RX2_N, pins J1-57, J1-59 B224_TX2_P, B224_TX2_N, pins J1-56, J1-58 B224_RX1_P, B224_RX1_N, pins J1-63, J1-65 B224_TX1_P, B224_TX1_N, pins J1-62, J1-64 B224_RX0_P, B224_RX0_N, pins J1-69, J1-71 B224_TX0_P, B224_TX0_N, pins J1-68, J1-70	1 reference clock signal (B224_CLK0) from B2B connector J3 (pins J3-59/J3-61) to bank's pins Y6/Y5 1 reference clock signal (B224_CLK1) from programmable PLL clock generator U5 to bank's pins V6/V5
505	GTR	J2	4 GTR lanes (4 RX / 4TX)	B505_RX3_P, B505_RX3_N, pins J2-51, J2-49 B505_TX3_P, B505_TX3_N, pins J2-54, J2-52 B505_RX2_P, B505_RX2_N, pins J2-57, J2-55 B505_TX2_P, B505_TX2_N, pins J2-60, J2-58 B505_RX1_P, B505_RX1_N, pins J2-63, J2-61 B505_TX1_P, B505_TX1_N, pins J2-66, J2-64 B505_RX0_P, B505_RX0_N, pins J2-69, J2-67 B505_TX0_P, B505_TX0_N, pins J2-72, J2-70	2 reference clock signals (B505_CLK0, B505_CLK1) from B2B connector J2 (pins J2-16/J2-18, J2-10/J2-12) to bank's pins F23/F24, E21/E22 2 reference clock signals (B505_CLK2, B505_CLK3) from programmable PLL clock generator U5 to bank's pins C21/C22, A21/A22

Table 3: B2B connector pin-outs of available MGT lanes of the MPSoC

1) Bank 224 only available at XC**ZU4** / XC**ZU5** MPSoC.

3.3 JTAG Interface

JTAG access is provided through the MPSoC's PS configuration bank 503 with bank voltage 'PS_1V8'.

MIO	U7 Pin	Pin Name	MIO	U17 Pin	Pin Name
0	B2	CLK	7	C2	CS#
1	D2	DO/IO1	8	D3	DI/IO0
2	C4	WP#/IO2	9	D2	DO/IO1
3	D4	HOLD#/IO3	10	C4	WP#/IO2
4	D3	DI/IO0	11	D4	HOLD#/IO3
5	C2	CS#	12	B2	CLK

Table 7: MIO pin assignment of the Quad SPI Flash memory ICs

5 On-board Peripherals

5.1 Flash

The TE0803 SoM can be configured with max. 512 MByte Flash memory for configuration and operation.

Name	IC	Designator	PS7	MIO	Notes
SPI Flash	N25Q256A11E1240E	U7	QSPI0	MIO0 ... MIO5	Dual parallel booting possible, 32 MByte memory per Flash IC at standard configuration
SPI Flash	N25Q256A11E1240E	U17	QSPI0	MIO7 ... MIO12	As above

Table 10: Peripherals connected to the PS MIO pins

5.2 DDR4 SDRAM

The TE0803-01 SoM is equipped with with four DDR4-2400 SDRAM modules with up to 8 GByte of memory. The SDRAM modules are connected to the Zynq MPSoC's PS DDR controller (bank 504) via 64-bit wide data bus.

Refer to the Xilinx Zynq UltraScale+ datasheet DS925 for more information, if the specific Zynq UltraScale+ MPSoC chip on module supports the maximum data transmission rate of 2400 MByte/s.

5.3 Programmable PLL Clock Generator

Following table illustrates on-board Si5338A programmable clock multiplier chip inputs and outputs:

Input	Connected to	Frequency	Notes
IN1 / IN2	B2B Connector pins J2-4, J2-6 (differential pair)	User	AC decoupling required on base
IN3	On-board Oscillator (U6)	25.000000 MHz	-
Output	**Connected to**	**Frequency**	**Notes**
CLK0 A/B	B2B Connector pins J2-1, J2-3 (differential pair)	User	Default off
CLK1 A/B	B224 CLK1 (only available at ZU5EV MPSoC)	User	Default off
CLK2 A/B	B505 CLK3	User	Default off
CLK3 A/B	B505 CLK2	User	Default off

Table 11: Programmable PLL clock generator input/output

The Si5338A programmable clock generator's control interface pins are exposed to B2B connector J2. For further information refer to the Si5338A data sheet.

Signal	B2B Connector pin	Function
PLL_SCL / PLL_SDA	J2-90 / J2-92	I^2C interface, external pull-ups needed for SCL/SDA line. I^2C address in current configuration: 1110000b

Table 12: B2B connector pin-out of Si5338A control interface

> ⚠ Si5338A OTP ROM is not programmed by default at delivery, so it is customers responsibility to either configure Si5338A during FSBL or then use Silicon Labs programmer and burn the OTP ROM with customer fixed clock setup.

Si5338A OTP can only be programmed two times, as different user configurations may require different setup, TE0803 is normally shipped with blank OTP.
Refer to Si5338A datasheet for more information.

5.4 Clocking

The TE0803-01 SoM is equipped with two on-board oscillators to provide the Zynq MPSoC's PS configuration bank 503 with reference clock signals.

Clock	Frequency	Bank 503 Pin	Connected to
PS_CLK	33.333333 MHz	R16	MEMS oscillator, U32
PS_PAD (RTC)	32.768 kHz	N17/N18	Quartz crystal, Y2

Table 13: Reference clock-signals to PS configuration bank 503

5.5 On-board LEDs

LED	Color	Connected to	Description and Notes
D1	Red	DONE signal (PS Configuration Bank 503)	This LED goes ON when power has been applied to the module and stays ON until MPSoC's programmable logic is configured properly.

Table 14: LED's description

Current rating of Samtec Razor Beam LP Terminal/Socket Strip ST5/SS5 B2B connectors is 1.5 A per pin (1 pin powered per row).

6.3 Power-On Sequence Diagram

The TE0803 SoM meets the recommended criteria to power up the Xilinx Zynq UltraScale+ MPSoC properly by keeping a specific sequence of enabling the on-board DC-DC converters dedicated to the particular Power Domains and powering up the on-board voltages.

The on-board voltages of the TE0803 SoM will be powered-up in order of a determined sequence by activating the above-mentioned power rails and the Enable-Signals of the DC-DC converters. The on-board voltages will be powered up at three steps.

1. Low-Power Domain (LPD)
2. Programmable Logic (PL) and Full-Power Domain (FPD)
3. PS GTR transceiver and DDR memory (additionally GTH transceiver at modules with ZU5EV MPSoC)

Hence, those three power instances will be powered up consecutively and the Power-Good-Signals of the previous instance has to be asserted.

Following diagram clarifies the sequence of enabling the three power instances utilizing the DC-DC converter control signals ('Enable', 'Power-Good'), which will power-up in descending order as listed in the blocks of the diagram.

EN_PL	J2-101	max PL_DCIN	Left floating for logic high (drive to GND for logic low)	PG_PL	J2-104	External pull-up needed (max. voltage 'GT_DCDC'), Max. sink current 1 mA	TPS82085SIL / NC7S08P5X datasheet
EN_DDR	J2-112	DCDCIN	NC7S08P5X data sheet	PG_DDR	J2-114	4K7, pulled up to DCDCIN	-
EN_PSGT	J2-84	DCDCIN	NC7S08P5X data sheet	PG_PSGT	J2-82	External pull-up needed (max. 5.5V), Max. sink current 1 mA	TPS74801 datasheet
EN_GT_R	J2-95	GT_DCDC	NC7S08P5X data sheet	PG_GT_R	J2-91	External pull-up needed (max. 5.5V), Max. sink current 1 mA	TPS74401 datasheet
-	-	-	-	PG_VCU_1V0	J2-97	External pull-up needed (max. 5.5V), Max. sink current 1 mA	TPS82085SIL datasheet

Table 16: Recommended operation conditions of DC-DC converter control signals

To avoid any damage to the MPSoC module, check for stabilized on-board voltages in steady state before powering up the MPSoC's I/O bank voltages VCCOx. All I/O's should be tri-stated during power-on sequence.

Core voltages and main supply voltages have to reach stable state and their "Power Good" signals have to be asserted before other voltages like bank I/O voltages (VCCOx) can be powered up.

It is important that all PS and PL I/Os are tri-stated at power-on until the "Power Good" signals are high, meaning that all on-module voltages have become stable and module is properly powered up.

See Xilinx datasheet DS925 for additional information. User should also check related base board documentation when intending base board design for TE0803 SoM.

6.5 Voltage Monitor Circuit

The voltages 'LP_DCDC' and 'LP_0V85' are monitored by the voltage monitor circuit U41, which generates the POR_B reset signal at Power-On. A manual reset is also possible by driving the MR-pin (J2-83) to GND. Leave this pin unconnected or connect to VDD (LP_DCDC) when unused.

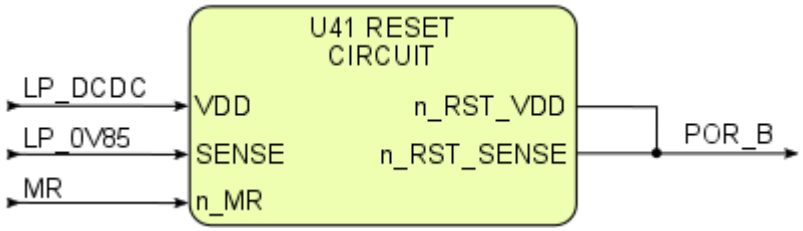


Figure 5: Voltage monitor circuit

6.6 Power Rails

Voltages on B2B Connectors	B2B J1 Pin	B2B J2 Pin	B2B J3 Pin	B2B J4 Pin	Input / Output	Note
PL_DCIN	J1-151, J1-153, J1-157, J1-159	-	-	-	Input	-
DCDCIN	-	J2-154, J2-156, J2-158, J2-160, J2-153, J2-155, J2-157, J2-159	-	-	Input	-
LP_DCDC	-	J2-138, J2-140, J2-142, J2-144	-	-	Input	-
PS_BATT	-	J2-125	-	-	Input	-
GT_DCDC	-	-	J3-157, J3-158, J3-159, J3-160	-	Input	-
PS_1V8	-	J2-99	J3-148	-	Output	Internal voltage level 1.8V nominal output
PL_1V8	J1-91, J1-121	-	-	-	Output	Internal voltage level 1.8V nominal output
DDR_1V2	-	J2-135	-	-	Output	Internal voltage level 1.2V nominal output

Table 17: Power rails of the MPSoC module on accessible connectors

6.7 Bank Voltages

Bank	Type	Schematic Name / B2B Connector Pins	Voltage	Reference Input Voltage	Voltage Range
25	HD	VCCO25, pins J3-15, J3-16	User	-	Max. 3.3V
26	HD	VCCO26, pins J3-43, J3-44	User	-	Max. 3.3V

Bank	Type	Schematic Name / B2B Connector Pins	Voltage	Reference Input Voltage	Voltage Range
64	HP	VCCO64, J4-58, J4-106	User	VREF_64, pin J4-88	Max. 1.8V
65	HP	VCCO65, J4-69, J4-105	User	VREF_65, pin J4-15	Max. 1.8V
66	HP	VCCO66, J1-90, J1-120	User	VREF_66, pin J1-108	Max. 1.8V
500	MIO	PS_1V8	1.8V	-	-
501	MIO	PS_1V8	1.8V	-	-
502	MIO	PS_1V8	1.8V	-	-
503	CONFIG	PS_1V8	1.8V	-	-

Table 18: Range of MPSoC module's bank voltages

7 B2B connectors

5.2 x 7.6 cm UltraSoM+ modules use four Samtec Razor Beam LP Terminal Strip (ST5) on the bottom side.

- 4x REF-192552-02 (160-pins)
  - ST5 Mates with SS5

5.2 x 7.6 cm UltraSoM+ carrier use four Samtec Razor Beam LP Socket Strip (SS5) on the top side.

- 4x REF192552-01 (160-pins)
  - SS5 Mates with ST5

7.1 Features

- Board-to-Board Connector 160-pins, 80 contacts per row
- Ultrafine .0197" (0.50 mm) pitch
- Narrow body design saves space on board
- Lead style -03.5
- Samtec 28+ Gbps Solution
- Mates with: ST5
- Insulator Material: Liquid Crystal Polymer, schwarz
- Operating Temperature Range: -55°C bis +125°C
- Lead-Free Solderable: Yes
- RoHS Konform: Yes

7.2 Connector Stacking height

When using the standard type on baseboard and module, the mating height is 5 mm.

Other mating heights are possible by using connectors with a different height:

Order number	REF number	Samtec Number	Type	Contribution to stacking height	Comment
27219	REF192552-01	SS5-80-3.50-L-D-K-TR	Baseboard connector	3.5mm	Standard connector used on modules
27018	REF-189545-02	SS5-80-3.00-L-D-K-TR	Baseboard connector	3 mm	Assembly option on request
27220	REF-192552-02	ST5-80-1.50-L-D-P-TR	Module connector	1.5 mm	Standard connector used on modules
27017	REF-189545-01	ST5-80-1.00-L-D-P-TR	Module connector	1 mm	Assembly option on request

The module can be manufactured using other connectors upon request.

7.3 Current Rating

Current rating of Samtec Razor Beam LP Terminal/Socket Strip ST5/SS5 B2B connectors is 1.5 A per pin (1 pin powered per row).

7.4 Connector Speed Ratings

The connector speed rating depends on the stacking height:

Stacking height	Speed rating
4 mm, Single-Ended	13GHz/26Gbps
4 mm, Differential	13.5GHz/27Gbps
5 mm, Single-Ended	13.5GHz/27Gbps
5 mm, Differential	20GHz/40 Gbps

The SS5/ST5 series board-to-board spacing is currently available in 4mm (0.157"), 4.5mm (0.177") and 5mm (0.197") stack heights.

The data in the reports is applicable only to the 4mm and 5mm board-to-board mated connector stack height.

7.5 Manufacturer Documentation

Geändert
30 05, 2017 by Susanne Kunath
30 05, 2017 by Susanne Kunath
13 11, 2017 by John Hartfiel
13 11, 2017 by John Hartfiel
13 11, 2017 by John Hartfiel
13 11, 2017 by John Hartfiel
13 11, 2017 by John Hartfiel
13 11, 2017 by John Hartfiel
13 11, 2017 by John Hartfiel

8 Variants Currently In Production

Trenz shop TE0803 overview page	
English page	German page

9 Technical Specifications

9.1 Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes / Reference Document
PL_DCIN	-0.3	7	V	TPS82085SIL / EN63A0QI data sheet
DCDCIN	-0.3	7	V	TPS82085SIL / TPS51206PSQ data sheet
LP_DCDC	-0.3	4	V	TPS3106K33DBVR data sheet
GT_DCDC	-0.3	7	V	TPS82085SIL data sheet
PS_BATT	-0.5	2	V	Xilinx DS925 data sheet
VCCO for HD I/O banks	-0.5	3.4	V	Xilinx DS925 data sheet
VCCO for HP I/O banks	-0.5	2	V	Xilinx DS925 data sheet
VREF	-0.5	2	V	Xilinx DS925 data sheet
I/O input voltage for HD I/O banks	-0.55	VCCO + 0.55	V	Xilinx DS925 data sheet
I/O input voltage for HP I/O banks	-0.55	VCCO + 0.55	V	Xilinx DS925 data sheet
PS I/O input voltage (MIO pins)	-0.5	VCCO_PSIO + 0.55	V	Xilinx DS925 data sheet, VCCO_PSIO 1.8V nominally
Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage	-0.5	1.2	V	Xilinx DS925 data sheet
Voltage on input pins of NC7S08P5X 2-Input AND Gate	-0.5	VCC + 0.5	V	NC7S08P5X data sheet, see schematic for VCC
Voltage on input pins (nMR) of TPS3106K33DBVR Voltage Monitor, U41	-0.3	VDD + 0.3	V	TPS3106 data sheet, VDD = LP_DCDC
"Enable"-signals on TPS82085SIL ('EN_LPD')	-0.3	7	V	TPS82085SIL data sheet
Storage temperature (ambient)	-40	100	°C	ROHM Semiconductor SML-P11 Series data sheet

⚠ Assembly variants for higher storage temperature range are available on request.

9.2 Recommended Operating Conditions

Parameter	Min	Max	Unit	Notes / Reference Document
PL_DCIN	2.5	6	V	EN63A0QI / TPS82085SIL data sheet

Parameter	Min	Max	Unit	Notes / Reference Document
DCDCIN	3.1	6	V	TPS82085SIL / TPS51206PSQ data sheet
LP_DCDC	2.5	3.6	V	TPS82085SIL / TPS3106K33DBVR data sheet
GT_DCDC	2.5	6	V	TPS82085SIL data sheet
PS_BATT	1.2	1.5	V	Xilinx DS925 data sheet
VCCO for HD I/O banks	1.14	3.4	V	Xilinx DS925 data sheet
VCCO for HP I/O banks	0.95	1.9	V	Xilinx DS925 data sheet
I/O input voltage for HD I/O banks.	-0.2	VCCO + 0.2	V	Xilinx DS925 data sheet
I/O input voltage for HP I/O banks	-0.2	VCCO + 0.2	V	Xilinx DS925 data sheet
PS I/O input voltage (MIO pins)	-0.2	VCCO_PSIO + 0.2	V	Xilinx DS925 data sheet, VCCO_PSIO 1.8V nominally
Voltage on input pins of NC7S08P5X 2-Input AND Gate	0	VCC	V	NC7S08P5X data sheet, see schematic for connected VCCs
Voltage on input pins (MR) of TPS3106K33DBVR Voltage Monitor, U41	0	VDD	V	TPS3106 data sheet, VDD = LP_DCDC

⚠ Please check Xilinx datasheet DS925 for complete list of absolute maximum and recommended operating ratings.

9.3 Operating Temperature Ranges

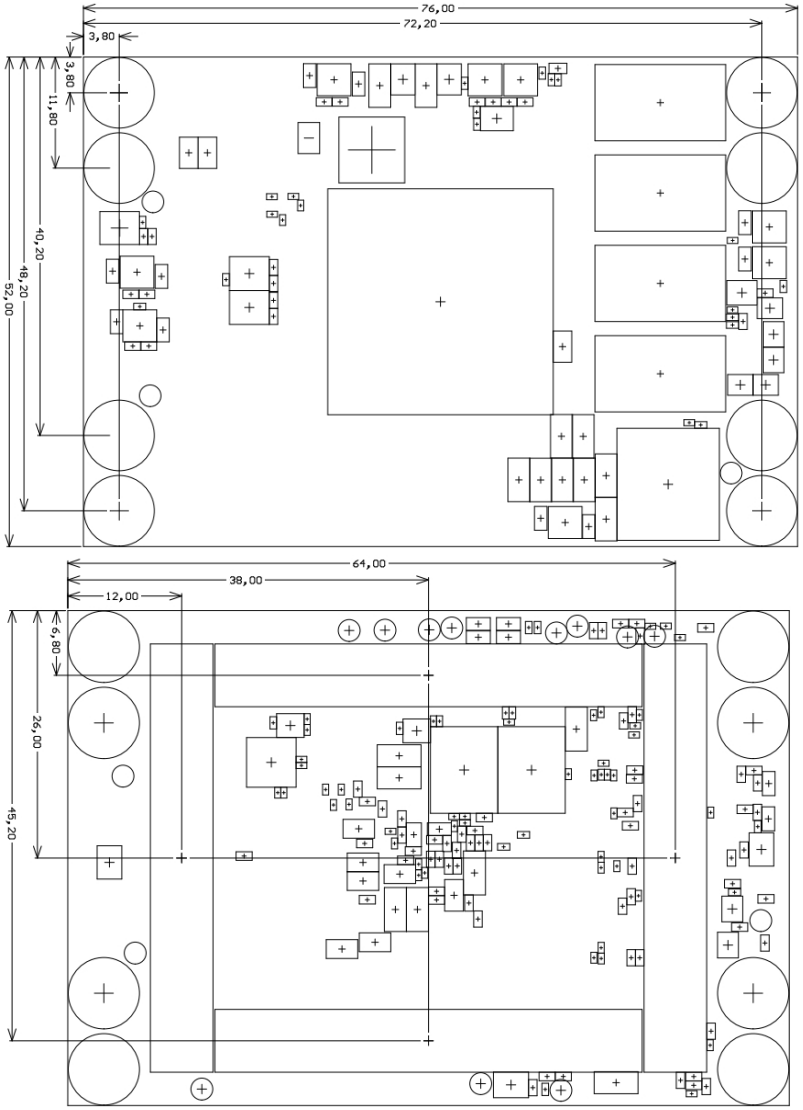
Extended grade: 0°C to +100°C.

The module operating temperature range depends also on customer design and cooling solution. Please contact us for options.

9.4 Physical Dimensions

- Module size: 52 mm × 76 mm. Please download the assembly diagram for exact numbers
- Mating height with standard connectors: 4mm
- PCB thickness: 1.6mm
- Highest part on PCB: approx. 3mm. Please download the step model for exact numbers

All dimensions are given in millimeters.

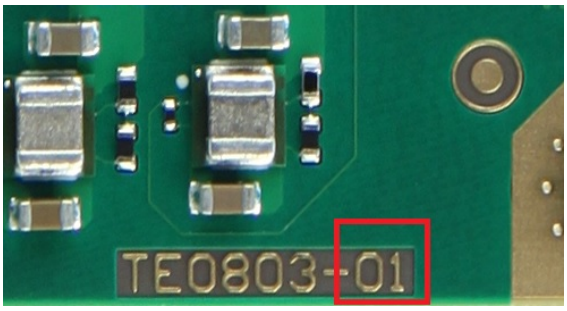


10 Revision History

10.1 Hardware Revision History

Date	Revision	Notes	Link to PCN	Documentation Link
2016-12-23	01	First production release	-	TE0803-01

Hardware revision number is written on the PCB board together with the module model number separated by the dash.



10.2 Document Change History

Date	Revision	Contributors	Description
2018-08-06	v.28	John Hartfiel	• typo correction
2017-11-13	v.23	Ali Naseri	• updated B2B connector max. current rating per pin
2017-11-13	v.19	John Hartfiel	• rework B2B section
2017-10-19	v.18	John Hartfiel	• Removed ES1 Note
2017-08-15	v.17	Vitali Tsiukala	• Changed Signals Count in the table B2B-connectors
2017-08-07	v.14	Jan Kumann	• New smaller images. • New QSPI Flash MIO mapping table. • Temperature information changes. • Few corrections.
2017-05-17	V.4	Ali Naseri	Current TRM release.
2017-05-10	v.1	Ali Naseri	Initial document.

11 Disclaimer

11.1 Data privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

11.2 Document Warranty

The material contained in this document is provided “as is” and is subject to being changed at any time without notice. Trenz Electronic does not warrant the accuracy and completeness of the materials in this document. Further, to the maximum extent permitted by applicable law, Trenz Electronic disclaims all warranties, either express or implied, with regard to this document and any information contained herein, including but not limited to the implied warranties of merchantability, fitness for a particular purpose or non infringement of intellectual property. Trenz Electronic shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein.

11.3 Limitation of Liability

In no event will Trenz Electronic, its suppliers, or other third parties mentioned in this document be liable for any damages whatsoever (including, without limitation, those resulting from lost profits, lost data or business interruption) arising out of the use, inability to use, or the results of use of this document, any documents linked to this document, or the materials or information contained at any or all such documents. If your use of the materials or information from this document results in the need for servicing, repair or correction of equipment or data, you assume all costs thereof.

11.4 Copyright Notice

No part of this manual may be reproduced in any form or by any means (including electronic storage and retrieval or translation into a foreign language) without prior agreement and written consent from Trenz Electronic.

11.5 Technology Licenses

The hardware / firmware / software described in this document are furnished under a license and may be used / modified / copied only in accordance with the terms of such license.

11.6 Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

11.7 REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release