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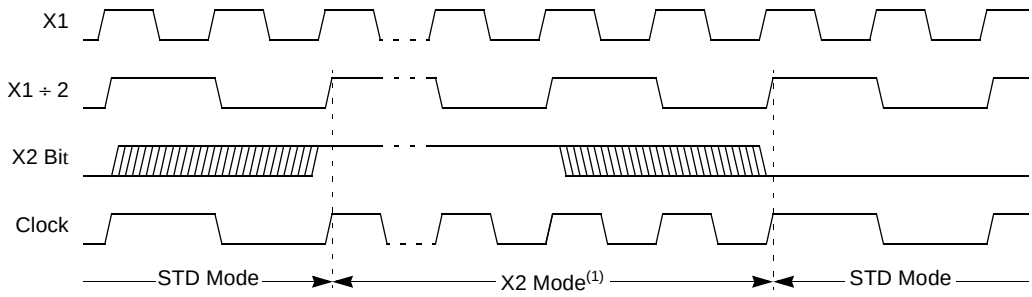
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, IDE/ATAPI, Memory Card, SPI, UART/USART, USB
Peripherals	Audio, I²S, MP3, PCM, POR, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.3V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-CTBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c51snd2c-7ftul

Figure 5. Mode Switching Waveforms



Note: 1. In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (timers, etc.) will have their time reference divided by 2. For example, a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms.

PLL

PLL Description

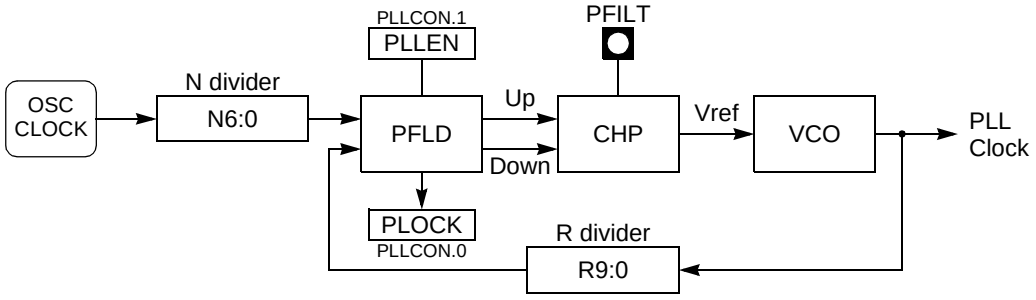
The AT8xC51SND2C PLL is used to generate internal high frequency clock (the PLL Clock) synchronized with an external low-frequency (the Oscillator Clock). The PLL clock provides the MP3 decoder, the audio interface, and the USB interface clocks. Figure 6 shows the internal structure of the PLL.

The PFLD block is the Phase Frequency Comparator and Lock Detector. This block makes the comparison between the reference clock coming from the N divider and the reverse clock coming from the R divider and generates some pulses on the Up or Down signal depending on the edge position of the reverse clock. The PLLEN bit in PLLCON register is used to enable the clock generation. When the PLL is locked, the bit PLOCK in PLLCON register (see Table 18) is set.

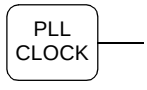
The CHP block is the Charge Pump that generates the voltage reference for the VCO by injecting or extracting charges from the external filter connected on PFILT pin (see Figure 7). Value of the filter components are detailed in the Section “DC Characteristics”.

The VCO block is the Voltage Controlled Oscillator controlled by the voltage V_{ref} produced by the charge pump. It generates a square wave signal: the PLL clock.

Figure 6. PLL Block Diagram and Symbol



$$PLLclk = \frac{OSCclk \times (R + 1)}{N + 1}$$



PLL Clock Symbol

Table 49. SFR Addresses and Reset Values

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h	UEPINT 0000 0000	DAT16H XXXX XXXX		NVERS XXXX XXXX(2)					FFh
F0h	B(1) 0000 0000								F7h
E8h		PLLCON 0000 1000	USBCLK 0000 0000	MP3CLK 0000 0000	AUDCLK 0000 0000	MMCLK 0000 0000	PLLNDIV 0000 0000	PLLRDIV 0000 0000	EFh
E0h	ACC(1) 0000 0000		UBYCTLX 0000 0000		MMCON0 0000 0000	MMCON1 0000 0000	MMCON2 0000 0000	MMINT 0000 0011	E7h
D8h	P5(1) XXXX 1111				MMDAT 1111 1111	MMCMD 1111 1111	MMSTA 0000 0000	MMMSK 1111 1111	DFh
D0h	PSW(1) 0000 0000	FCON(3) 1111 0000(4)			UEPCONX 1000 0000	UEPRST 0000 0000			D7h
C8h	MP3STA(1) 0000 0001						UEPSTAX 0000 0000	UEPDATX XXXX XXXX	CFh
C0h	P4(1) 1111 1111		UEPIEN 0000 0000	SPCON 0001 0100	SPSTA 0000 0000	SPDAT XXXX XXXX	USBADDR 0000 0000	UEPNUM 0000 0000	C7h
B8h	IPL0(1) X000 0000	SADEN 0000 0000	UFNUML 0000 0000	UFNUMH 0000 0000	USBCON 0000 0000	USBINT 0000 0000	USBIEN 0001 0000		BFh
B0h	P3(1) 1111 1111	IEN1 0000 0000	IPL1 0000 0000	IPH1 0000 0000	MP3BAS 0000 0000	MP3MED 0000 0000	MP3TRE 0000 0000	IPH0 X000 0000	B7h
A8h	IEN0(1) 0000 0000	SADDR 0000 0000	MP3CON 0011 1111		MP3DAT 0000 0000	MP3ANC 0000 0000		MP3STA1 0100 0001	AFh
A0h	P2(1) 1111 1111		AUXR1 XXXX 00X0	KBCON 0000 1111	KBSTA 0000 0000		WDTRST XXX XXXX	WDTPRG XXXX X000	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX	AUDCON0 0000 1000	AUDCON1 1011 0010	AUDSTA 1100 0000	AUDDAT 1111 1111	MP3VOL 0000 0000	MP3VOR 0000 0000	9Fh
90h	AUXCON(1) 1111 1111	BRL 0000 0000	BDRCON XXX0 0000	SSCON 0000 0000	SSSTA 1111 1000	SSDAT 1111 1111	SSADR 1111 1110		97h
88h	TCON(1) 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR X000 1101	CKCON 0000 000X(5)	8Fh
80h	P0(1) 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00XX 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Reserved

Notes:
1. SFR registers with least significant nibble address equal to 0 or 8 are bit-addressable.
2. NVERS reset value depends on the silicon version: 1000 0100 for AT89C51SND2C product and 0000 0001 for AT83SND2C product.
3. FCON register is only available in AT89C51SND2C product.
4. FCON reset value is 00h in case of reset with hardware condition.
5. CKCON reset value depends on the X2B bit (programmed or unprogrammed) in the Hardware Byte.

Figure 19. Interrupt Control System

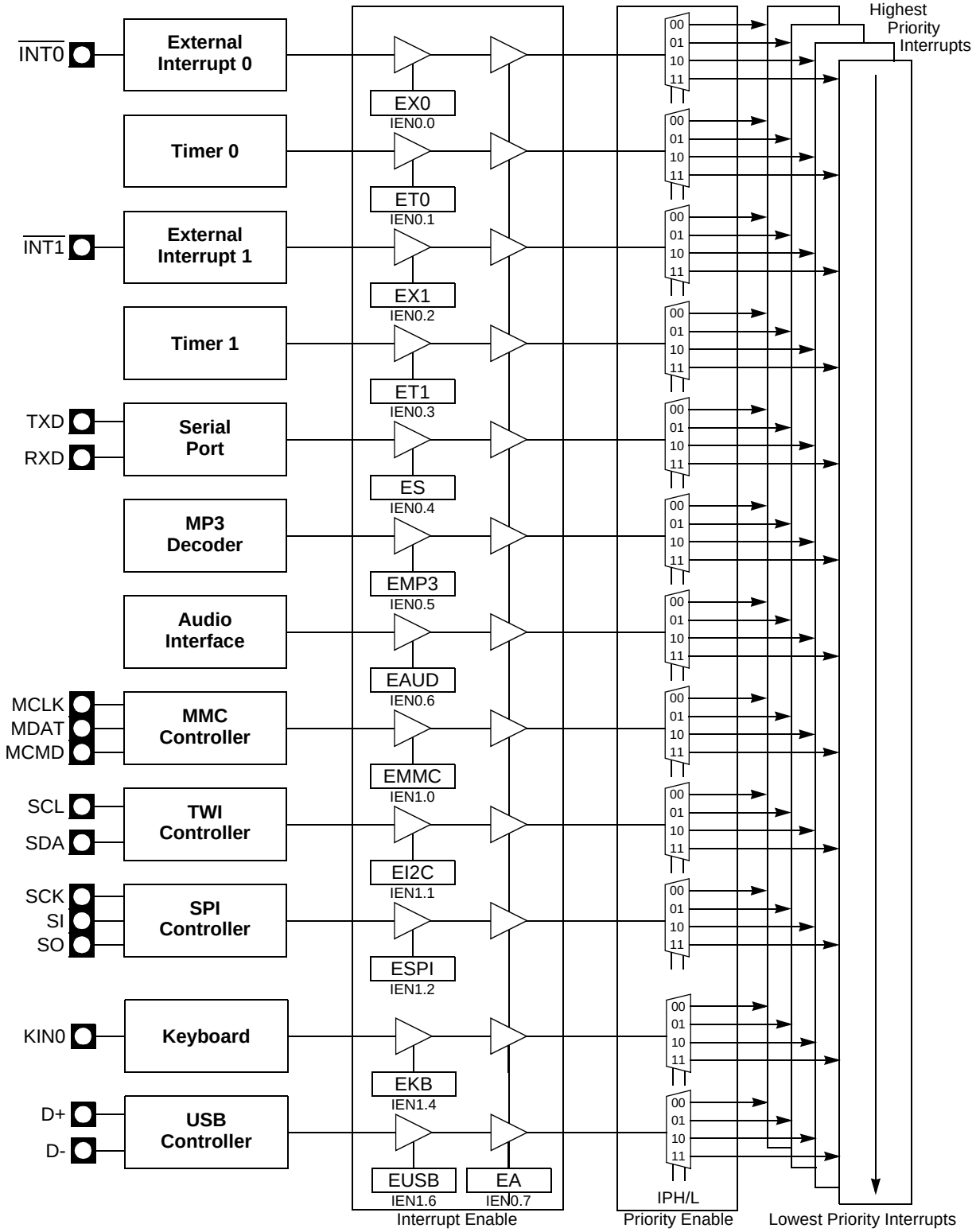


Table 55. IPH0 Register

IPH0 (S:B7h) – Interrupt Priority High Register 0

7	6	5	4	3	2	1	0
-	IPHAUD	IPHMP3	IPHS	IPHT1	IPHX1	IPHT0	IPHX0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	IPHAUD	**Audio Interface Interrupt Priority Level MSB** Refer to Table 51 for priority level description.
5	IPHMP3	**MP3 Decoder Interrupt Priority Level MSB** Refer to Table 51 for priority level description.
4	IPHS	**Serial Port Interrupt Priority Level MSB** Refer to Table 51 for priority level description.
3	IPHT1	**Timer 1 Interrupt Priority Level MSB** Refer to Table 51 for priority level description.
2	IPHX1	**External Interrupt 1 Priority Level MSB** Refer to Table 51 for priority level description.
1	IPHT0	**Timer 0 Interrupt Priority Level MSB** Refer to Table 51 for priority level description.
0	IPHX0	**External Interrupt 0 Priority Level MSB** Refer to Table 51 for priority level description.

Reset Value = X000 0000b

Table 58. IPL1 Register

IPL1 (S:B2h) – Interrupt Priority Low Register 1

7	6	5	4	3	2	1	0
-	IPLUSB	-	IPLKB	-	IPLSPI	IPLI2C	IPLMMC

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is always 0. Do not set this bit.
6	IPLUSB	**USB Interrupt Priority Level LSB** Refer to Table 51 for priority level description.
5	-	**Reserved** The value read from this bit is always 0. Do not set this bit.
4	IPLKB	**Keyboard Interrupt Priority Level LSB** Refer to Table 51 for priority level description.
3	-	**Reserved** The value read from this bit is always 0. Do not set this bit.
2	IPLSPI	**SPI Interrupt Priority Level LSB** Refer to Table 51 for priority level description.
1	IPLI2C	**Two Wire Controller Interrupt Priority Level LSB** Refer to Table 51 for priority level description.
0	IPLMMC	**MMC Interrupt Priority Level LSB** Refer to Table 51 for priority level description.

Reset Value = 0000 0000b

3. Figure 32 gives the autoreload period calculation formulas for both TF0 and TF1 flags.

Figure 33. Timer/Counter 0 in Mode 3: 2 8-bit Counters

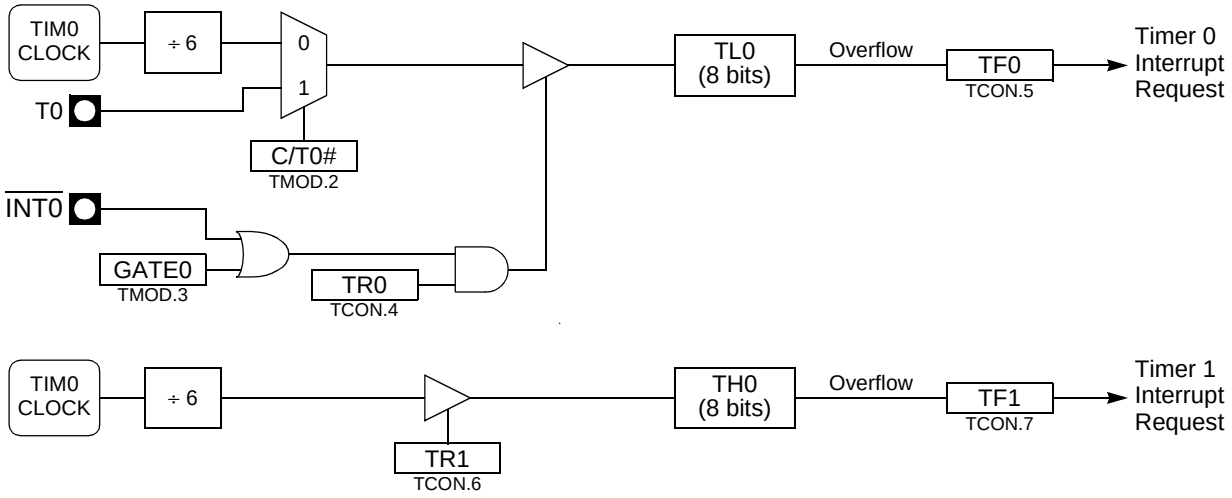


Figure 34. Mode 3 Overflow Period Formula

$$TF0_{PER} = \frac{6 \cdot (256 - TL0)}{F_{TIM0}} \qquad TF1_{PER} = \frac{6 \cdot (256 - TH0)}{F_{TIM0}}$$

Timer 1

Timer 1 is identical to Timer 0 except for Mode 3 which is a hold-count mode. The following comments help to understand the differences:

- Timer 1 functions as either a Timer or event Counter in three modes of operation. Figure 27 through Figure 31 show the logical configuration for modes 0, 1, and 2. Timer 1's mode 3 is a hold-count mode.
- Timer 1 is controlled by the four high-order bits of TMOD register (see Figure 63) and bits 2, 3, 6 and 7 of TCON register (see Figure 62). TMOD register selects the method of Timer gating (GATE1), Timer or Counter operation (C/T1#) and mode of operation (M11 and M01). TCON register provides Timer 1 control functions: overflow flag (TF1), run control bit (TR1), interrupt flag (IE1) and interrupt type control bit (IT1).
- Timer 1 can serve as the Baud Rate Generator for the Serial Port. Mode 2 is best suited for this purpose.
- For normal Timer operation (GATE1 = 0), setting TR1 allows TL1 to be incremented by the selected input. Setting GATE1 and TR1 allows external pin $\overline{INT1}$ to control Timer operation.
- Timer 1 overflow (count rolls over from all 1s to all 0s) sets the TF1 flag generating an interrupt request.
- When Timer 0 is in mode 3, it uses Timer 1's overflow flag (TF1) and run control bit (TR1). For this situation, use Timer 1 only for applications that do not require an interrupt (such as a Baud Rate Generator for the Serial Port) and switch Timer 1 in and out of mode 3 to turn it off and on.
- It is important to stop the Timer/Counter before changing modes.

Table 102. Dac Control Register Register - DAC_CTRL (00h)

7	6	5	4	3	2	1	0
ONPADRV	ONAUXIN	ONDACR	ONDACL	ONLNOR	ONLNOL	ONLNIR	ONLNIL

Bit Number	Bit Mnemonic	Description
7	ONPADRV	Differential mono PA driver Clear to power down. Set to power up.
6	ONAUXIN	Differential mono auxiliary input amplifier Clear to power down. Set to power up.
5	ONDACR	Right channel DAC Clear to power down. Set to power up.
4	ONDACL	Left channel DAC Clear to power down. Set to power up.
3	ONLNOR	Right channel line out driver Clear to power down. Set to power up.
2	ONLNOL	Left channel line out driver Clear to power down. Set to power up.
1	ONLNIR	Right channel line in amplifier Clear to power down. Set to power up.
0	ONLNIL	Left channel line in amplifier Clear to power down. Set to power up.

Reset Value = 00000000b

Table 103. DAC Left Line In Gain Register - DAC_LLIG (01h)

7	6	5	4	3	2	1	0
-	-	-	LLIG4	LLIG3	LLIG2	LLIG1	LLIG0

Bit Number	Bit Mnemonic	Description
7:5	-	Not used
4:0	LLIG 4:0	Left channel line in analog gain selector

Reset Value = 00000101b

Register

Table 119. PA Control Register - PA_CTRL (11h)l

7	6	5	4	3	2	1	0
-	APAON	APAPRECH	APALP	APAGAIN3	APAGAIN2	APAGAIN1	APAGAIN0

Bit Number	Bit Mnemonic	Description
7	-	Not used
6	APAON	Audio power amplifier on bit
5	APAPRECH	Audio power amplifier precharge bit
4	APALP	Audio power amplifier low power bit
3:0	APAGAIN3:0	Audio power amplifier gain

Reset Value = 00000000b

Serial Interface Engine (SIE)

The SIE performs the following functions:

- NRZI data encoding and decoding.
- Bit stuffing and unstuffing.
- CRC generation and checking.
- ACKs and NACKs automatic generation.
- TOKEN type identifying.
- Address checking.
- Clock recovery (using DPLL).

Figure 65. SIE Block Diagram

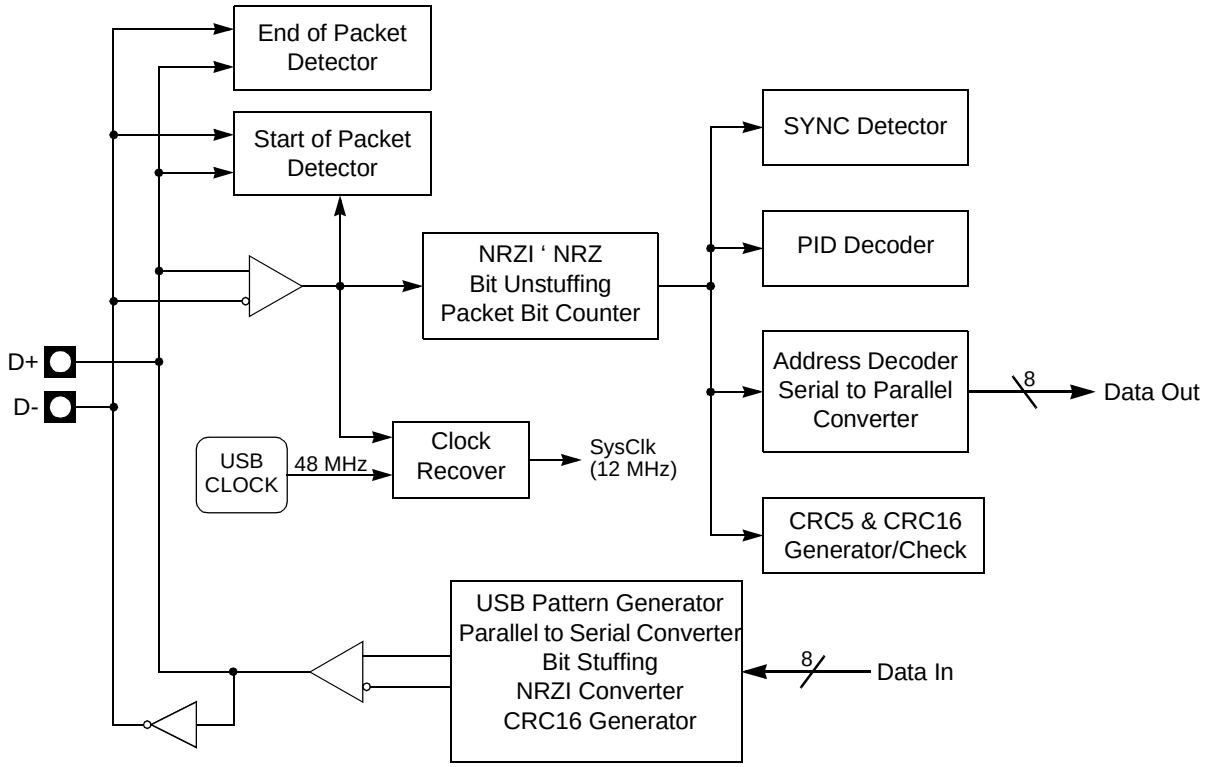


Table 126. UEPCONX Register

UEPCONX (S:D4h) – USB Endpoint X Control Register (X = EPNUM set in UEPNUM)

7	6	5	4	3	2	1	0
EPEN	**NAKIEN**	**NAKOUT**	**NAKIN**	**DTGL**	**EPDIR**	**EPTYPE1**	**EPTYPE0**

Bit Number	Bit Mnemonic	Description
7	EPEN	**Endpoint Enable Bit** Set to enable the endpoint according to the device configuration. Endpoint 0 should always be enabled after a hardware or USB bus reset and participate in the device configuration. Clear to disable the endpoint according to the device configuration.
6	NAKIEN	**NAK Interrupt enable** Set this bit to enable NAK IN or NAK OUT interrupt. Clear this bit to disable NAK IN or NAK OUT Interrupt.
5	NAKOUT	**NAK OUT received** This bit is set by hardware when an NAK handshake has been sent in response of a OUT request from the Host. This triggers a USB interrupt when NAKIEN is set. This bit should be cleared by software.
4	NAKIN	**NAK IN received** This bit is set by hardware when an NAK handshake has been sent in response of a IN request from the Host. This triggers a USB interrupt when NAKIEN is set. This bit should be cleared by software.
3	DTGL	**Data Toggle Status Bit (Read-only)** Set by hardware when a DATA1 packet is received. Cleared by hardware when a DATA0 packet is received.
2	EPDIR	**Endpoint Direction Bit** Set to configure IN direction for Bulk, Interrupt and Isochronous endpoints. Clear to configure OUT direction for Bulk, Interrupt and Isochronous endpoints. This bit has no effect for Control endpoints.
1-0	EPTYPE1:0	**Endpoint Type Bits** Set this field according to the endpoint configuration (Endpoint 0 should always be configured as Control): 00 Control endpoint 01 Isochronous endpoint 10 Bulk endpoint 11 Interrupt endpoint

Reset Value = 1000 0000b

Table 127. UEPSTAX Register

UEPSTAX (S:CEh) – USB Endpoint X Status and Control Register (X = EPNUM set in UEPNUM)

7	6	5	4	3	2	1	0
DIR	**RXOUTB1**	**STALLRQ**	**TXRDY**	**STLCRC**	**RXSETUP**	**RXOUTB0**	**TXCMP**

Bit Number	Bit Mnemonic	Description
7	DIR	**Control Endpoint Direction Bit** This bit is relevant only if the endpoint is configured in Control type. Set for the data stage. Clear otherwise. Note: This bit should be configured on RXSETUP interrupt before any other bit is changed. This also determines the status phase (IN for a control write and OUT for a control read). This bit should be cleared for status stage of a Control Out transaction.
6	RXOUTB1	**Received OUT Data Bank 1 for Endpoints 1 and 2 (Ping-pong mode)** This bit is set by hardware after a new packet has been stored in the endpoint FIFO data bank 1 (only in Ping-pong mode). Then, the endpoint interrupt is triggered if enabled and all the following OUT packets to the endpoint bank 1 are rejected (NAK'ed) until this bit has been cleared, excepted for Isochronous Endpoints. This bit should be cleared by the device firmware after reading the OUT data from the endpoint FIFO.

Table 141. R3 Response Format (OCR Register)

Bit Position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'0'	'111111'	-	'1111111'	'1'
Description	Start bit	Transmission bit	Reserved	OCR register	Reserved	End bit

Table 142. R4 Response Format (Fast I/O)

Bit Position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'0'	'100111'	-	-	'1'
Description	Start bit	Transmission bit	Command Index	Argument	CRC7	End bit

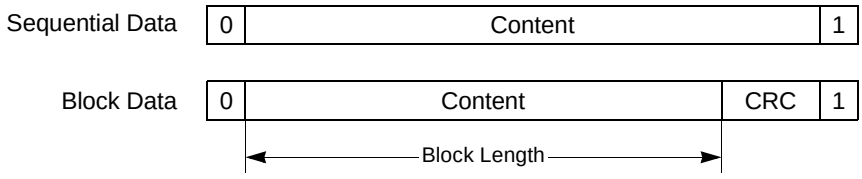
Table 143. R5 Response Format

Bit Position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'0'	'101000'	-	-	'1'
Description	Start bit	Transmission bit	Command Index	Argument	CRC7	End bit

Data Packet Format

There are 2 types of data packets: stream and block. As shown in Figure 89, stream data packets have an indeterminate length while block packets have a fixed length depending on the block length. Each data packet is preceded by a Start bit: a low level on MCMD line and succeeded by an End bit: a high level on MCMD line. Due to the fact that there is no predefined end in stream packets, CRC protection is not included in this case. The CRC protection algorithm for block data is a 16-bit CCITT polynomial.

Figure 89. Data Token Format



Clock Control

The MMC bus clock signal can be used by the host to turn the cards into energy saving mode or to control the data flow (to avoid under-run or over-run conditions) on the bus. The host is allowed to lower the clock frequency or shut it down.
There are a few restrictions the host must follow:

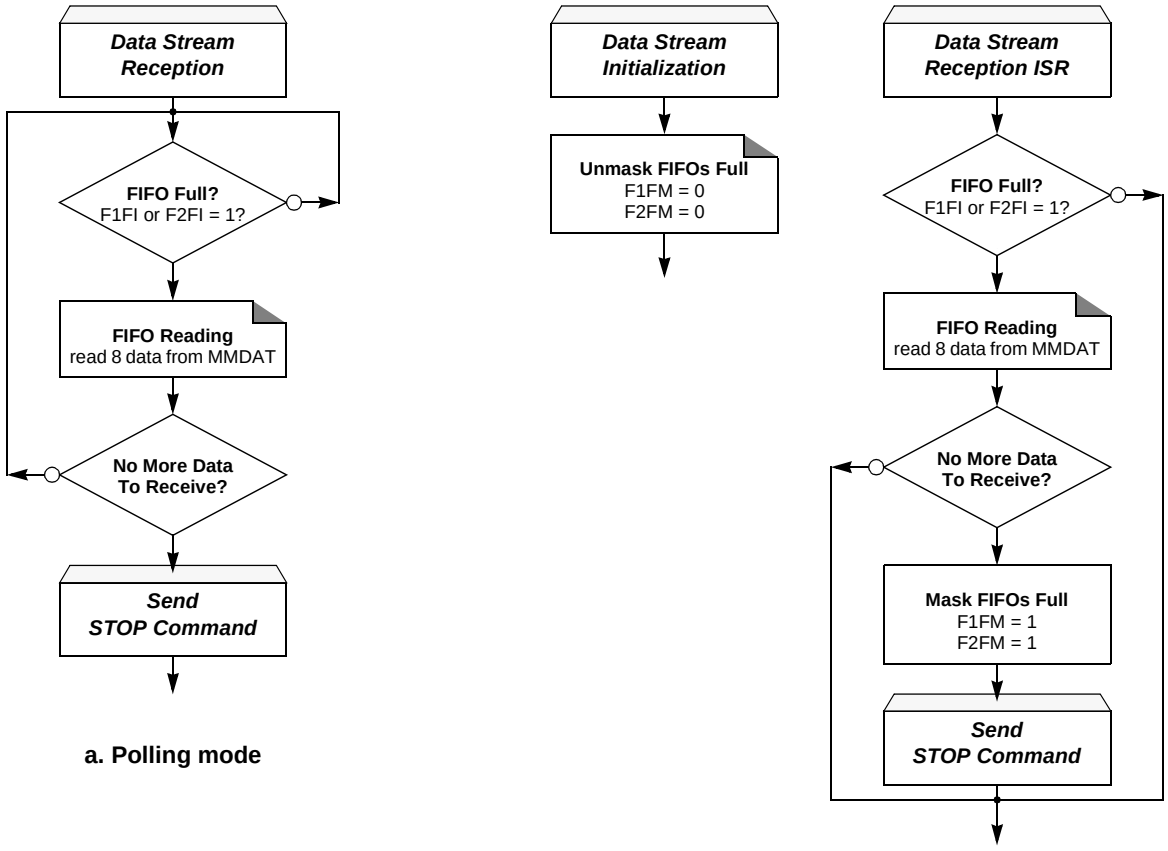
- The bus frequency can be changed at any time (under the restrictions of maximum data transfer frequency, defined by the cards, and the identification frequency defined by the specification document).
- It is an obvious requirement that the clock must be running for the card to output data or response tokens. After the last MultiMedia Card bus transaction, the host is

This time-out may be disarmed after receiving 8 data (F1FI flag set) or after receiving end of frame (EOFI flag set) in case of block length less than 8 data (1, 2 or 4).

Data Reading

Data is read from the FIFO by reading to MMDAT register. Each time one FIFO becomes full (F1FI or F2FI set), user is requested to flush this FIFO by reading 8 data.

Figure 99. Data Stream Reception Flows



a. Polling mode

b. Interrupt mode

Table 152. MMDAT Register

MMDAT (S:DCh) – MMC Data Register

7	6	5	4	3	2	1	0
MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0

Bit Number	Bit Mnemonic	Description
7 - 0	MD7:0	**MMC Data Byte** Input (write) or output (read) register of the data FIFO.

Reset Value = 1111 1111b

Table 153. MMCLK Register

MMCLK (S:EDh) – MMC Clock Divider Register

7	6	5	4	3	2	1	0
MMCD7	MMCD6	MMCD5	MMCD4	MMCD3	MMCD2	MMCD1	MMCD0

Bit Number	Bit Mnemonic	Description
7 - 0	MMCD7:0	**MMC Clock Divider** 8-bit divider for MMC clock generation.

Reset Value = 0000 0000b

Slave Mode with Interrupt Policy

Figure 111 shows the initialization phase and the transfer phase flows using the interrupt.

The transfer format depends on the master controller.

Reading SPSTA at the beginning of the ISR is mandatory for clearing the SPIF flag. Clear is effective when reading SPDAT.

Figure 113. Slave SPI Interrupt Policy Flows

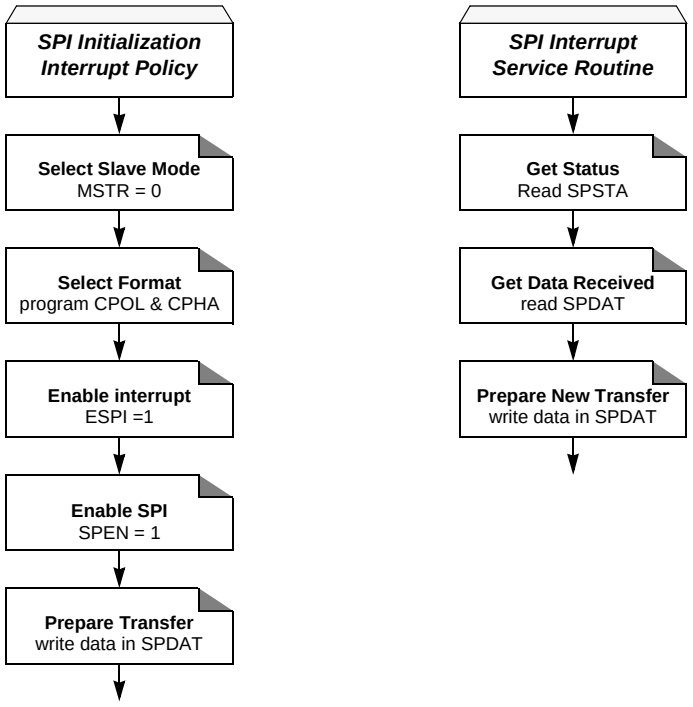
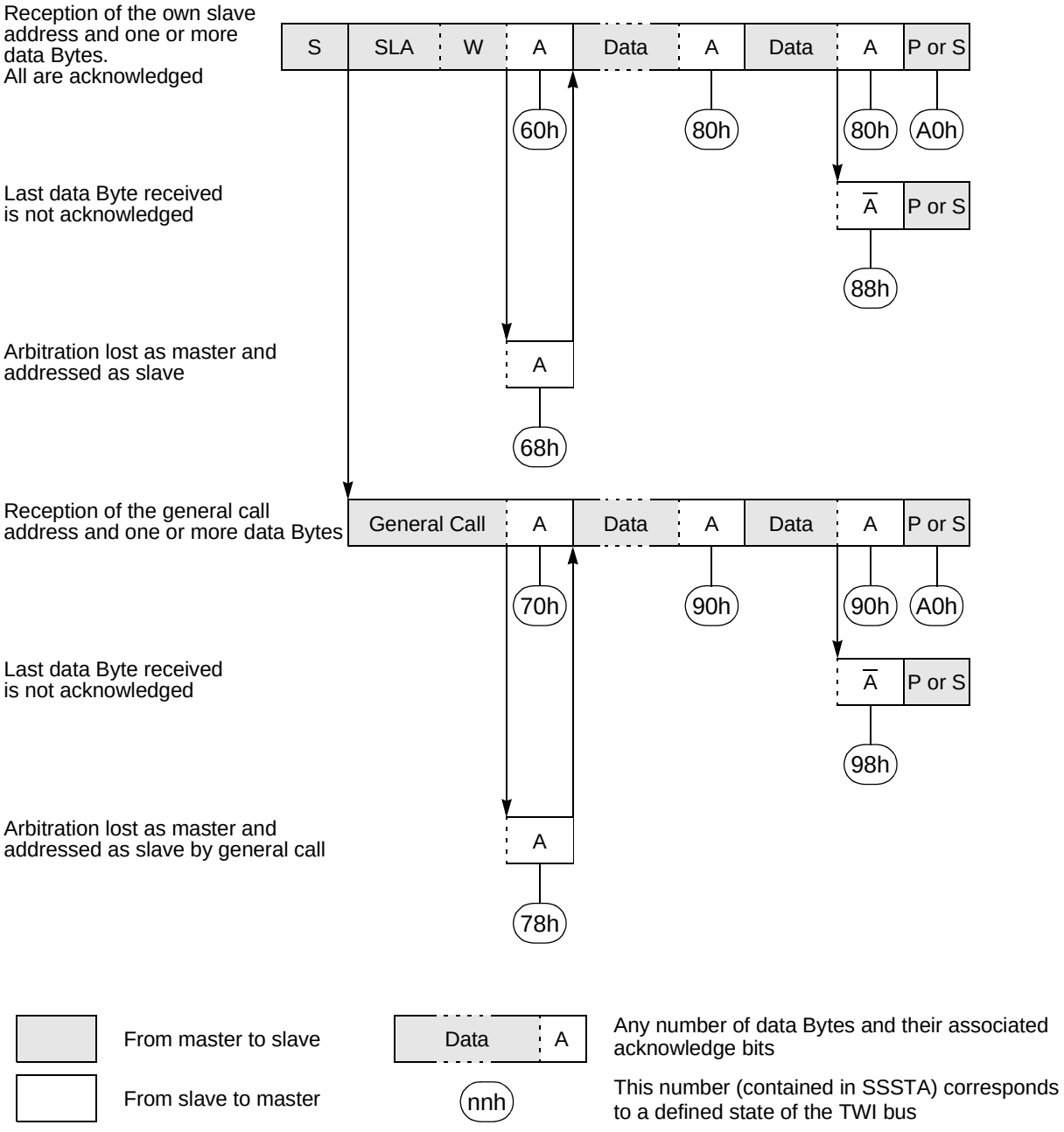


Figure 135. Format and States in the Slave Receiver Mode



Registers

Table 173. AUXCON Register
AUXCON (S:90h) – Auxiliary Control Register

7	6	5	4	3	2	1	0
SDA	**SCL**	**-**	**AUDCDOUT**	**AUDCDIN**	**AUDCCLK**	**AUDCCS**	**KIN0**

Bit Number	Bit Mnemonic	Description
7	SDA	**TWI Serial Data** SDA is the bidirectional Two Wire data line.
6	SCL	**TWI Serial Clock** When TWI controller is in master mode, SCL outputs the serial clock to the slave peripherals. When TWI controller is in slave mode, SCL receives clock from the master controller.
5:1		**Audio DAC Control** Refer to Audio DAC interface section
0	KIN0	**Keyboard Input Line**

Reset Value = 1111 1111b

Table 174. SSCON Register
SSCON (S:93h) – Synchronous Serial Control Register

7	6	5	4	3	2	1	0
SSCR2	SSPE	SSSTA	SSSTO	SSI	SSAA	SSCR1	SSCR0

Timings

Test conditions: capacitive load on all pins= 50 pF.

Table 194. External IDE 16-bit Bus Cycle - Data Read AC Timings

V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}$-15		T_{CLCL}-15		ns
T_{AVLL}	Address Valid to ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLAX}	Address hold after ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLRL}	ALE Low to $\overline{RD}$ Low	$3 \cdot T_{CLCL}$-30		$1.5 \cdot T_{CLCL}$-30		ns
T_{RLRH}	$\overline{RD}$ Pulse Width	$6 \cdot T_{CLCL}$-25		$3 \cdot T_{CLCL}$-25		ns
T_{RHLH}	$\overline{RD}$ high to ALE High	T_{CLCL}-20	T_{CLCL}+20	$0.5 \cdot T_{CLCL}$-20	$0.5 \cdot T_{CLCL}$+20	ns
T_{AVDV}	Address Valid to Valid Data In		$9 \cdot T_{CLCL}$-65		$4.5 \cdot T_{CLCL}$-65	ns
T_{AVRL}	Address Valid to $\overline{RD}$ Low	$4 \cdot T_{CLCL}$-30		$2 \cdot T_{CLCL}$-30		ns
T_{RLDV}	$\overline{RD}$ Low to Valid Data		$5 \cdot T_{CLCL}$-30		$2.5 \cdot T_{CLCL}$-30	ns
T_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
T_{RHDX}	Data Hold After $\overline{RD}$ High	0		0		ns
T_{RHDZ}	Instruction Float After $\overline{RD}$ High		$2 \cdot T_{CLCL}$-25		T_{CLCL}-25	ns

Table 195. External IDE 16-bit Bus Cycle - Data Write AC Timings

V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}$-15		T_{CLCL}-15		ns
T_{AVLL}	Address Valid to ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLAX}	Address hold after ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLWL}	ALE Low to $\overline{WR}$ Low	$3 \cdot T_{CLCL}$-30		$1.5 \cdot T_{CLCL}$-30		ns
T_{WLWH}	$\overline{WR}$ Pulse Width	$6 \cdot T_{CLCL}$-25		$3 \cdot T_{CLCL}$-25		ns
T_{WHLH}	$\overline{WR}$ High to ALE High	T_{CLCL}-20	T_{CLCL}+20	$0.5 \cdot T_{CLCL}$-20	$0.5 \cdot T_{CLCL}$+20	ns
T_{AVWL}	Address Valid to $\overline{WR}$ Low	$4 \cdot T_{CLCL}$-30		$2 \cdot T_{CLCL}$-30		ns
T_{QVWH}	Data Valid to $\overline{WR}$ High	$7 \cdot T_{CLCL}$-20		$3.5 \cdot T_{CLCL}$-20		ns
T_{WHQX}	Data Hold after $\overline{WR}$ High	T_{CLCL}-15		$0.5 \cdot T_{CLCL}$-15		ns

Flash Memory

Definition of symbols

Table 203. Flash Memory Timing Symbol Definitions

Signals	
S	$\overline{ISP}$
R	RST
B	FBUSY flag

Conditions	
L	Low
V	Valid
X	No Longer Valid

Timings

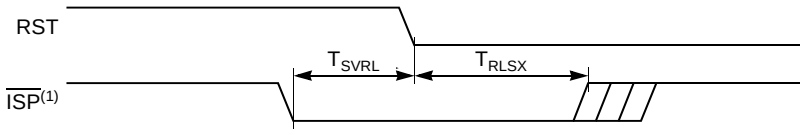
Table 204. Flash Memory AC Timing

V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
T_{SVRL}	Input $\overline{ISP}$ Valid to RST Edge	50			ns
T_{RLSX}	Input $\overline{ISP}$ Hold after RST Edge	50			ns
T_{BHBL}	FLASH Internal Busy (Programming) Time		10		ms
N_{FCY}	Number of Flash Write Cycles	100K			Cycle
T_{FDR}	Flash Data Retention Time	10			Years

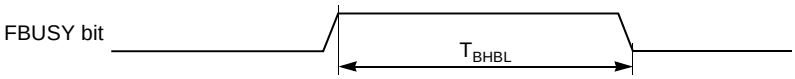
Waveforms

Figure 165. FLASH Memory - ISP Waveforms



Note: 1. $\overline{ISP}$ must be driven through a pull-down resistor (see Section “In System Programming”, page 212).

Figure 166. FLASH Memory - Internal Busy Waveforms



External Clock Drive and Logic Level References

Definition of symbols

Table 205. External Clock Timing Symbol Definitions

Signals	
C	Clock

Conditions	
H	High
L	Low
X	No Longer Valid

Timings

Table 206. External Clock AC Timings

V_{DD} = 2.7 to 3.3 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Max	Unit
T_{CLCL}	Clock Period	50		ns
T_{CHCX}	High Time	10		ns
T_{CLCX}	Low Time	10		ns
T_{CLCH}	Rise Time	3		ns
T_{CHCL}	Fall Time	3		ns
T_{CR}	Cyclic Ratio in X2 mode	40	60	%

Waveforms

Figure 167. External Clock Waveform

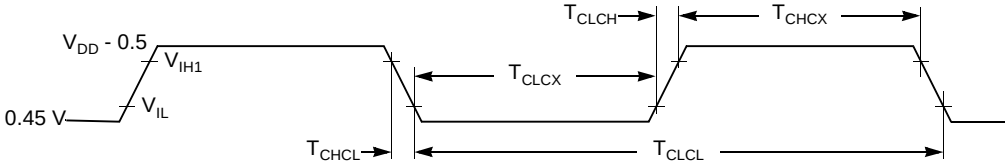
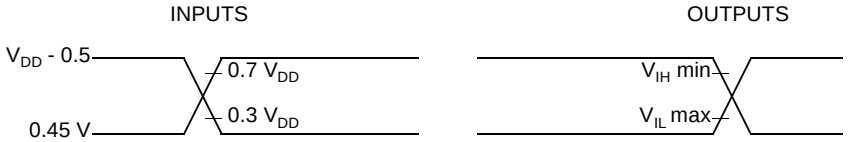


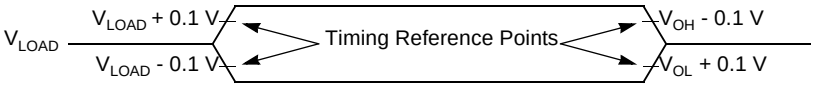
Figure 168. AC Testing Input/Output Waveforms



Note: 1. During AC testing, all inputs are driven at V_{DD} -0.5 V for a logic 1 and 0.45 V for a logic 0.

2. Timing measurements are made on all outputs at V_{IH} min for a logic 1 and V_{IL} max for a logic 0.

Figure 169. Float Waveforms



Note: For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with I_{OL}/I_{OH}= ±20 mA.