Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

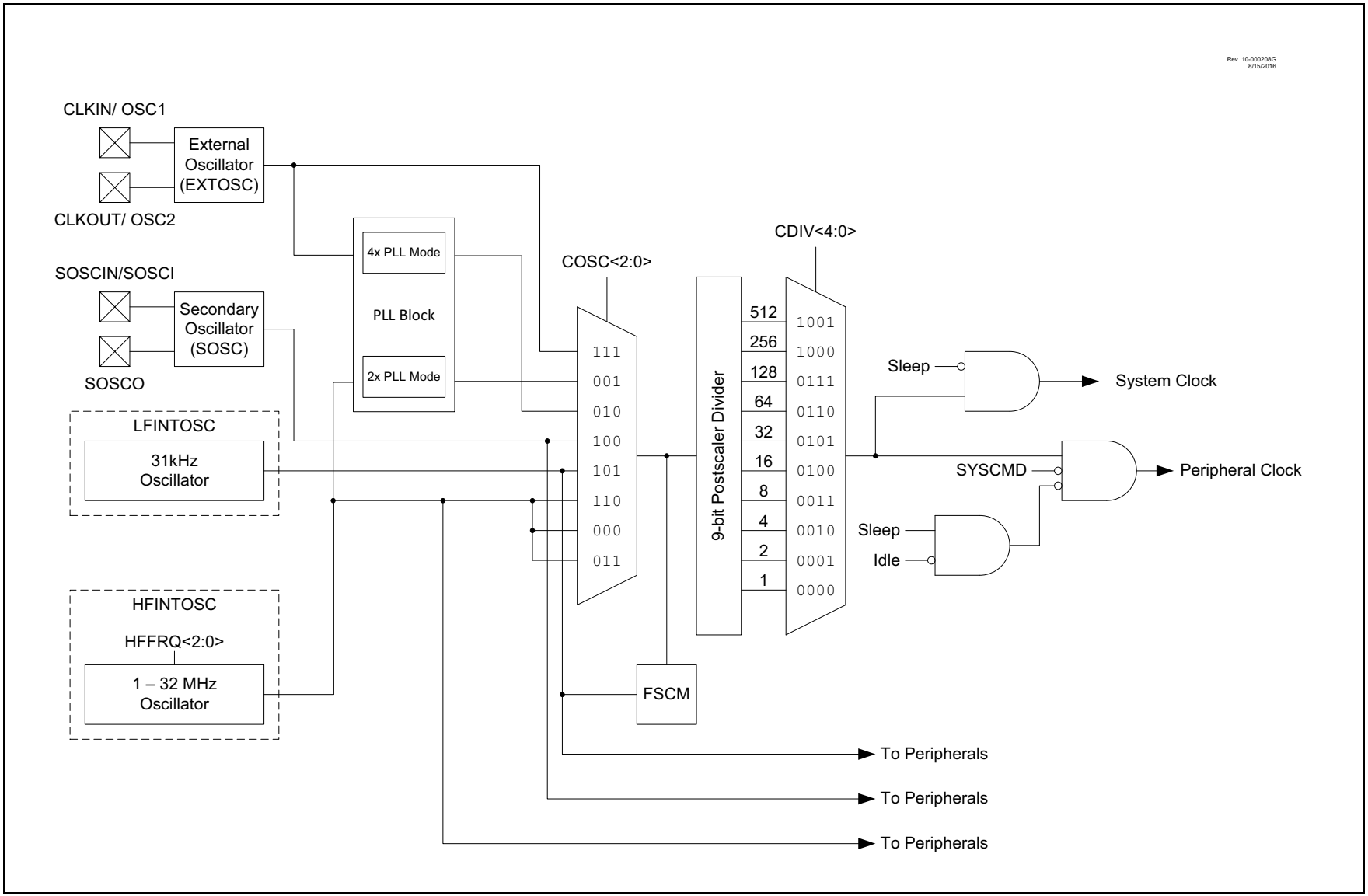
Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	224 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf15354t-i-ss

TABLE 4-10: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 62											
CPU CORE REGISTERS; see Table 4-3 for specifics											
1F0Ch	—	Unimplemented								---- ----	---- ----
1F0Dh	—	Unimplemented								---- ----	---- ----
1F0Eh	—	Unimplemented								---- ----	---- ----
1F0Fh	—	Unimplemented								---- ----	---- ----
1F10h	RA0PPS	—	—	—	RA0PPS<4:0>					--00 0000	--uu uuuu
1F11h	RA1PPS	—	—	—	RA1PPS<4:0>					--00 0000	--uu uuuu
1F12h	RA2PPS	—	—	—	RA2PPS<4:0>					--00 0000	--uu uuuu
1F13h	RA3PPS	—	—	—	RA3PPS<4:0>					--00 0000	--uu uuuu
1F14h	RA4PPS	—	—	—	RA4PPS<4:0>					--00 0000	--uu uuuu
1F15h	RA5PPS	—	—	—	RA5PPS<4:0>					--00 0000	--uu uuuu
1F16h	RA6PPS	—	—	—	RA6PPS<4:0>					--00 0000	--uu uuuu
1F17h	RA7PPS	—	—	—	RA7PPS<4:0>					--00 0000	--uu uuuu
1F18h	RB0PPS	—	—	—	RB0PPS<4:0>					--00 0000	--uu uuuu
1F19h	RB1PPS	—	—	—	RB1PPS<4:0>					--00 0000	--uu uuuu
1F1Ah	RB2PPS	—	—	—	RB2PPS<4:0>					--00 0000	--uu uuuu
1F1Bh	RB3PPS	—	—	—	RB3PPS<4:0>					--00 0000	--uu uuuu
1F1Ch	RB4PPS	—	—	—	RB4PPS<4:0>					--00 0000	--uu uuuu
1F1Dh	RB5PPS	—	—	—	RB5PPS<4:0>					--00 0000	--uu uuuu
1F1Eh	RB6PPS	—	—	—	RB6PPS<4:0>					--00 0000	--uu uuuu
1F1Fh	RB7PPS	—	—	—	RB7PPS<4:0>					--00 0000	--uu uuuu
1F20h	RC0PPS	—	—	—	RC0PPS<4:0>					--00 0000	--uu uuuu
1F21h	RC1PPS	—	—	—	RC1PPS<4:0>					--00 0000	--uu uuuu
1F22h	RC2PPS	—	—	—	RC2PPS<4:0>					--00 0000	--uu uuuu
1F23h	RC3PPS	—	—	—	RC3PPS<4:0>					--00 0000	--uu uuuu
1F24h	RC4PPS	—	—	—	RC4PPS<4:0>					--00 0000	--uu uuuu
1F25h	RC5PPS	—	—	—	RC5PPS<4:0>					--00 0000	--uu uuuu
1F26h	RC6PPS	—	—	—	RC6PPS<4:0>					--00 0000	--uu uuuu
1F27h	RC7PPS	—	—	—	RC7PPS<4:0>					--00 0000	--uu uuuu
1F28h — 1F37h	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

FIGURE 9-1: SIMPLIFIED PIC® MCU CLOCK SOURCE BLOCK DIAGRAM



13.3.3 NVMREG ERASE OF PFM

Before writing to PFM, the word(s) to be written must be erased or previously unwritten. PFM can only be erased one row at a time. No automatic erase occurs upon the initiation of the write to PFM.

To erase a PFM row:

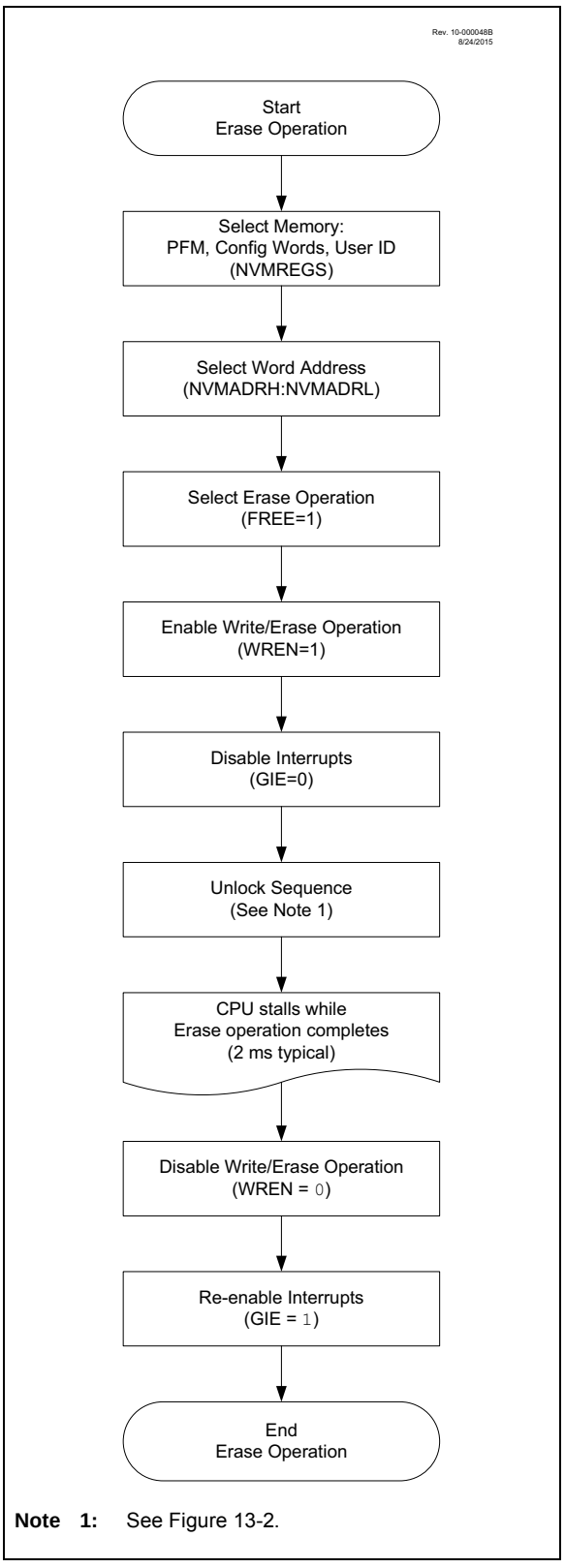
1. Clear the NVMREGS bit of the NVMCON1 register to erase PFM locations, or set the NMVREGS bit to erase User ID locations.
2. Write the desired address into the NVMADRH:NVMADRL register pair (Table 13-2).
3. Set the FREE and WREN bits of the NVMCON1 register.
4. Perform the unlock sequence as described in **Section 13.3.2 “NVM Unlock Sequence”**.

If the PFM address is write-protected, the WR bit will be cleared and the erase operation will not take place.

While erasing PFM, CPU operation is suspended, and resumes when the operation is complete. Upon completion, the NVMIF is set, and an interrupt will occur if the NVMIE bit is also set.

Write latch data is not affected by erase operations, and WREN will remain unchanged.

FIGURE 13-3: NVM ERASE FLOWCHART



Note 1: See Figure 13-2.

TABLE 15-1: PPS INPUT SIGNAL ROUTING OPTIONS

INPUT SIGNAL NAME	Input Register Name	Default Location at POR	Remappable to Pins of PORTx		
			PIC16(L)F15354/55		
			PORTA	PORTB	PORTC
INT	INTPPS	RB0	●	●	
T0CKI	T0CKIPPS	RA4	●	●	
T1CKI	T1CKIPSS	RC0	●		●
T1G	T1GPPS	RB5		●	●
T2IN	T2INPPS	RC3	●		●
CCP1	CCP1PPS	RC2		●	●
CCP2	CCP2PPS	RC1		●	●
CWG1IN	CWG1INPPS	RB0		●	●
CLCIN0	CLCIN0PPS	RA0	●		●
CLCIN1	CLCIN1PPS	RA1	●		●
CLCIN2	CLCIN2PPS	RB6		●	●
CLCIN3	CLCIN3PPS	RB7		●	●
ADACT	ADACTPPS	RB4		●	●
SCK1/SCL1	SSP1CLKPPS	RC3		●	●
SDI1/SDA1	SSP1DATPPS	RC4		●	●
SS1	SSP1SS1PPS	RA5	●		●
SCK2/SCL2	SSP2CLKPPS	RB1		●	●
SDI2/SDA2	SSP2DATPPS	RB2		●	●
SS2	SSP2SSPPS	RB0		●	●
RX1/DT1	RX1PPS	RC7		●	●
CK1	TX1PPS	RC6		●	●
RX2/DT2	RX2PPS	RB7		●	●
CK2	TX2PPS	RB6		●	●

REGISTER 15-2: RxyPPS: PIN Rxy OUTPUT SOURCE SELECTION REGISTER

U-0	U-0	U-0	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	RxyPPS<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **RxyPPS<5:0>:** Pin Rxy Output Source Selection bits
See Table 15-3.

Note 1: TRIS control is overridden by the peripheral as required.

REGISTER 15-3: PPSLOCK: PPS LOCK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0/0
—	—	—	—	—	—	—	PPSLOCKED
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-1 **Unimplemented:** Read as ‘0’

bit 0 **PPSLOCKED:** PPS Locked bit
1= PPS is locked. PPS selections can not be changed.
0= PPS is not locked. PPS selections can be changed.

19.2.1 CALIBRATION

Single-Point Calibration

Single-point calibration is performed by application software using Equation 19-1 and the assumed Mt. A reading of VTSENSE at a known temperature is taken, and the theoretical temperature is calculated by temporarily setting TOFFSET = 0. Then TOFFSET is computed as the difference of the actual and calculated temperatures. Finally, TOFFSET is stored in nonvolatile memory within the device, and is applied to future readings to gain a more accurate measurement.

The magnitude of error in a typical single-point calibration is approximately 3-4°C.

Note 1: The TOFFSET value may be determined by the user with a temperature test, or it can be based on the Microchip-supplied data from the DIA table. Please refer to **Section 6.0 "Device Information Area"** for more information.

2: Although the measurement range is -40°C to +125 °C, due to the variations in the value of Mv, the single-point calculated TSENSE value may indicate a temperature from -140°C to +225°C, before the calibration offset is applied.

Higher-Order Calibration

If the application requires more precise temperature measurement, additional calibrations steps will be necessary. For these applications, two-point or three-point calibration is recommended.

19.2.2 TEMPERATURE RESOLUTION

The resolution of the ADC reading, Ma (°C/count), depends on both the ADC resolution N and the reference voltage used for conversion, as shown in Equation 19-2. It is recommended to use the smallest VREF value, such as 2.048 FVR reference voltage, instead of VDD.

Note: Refer to **Section 37.0 "Electrical Specifications"** for FVR reference voltage accuracy.

EQUATION 19-2: TEMPERATURE RESOLUTION (°C/LSb)

$$Ma = \frac{V_{REF}}{2^N} \times Mt$$

$$Ma = \frac{\frac{V_{REF}}{2^N}}{Mv}$$

Where:

Mv = sensor voltage sensitivity (V/°C)

VREF = Reference voltage of the ADC module (in Volts)

N = Resolution of the ADC

EXAMPLE 19-1: TEMPERATURE RESOLUTION

Using VREF = 2.048V and a 10-bit ADC provides 2 mV/LSb measurements.

Because Mv can vary from -2.40 to -2.65 mV/°C, the range of Ma = 0.75 to 0.83 °C/LSb.

19.3 ADC Acquisition Time

To ensure accurate temperature measurements, the user must wait a fixed amount of time for the ADC value to settle, after the ADC input multiplexer is connected to the temperature indicator output, before the conversion is performed. This specification is provided in **Section 37.0 "Electrical Specifications"**.

20.2.6 ADC CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

1. Configure Port:
   - Disable pin output driver (Refer to the TRIS register)
   - Configure pin as analog (Refer to the ANSEL register)
2. Configure the ADC module:
   - Select ADC conversion clock
   - Select voltage reference
   - Select ADC input channel
   - Turn on ADC module
3. Configure ADC interrupt (optional):
   - Clear ADC interrupt flag
   - Enable ADC interrupt
   - Enable peripheral interrupt
   - Enable global interrupt(1)
4. Wait the required acquisition time(2).
5. Start conversion by setting the GO/$\overline{\text{DONE}}$ bit.
6. Wait for ADC conversion to complete by one of the following:
   - Polling the GO/$\overline{\text{DONE}}$ bit
   - Waiting for the ADC interrupt
7. Read ADC Result.
8. Clear the ADC interrupt flag (required if interrupt is enabled).

Note 1: The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

2: Refer to **Section 20.3 "ADC Acquisition Requirements"**.

EXAMPLE 20-1: ADC CONVERSION

```
;This code block configures the ADC
;for polling, Vdd and Vss references, ADCRC
;oscillator and AN0 input.
;
;Conversion start & polling for completion ;
are included.
;
BANKSEL    ADCON1        ;
MOVLW      B'11110000'   ;Right justify, ADCRC
                         ;oscillator
MOVWF      ADCON1        ;Vdd and Vss Vref
BANKSEL    TRISA         ;
BSF        TRISA,0       ;Set RA0 to input
BANKSEL    ANSEL         ;
BSF        ANSEL,0       ;Set RA0 to analog
BANKSEL    ADCON0        ;
MOVLW      B'00000001'   ;Select channel AN0
MOVWF      ADCON0        ;Turn ADC On
CALL       SampleTime    ;Acquisiton delay
BSF        ADCON0,ADGO   ;Start conversion
BTFSC      ADCON0,ADGO   ;Is conversion done?
GOTO       $-1           ;No, test again
BANKSEL    ADRESH        ;
MOVF       ADRESH,W      ;Read upper 2 bits
MOVWF      RESULTHI      ;store in GPR space
BANKSEL    ADRESL        ;
MOVF       ADRESL,W      ;Read lower 8 bits
MOVWF      RESULTLO      ;Store in GPR space
```


22.0 NUMERICALLY CONTROLLED OSCILLATOR (NCO) MODULE

The Numerically Controlled Oscillator (NCO) module is a timer that uses overflow from the addition of an increment value to divide the input frequency. The advantage of the addition method over simple counter driven timer is that the output frequency resolution does not vary with the divider value. The NCO is most useful for application that requires frequency accuracy and fine resolution at a fixed duty cycle.

Features of the NCO include:

- 20-bit Increment Function
- Fixed Duty Cycle mode (FDC) mode
- Pulse Frequency (PF) mode
- Output Pulse Width Control
- Multiple Clock Input Sources
- Output Polarity Control
- Interrupt Capability

Figure 22-1 is a simplified block diagram of the NCO module.

23.12 Register Definitions: Comparator Control

REGISTER 23-1: CMxCON0: COMPARATOR Cx CONTROL REGISTER 0

R/W-0/0	R-0/0	U-0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
ON	OUT	—	POL	—	—	HYS	SYNC
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **ON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled and consumes no active power

bit 6 **OUT:** Comparator Output bit
If CxPOL = 1 (inverted polarity):
1 = CxVP < CxVN
0 = CxVP > CxVN
If CxPOL = 0 (noninverted polarity):
1 = CxVP > CxVN
0 = CxVP < CxVN

bit 5 **Unimplemented:** Read as '0'

bit 4 **POL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **HYS:** Comparator Hysteresis Enable bit
1 = Comparator hysteresis enabled
0 = Comparator hysteresis disabled

bit 0 **SYNC:** Comparator Output Synchronous Mode bit
1 = Comparator output to Timer1 and I/O pin is synchronous to changes on Timer1 clock source. Output updated on the falling edge of Timer1 clock source.
0 = Comparator output to Timer1 and I/O pin is asynchronous

REGISTER 23-5: CMOUT: COMPARATOR OUTPUT REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R-0/0	R-0/0
—	—	—	—	—	—	MC2OUT	MC1OUT
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **MC2OUT:** Mirror Copy of C2OUT bit

bit 0 **MC1OUT:** Mirror Copy of C1OUT bit

TABLE 23-3: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CMxCON0	ON	OUT	—	POL	—	—	HYS	SYNC	256
CMxCON1	—	—	—	—	—	—	INTP	INTN	257
CMOUT	—	—	—	—	—	—	MC2OUT	MC1OUT	259
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		216
DAC1CON0	DAC1EN	—	DAC1OE1	DAC1OE2	DAC1PSS<1:0>		—	DAC1NSS	238
DAC1CON1	—	—	—	DAC1R<4:0>					238
INTCON	GIE	PEIE	—					INTEDG	119
PIE2	—	ZCDIE	—	—	—	—	C2IE	C1IE	122
PIR2	—	ZCDIF	—	—	—	—	C2IF	C1IF	130
RxyPPS	—	—	—	RxyPPS<4:0>					197
CLCINxPPS	—	—	CLCIN0PPS<5:0>						196
T1GPPS	—	—	T1GPPS<5:0>						196

Legend: — = unimplemented location, read as ‘0’. Shaded cells are unused by the comparator module.

26.3 Timer Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

26.4 Secondary Oscillator

A dedicated low-power 32.768 kHz oscillator circuit is built-in between pins SOSCI (input) and SOSCO (amplifier output). This internal circuit is designed to be used in conjunction with an external 32.768 kHz crystal.

The oscillator circuit is enabled by setting the SOSCEN bit of the OSCEN register. The oscillator will continue to run during Sleep.

Note:	The oscillator requires a start-up and stabilization time before use. Thus, SOSCEN should be set and a suitable delay observed prior to using Timer1 with the SOSC source. A suitable delay similar to the OST delay can be implemented in software by clearing the TMR1IF bit then presetting the TMR1H:TMR1L register pair to FC00h. The TMR1IF flag will be set when 1024 clock cycles have elapsed, thereby indicating that the oscillator is running and reasonably stable.

26.5 Timer Operation in Asynchronous Counter Mode

If the control bit $\overline{\text{SYNC}}$ of the T1CON register is set, the external clock input is not synchronized. The timer increments asynchronously to the internal phase clocks. If the external clock source is selected then the timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see **Section 26.5.1 "Reading and Writing Timer1 in Asynchronous Counter Mode"**).

Note:	When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce an additional increment.

26.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TMR1L register pair.

26.6 Timer Gate

Timer1 can be configured to count freely or the count can be enabled and disabled using the time gate circuitry. This is also referred to as Timer Gate Enable.

The timer gate can also be driven by multiple selectable sources.

26.6.1 TIMER GATE ENABLE

The Timer Gate Enable mode is enabled by setting the GE bit of the T1GCON register. The polarity of the Timer Gate Enable mode is configured using the GPOL bit of the T1GCON register.

When Timer Gate Enable signal is enabled, the timer will increment on the rising edge of the Timer1 clock source. When Timer Gate Enable signal is disabled, the timer always increments, regardless of the GE bit. See Figure 26-3 for timing details.

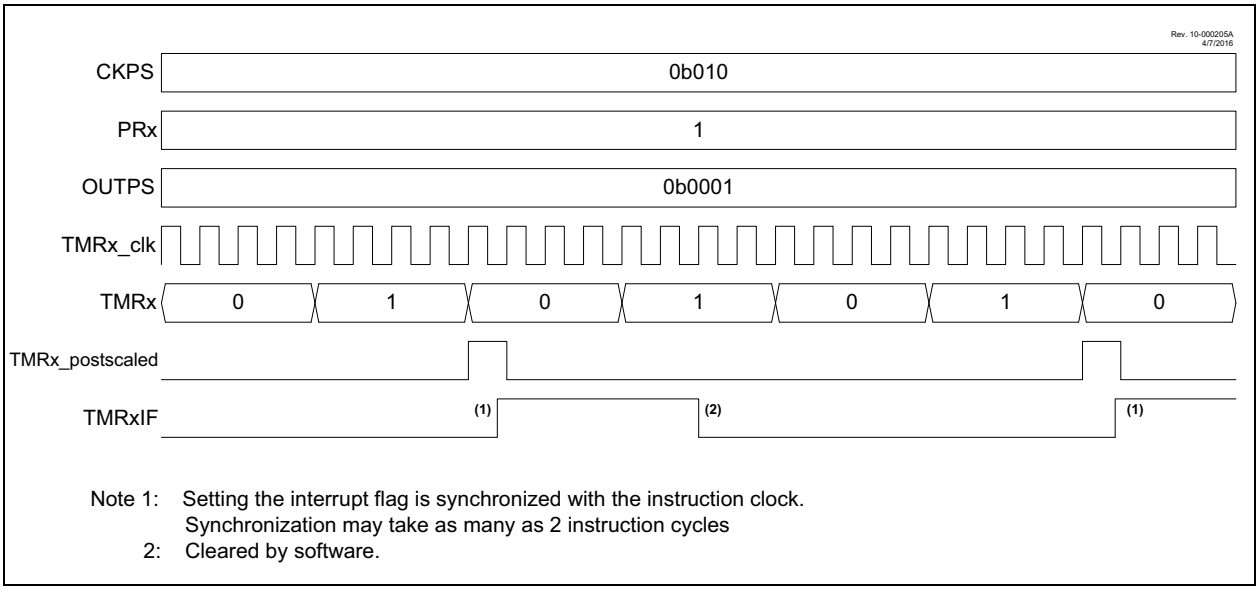
TABLE 26-2: TIMER GATE ENABLE SELECTIONS

T1CLK	T1GPOL	T1G	Timer Operation
↑	1	1	Counts
↑	1	0	Holds Count
↑	0	1	Holds Count
↑	0	0	Counts

27.4 Timer2 Interrupt

Timer2 can also generate a device interrupt. The interrupt is generated when the postscaler counter matches one of 16 postscale options (from 1:1 through 1:16), which are selected with the postscaler control bits, OUTPS<3:0> of the T2CON register. The interrupt is enabled by setting the TMR2IE interrupt enable bit of the PIE4 register. Interrupt timing is illustrated in Figure 27-3.

FIGURE 27-3: TIMER2 PRESCALER, POSTSCALER, AND INTERRUPT TIMING DIAGRAM



Note 1: Setting the interrupt flag is synchronized with the instruction clock. Synchronization may take as many as 2 instruction cycles
2: Cleared by software.

28.1 Capture Mode

Capture mode makes use of the 16-bit Timer1 resource. When an event occurs on the capture source, the 16-bit CCPRxH:CCPRxL register pair captures and stores the 16-bit value of the TMR1H:TMR1L register pair, respectively. An event is defined as one of the following and is configured by the CCPxMODE<3:0> bits of the CCPxCON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

When a capture is made, the Interrupt Request Flag bit CCPxIF of the PIR6 register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPRxH, CCPRxL register pair is read, the old captured value is overwritten by the new captured value.

Figure 28-1 shows a simplified diagram of the capture operation.

28.1.1 CAPTURE SOURCES

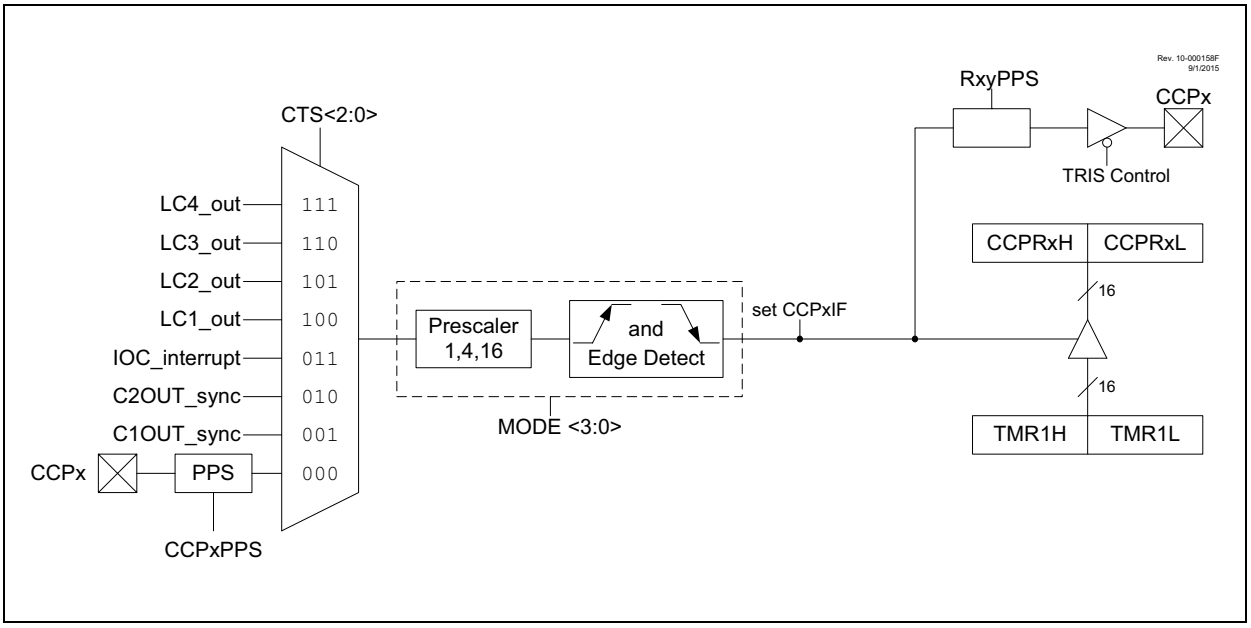
In Capture mode, the CCPx pin should be configured as an input by setting the associated TRIS control bit.

Note:	If the CCPx pin is configured as an output, a write to the port can cause a capture condition.

The capture source is selected by configuring the CCPxCTS<2:0> bits of the CCPxCAP register. The following sources can be selected:

- CCPxPPS input
- C1OUT_sync
- C2OUT_sync
- IOC_interrupt
- LC1_out
- LC2_out
- LC3_out
- LC4_out

FIGURE 28-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



30.10 Auto-Shutdown

Auto-shutdown is a method to immediately override the CWG output levels with specific overrides that allow for safe shutdown of the circuit. The shutdown state can be either cleared automatically or held until cleared by software. The auto-shutdown circuit is illustrated in Figure 30-12.

30.10.1 SHUTDOWN

The shutdown state can be entered by either of the following two methods:

- Software generated
- External Input

30.10.1.1 Software Generated Shutdown

Setting the SHUTDOWN bit of the CWG1AS0 register will force the CWG into the shutdown state.

When the auto-restart is disabled, the shutdown state will persist as long as the SHUTDOWN bit is set.

When auto-restart is enabled, the SHUTDOWN bit will clear automatically and resume operation on the next rising edge event.

30.10.2 EXTERNAL INPUT SOURCE

External shutdown inputs provide the fastest way to safely suspend CWG operation in the event of a Fault condition. When any of the selected shutdown inputs goes active, the CWG outputs will immediately go to the selected override levels without software delay. Several input sources can be selected to cause a shutdown condition. All input sources are active-low. The sources are:

- Comparator C1OUT_sync
- Comparator C2OUT_sync
- Timer2 – TMR2_postscaled
- CWG1IN input pin

Shutdown inputs are selected using the CWG1AS1 register (Register 30-6).

Note:	Shutdown inputs are level sensitive, not edge sensitive. The shutdown state cannot be cleared, except by disabling auto-shutdown, as long as the shutdown input level persists.

30.11 Operation During Sleep

The CWG module operates independently from the system clock and will continue to run during Sleep, provided that the clock and input sources selected remain active.

The HFINTOSC remains active during Sleep when all the following conditions are met:

- CWG module is enabled
- Input source is active
- HFINTOSC is selected as the clock source, regardless of the system clock source selected.

In other words, if the HFINTOSC is simultaneously selected as the system clock and the CWG clock source, when the CWG is enabled and the input source is active, then the CPU will go idle during Sleep, but the HFINTOSC will remain active and the CWG will continue to operate. This will have a direct effect on the Sleep mode current.

REGISTER 31-3: CLCxSEL0: GENERIC CLCx DATA 0 SELECT REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	LCxD1S<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **LCxD1S<5:0>:** CLCx Data1 Input Selection bits
See Table 31-2.

REGISTER 31-4: CLCxSEL1: GENERIC CLCx DATA 1 SELECT REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	LCxD2S<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **LCxD2S<5:0>:** CLCx Data 2 Input Selection bits
See Table 31-2.

REGISTER 31-5: CLCxSEL2: GENERIC CLCx DATA 2 SELECT REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	LCxD3S<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **LCxD3S<5:0>:** CLCx Data 3 Input Selection bits
See Table 31-2.

REGISTER 31-6: CLCxSEL3: GENERIC CLCx DATA 3 SELECT REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	LCxD4S<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **LCxD4S<5:0>:** CLCx Data 4 Input Selection bits
See Table 31-2.

32.6.5 I²C MASTER MODE REPEATED START CONDITION TIMING

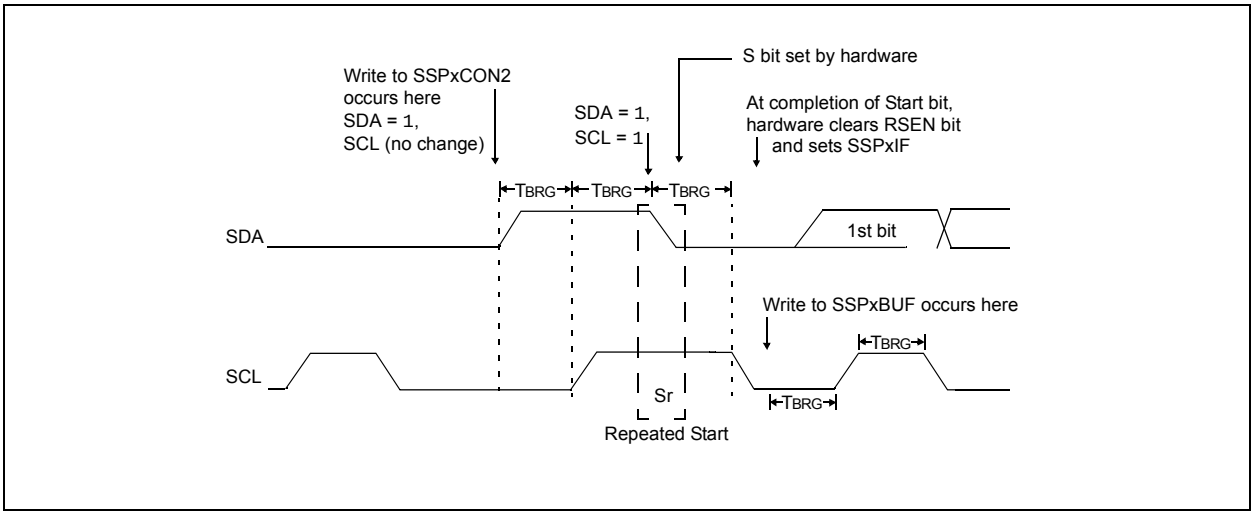
A Repeated Start condition (Figure 32-27) occurs when the RSEN bit of the SSPxCON2 register is programmed high and the master state machine is no longer active. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the Baud Rate Generator is loaded and begins counting. The SDA pin is released (brought high) for one Baud Rate Generator count (TBRG). When the Baud Rate Generator times out, if SDA is sampled high, the SCL pin will be deasserted (brought high). When SCL is sampled high, the Baud Rate Generator is reloaded and begins counting. SDA and SCL must be sampled high for one TBRG. This action is then followed by assertion of the SDA pin (SDA = 0) for one TBRG while SCL is high. SCL is asserted low. Following this, the RSEN bit of the SSPxCON2 register will be automatically cleared and the Baud Rate Generator will not be reloaded, leaving the SDA pin held low. As soon as a Start condition is detected on the SDA and SCL pins, the S bit of the SSPxSTAT register will be set. The SSPxIF bit will not be set until the Baud Rate Generator has timed out.

Note 1: If RSEN is programmed while any other event is in progress, it will not take effect.

2: A bus collision during the Repeated Start condition occurs if:

- SDA is sampled low when SCL goes from low-to-high.
- SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data '1'.

FIGURE 32-27: REPEATED START CONDITION WAVEFORM



33.4.2 SYNCHRONOUS SLAVE MODE

The following bits are used to configure the EUSART for synchronous slave operation:

- SYNC = 1
- CSRC = 0
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TXxSTA register configures the device for synchronous operation. Clearing the CSRC bit of the TXxSTA register configures the device as a slave. Clearing the SREN and CREN bits of the RCxSTA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RCxSTA register enables the EUSART.

33.4.2.1 EUSART Synchronous Slave Transmit

The operation of the Synchronous Master and Slave modes are identical (see **Section 33.4.1.3 "Synchronous Master Transmission")**, except in the case of the Sleep mode.

If two words are written to the TXxREG and then the SLEEP instruction is executed, the following will occur:

1. The first character will immediately transfer to the TSR register and transmit.
2. The second word will remain in the TXxREG register.
3. The TXxIF bit will not be set.
4. After the first character has been shifted out of TSR, the TXxREG register will transfer the second character to the TSR and the TXxIF bit will now be set.
5. If the PEIE and TXxIE bits are set, the interrupt will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will call the Interrupt Service Routine.

33.4.2.2 Synchronous Slave Transmission Set-up:

1. Set the SYNC and SPEN bits and clear the CSRC bit.
2. Clear the ANSEL bit for the CK pin (if applicable).
3. Clear the CREN and SREN bits.
4. If interrupts are desired, set the TXxIE bit of the PIE3 register and the GIE and PEIE bits of the INTCON register.
5. If 9-bit transmission is desired, set the TX9 bit.
6. Enable transmission by setting the TXEN bit.
7. If 9-bit transmission is selected, insert the Most Significant bit into the TX9D bit.
8. Start transmission by writing the Least Significant eight bits to the TXxREG register.

FIGURE 35-2: PICkit™ PROGRAMMER STYLE CONNECTOR INTERFACE

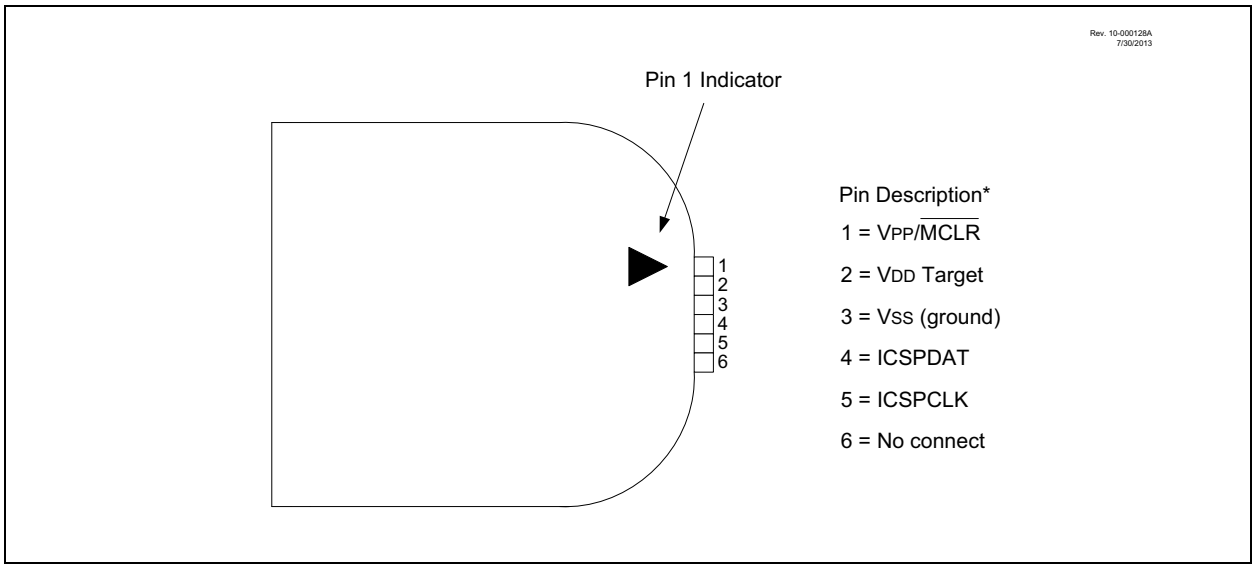


FIGURE 35-3: TYPICAL CONNECTION FOR ICSP™ PROGRAMMING

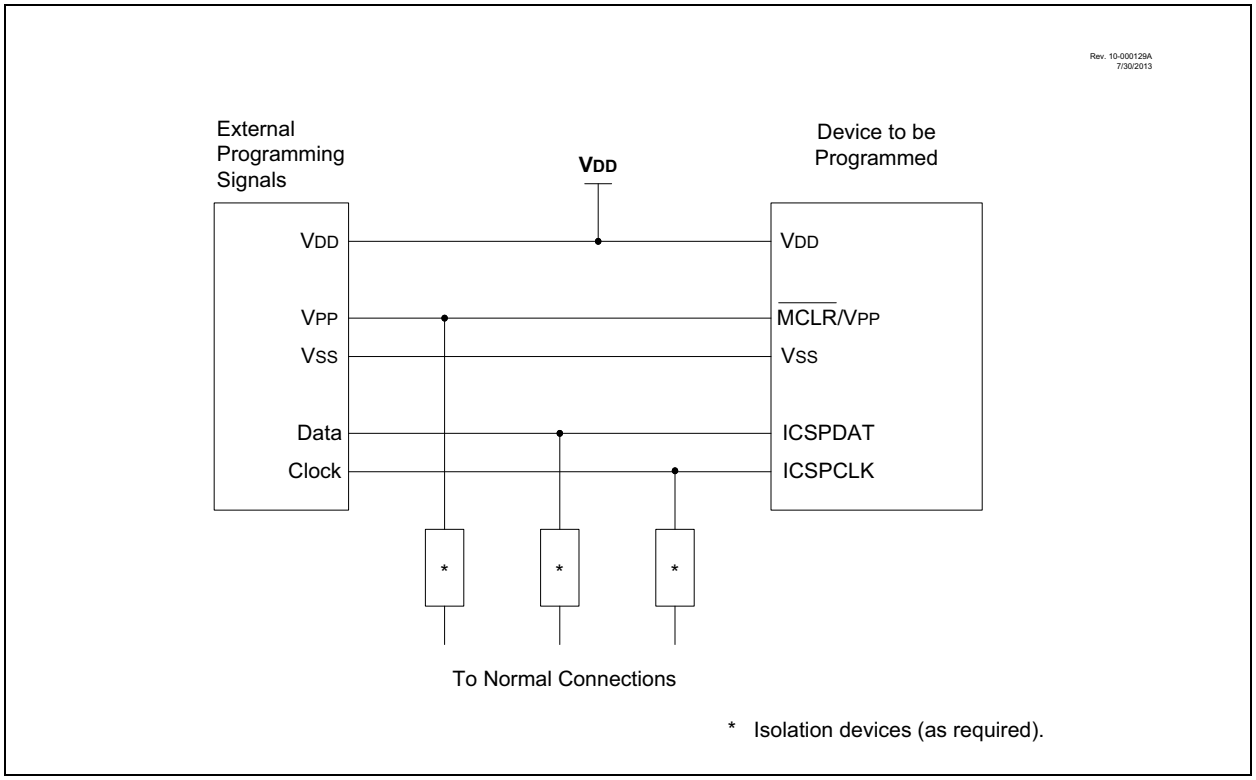


TABLE 37-9: PLL SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) $V_{DD} \geq 2.5V$							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
PLL01	F_{PLLIN}	PLL Input Frequency Range	4	—	8	MHz	
PLL02	F_{PLLOUT}	PLL Output Frequency Range	16	—	32	MHz	**Note 1**
PLL03	T_{PLLST}	PLL Lock Time from Start-up	—	200	—	µs	
PLL04	F_{PLLJIT}	PLL Output Frequency Stability (Jitter)	-0.25	—	0.25	%	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The output frequency of the PLL must meet the F_{OSC} requirements listed in Parameter D002.

FIGURE 37-17: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)

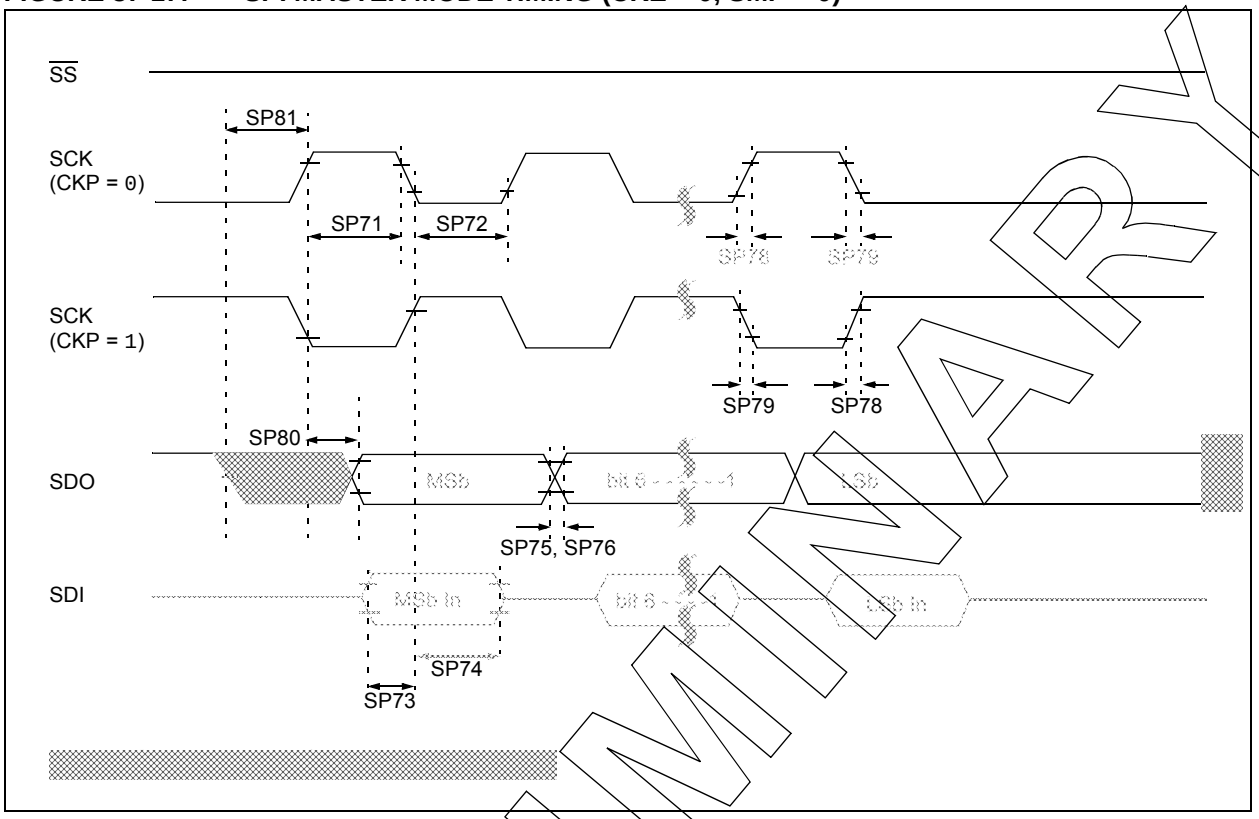
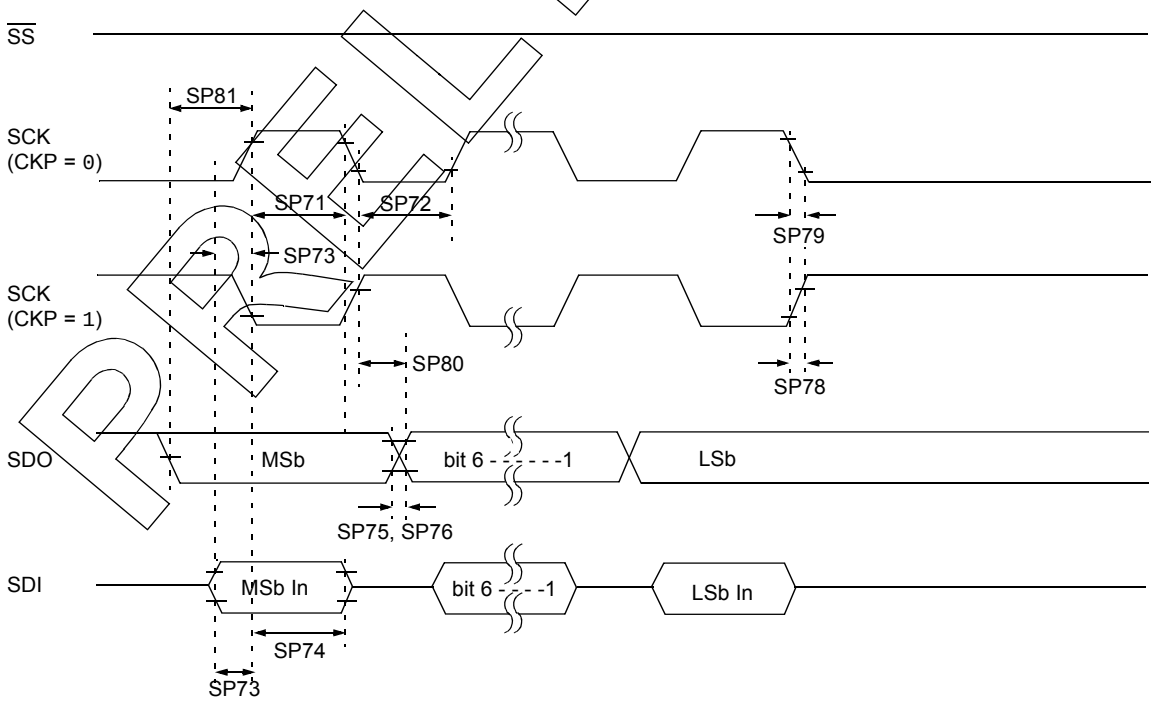


FIGURE 37-18: SPI MASTER MODE TIMING (CKE = 1, SMP = 1)



Note: Refer to Figure 37-4 for load conditions.

