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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	224 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16lf15355-e-so">https://www.e-xfl.com/product-detail/microchip-technology/pic16lf15355-e-so</a>

# PIC16(L)F15354/55

**TABLE 1-2: PIC16(L)F15354/55 PINOUT DESCRIPTION**

Name	Function	Input Type	Output Type	Description
RA0/ANA0/C1IN0-/C2IN0-/CLCIN0 <sup>(1)</sup> /IOCA0	RA0	TTL/ST	CMOS/OD	General purpose I/O.
	ANA0	AN	—	ADC Channel A0 input.
	C1IN0-	AN	—	Comparator 1 negative input.
	C2IN0-	AN	—	Comparator 2 negative input.
	CLCIN0 <sup>(1)</sup>	TTL/ST	—	Configurable Logic Cell source input.
	IOCA0	TTL/ST	—	Interrupt-on-change input.
RA1/ANA1/C1IN1-/C2IN1-/CLCIN1 <sup>(1)</sup> /IOCA1	RA1	TTL/ST	CMOS/OD	General purpose I/O.
	ANA1	AN	—	ADC Channel A1 input.
	C1IN1-	AN	—	Comparator 1 negative input.
	C2IN1-	AN	—	Comparator 2 negative input.
	CLCIN1 <sup>(1)</sup>	TTL/ST	—	Configurable Logic Cell source input.
	IOCA1	TTL/ST	—	Interrupt-on-change input.
RA2/ANA2/C1IN0+/C2IN0+/VREF-/DAC1OUT1/IOCA2	RA2	TTL/ST	CMOS/OD	General purpose I/O.
	ANA2	AN	—	ADC Channel A2 input.
	C1IN0+	AN	—	Comparator 2 positive input.
	C2IN0+	AN	—	Comparator 2 positive input.
	DAC1OUT1	—	AN	Digital-to-Analog Converter output.
	IOCA2	TTL/ST	—	Interrupt-on-change input.
RA3/ANA3/C1IN1+/VREF+/IOCA3/DAC1REF+	RA3	TTL/ST	CMOS/OD	General purpose I/O.
	ANA3	AN	—	ADC Channel A3 input.
	C1IN1+	AN	—	Comparator 1 positive input.
	VREF+	AN	—	External ADC and/or DAC positive reference input.
	IOCA3	TTL/ST	—	Interrupt-on-change input.
	DAC1REF+	TTL/ST	AN	DAC positive reference.
RA4/ANA4/T0CKI <sup>(1)</sup> /IOCA4	RA4	TTL/ST	CMOS/OD	General purpose I/O.
	ANA4	AN	—	ADC Channel A4 input.
	T0CKI <sup>(1)</sup>	TTL/ST	—	Timer0 clock input.
	IOCA4	TTL/ST	—	Interrupt-on-change input.
RA5/ANA5/SS1 <sup>(1)</sup> /IOCA5	RA5	TTL/ST	CMOS/OD	General purpose I/O.
	ANA5	AN	—	ADC Channel A5 input.
	SS1 <sup>(1)</sup>	TTL/ST	—	MSSP1 SPI slave select input.
	IOCA5	TTL/ST	—	Interrupt-on-change input.

**Legend:** AN = Analog input or output      CMOS = CMOS compatible input or output      OD = Open-Drain  
TTL = TTL compatible input      ST = Schmitt Trigger input with CMOS levels      I<sup>2</sup>C = Schmitt Trigger input with I<sup>2</sup>C  
HV = High Voltage      XTAL = Crystal levels

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-2 for details on which PORT pins may be used for this signal.
  - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-3.
  - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
  - 4: These pins are configured for I<sup>2</sup>C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBus input buffer thresholds.

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**TABLE 1-2: PIC16(L)F15354/55 PINOUT DESCRIPTION (CONTINUED)**

Name	Function	Input Type	Output Type	Description
RE3/ANE3/IOCE3/MCLR/VPP	RE3	TTL/ST	—	General purpose input only (when MCLR is disabled by the Configuration bit).
	IOCE3	TTL/ST	—	Interrupt-on-change input.
	MCLR	ST	—	Master clear input with internal weak pull up resistor.
	VPP	HV	—	ICSP™ High-Voltage Programming mode entry input.
VDD	VDD	Power	—	Positive supply voltage input.
VSS		Power	—	Ground reference.

**Legend:** AN = Analog input or output      CMOS = CMOS compatible input or output      OD = Open-Drain  
TTL = TTL compatible input      ST = Schmitt Trigger input with CMOS levels      I<sup>2</sup>C = Schmitt Trigger input with I<sup>2</sup>C  
HV = High Voltage      XTAL = Crystal levels

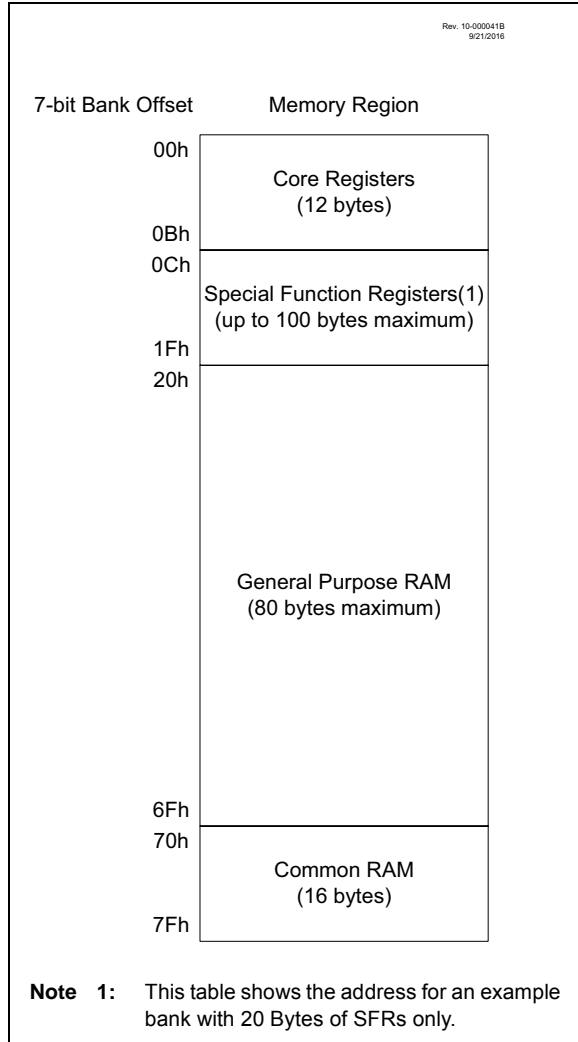
- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-2 for details on which PORT pins may be used for this signal.
  - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-3.
  - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
  - 4: These pins are configured for I<sup>2</sup>C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBus input buffer thresholds.

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## 4.3 Data Memory Organization

The data memory is partitioned into 64 memory banks with 128 bytes in each bank.

**FIGURE 4-3: BANKED MEMORY PARTITIONING**



Each bank consists of:

- 12 core registers
- Up to 100 Special Function Registers (SFR)
- Up to 80 bytes of General Purpose RAM (GPR)
- 16 bytes of common RAM

### 4.3.1 BANK SELECTION

The active bank is selected by writing the bank number into the Bank Select Register (BSR). Unimplemented memory will read as '0'. All data memory can be accessed either directly (via instructions that use the file registers) or indirectly via the two File Select Registers (FSR). See **Section 4.6 "Indirect Addressing"** for more information.

Data memory uses a 13-bit address. The upper six bits of the address define the Bank address and the lower seven bits select the registers/RAM in that bank.

### 4.3.2 CORE REGISTERS

The core registers contain the registers that directly affect the basic operation. The core registers occupy the first 12 addresses of every data memory bank (addresses x00h/x08h through x0Bh/x8Bh). These registers are listed below in Table 4-3.

**TABLE 4-3: CORE REGISTERS**

Addresses	BANKx
x00h or x80h	INDF0
x01h or x81h	INDF1
x02h or x82h	PCL
x03h or x83h	STATUS
x04h or x84h	FSR0L
x05h or x85h	FSR0H
x06h or x86h	FSR1L
x07h or x87h	FSR1H
x08h or x88h	BSR
x09h or x89h	WREG
x0Ah or x8Ah	PCLATH
x0Bh or x8Bh	INTCON

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## 4.3.3 SPECIAL FUNCTION REGISTER

The Special Function Registers are registers used by the application to control the desired operation of peripheral functions in the device. The Special Function Registers occupy the 20 bytes of the data banks 0-59 and 100 bytes of the data banks 60-63, after the core registers.

The SFRs associated with the operation of the peripherals are described in the appropriate peripheral chapter of this data sheet.

## 4.3.4 GENERAL PURPOSE RAM

There are up to 80 bytes of GPR in each data memory bank.

### 4.3.4.1 Linear Access to GPR

The general purpose RAM can be accessed in a non-banked method via the FSRs. This can simplify access to large memory structures. See **Section 4.6.2 “Linear Data Memory”** for more information.

## 4.3.5 COMMON RAM

There are 16 bytes of common RAM accessible from all banks.

## 4.3.6 DEVICE MEMORY MAPS

The memory maps are as shown in Table 4-4 through Table 4-9.

**TABLE 4-10: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 (CONTINUED)**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
<b>Bank 14</b>											
CPU CORE REGISTERS; see Table 4-3 for specifics											
70Ch	PIR0	—	—	TMR0IF	IOCIF	—	—	—	INTF	--00 ---0	--00 ---0
70Dh	PIR1	OSFIF	CSWIF	—	—	—	—	ADTIF	ADIF	00-- --00	00-- --00
70Eh	PIR2	—	ZCDIF	—	—	—	—	C2IF	C1IF	-0-- --00	-0-- --00
70Fh	PIR3	RC2IF	TX2IF	RC1IF	TX1IF	BCL2IF	SSP2IF	BCL1IF	SSP1IF	0000 0000	0000 0000
710h	PIR4	—	—	—	—	—	—	TMR2IF	TMR1IF	---- --00	---- --00
711h	PIR5	CLC4IF	CLC3IF	CLC2IF	CLC1IF	—	—	—	TMR1GIF	0000 ---0	0000 ---0
712h	PIR6	—	—	—	—	—	—	CCP2IF	CCP1IF	---- --00	---- --00
713h	PIR7	—	—	NVMIF	NCO1IF	—	—	—	CWG1IF	--00 ---0	--00 ---0
714h	—	Unimplemented								---- ----	---- ----
715h	—	Unimplemented								---- ----	---- ----
716h	PIE0	—	—	TMR0IE	IOCIE	—	—	—	INTE	--00 ---0	--00 ---0
717h	PIE1	OSFIE	CSWIE	—	—	—	—	ADTIE	ADIE	00-- --00	00-- --00
718h	PIE2	—	ZCDIE	—	—	—	—	C2IE	C1IE	-0-- --00	-0-- --00
719h	PIE3	RC2IE	TX2IE	RC1IE	TX1IE	BCL2IE	SSP2IE	BCL1IE	SSP1IE	0000 0000	0000 0000
71Ah	PIE4	—	—	—	—	—	—	TMR2IE	TMR1IE	---- --00	---- --00
71Bh	PIE5	CLC4IE	CLC3IE	CLC2IE	CLC1IE	—	—	—	TMR1GIE	0000 ---0	0000 ---0
71Ch	PIE6	—	—	—	—	—	—	CCP2IE	CCP1IE	---- --00	---- --00
71Dh	PIE7	—	—	NVMIE	NCO1IE	—	—	—	CWG1IE	--00 ---0	--00 ---0
71Eh	—	Unimplemented								---- ----	---- ----
71Fh	—	Unimplemented								---- ----	---- ----

**Legend:** x = unknown, u = unchanged, □ = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

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## REGISTER 10-2: PIE0: PERIPHERAL INTERRUPT ENABLE REGISTER 0

U-0	U-0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	R/W-0/0
—	—	TMR0IE	IOCE	—	—	—	INTE
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware set

- bit 7-6      **Unimplemented:** Read as '0'
- bit 5      **TMROIE:** Timer0 Overflow Interrupt Enable bit  
1 = Enables the Timer0 interrupt  
0 = Disables the Timer0 interrupt
- bit 4      **IOCE:** Interrupt-on-Change Interrupt Enable bit  
1 = Enables the IOC change interrupt  
0 = Disables the IOC change interrupt
- bit 3-1      **Unimplemented:** Read as '0'
- bit 0      **INTE:** INT External Interrupt Flag bit<sup>(1)</sup>  
1 = Enables the INT external interrupt  
0 = Disables the INT external interrupt

**Note 1:** The External Interrupt GPIO pin is selected by INTPPS (Register 15-1).

**Note:** Bit PEIE of the INTCON register must be set to enable any peripheral interrupt controlled by PIE1-PIE7. Interrupt sources controlled by the PIE0 register do not require PEIE to be set in order to allow interrupt vectoring (when GIE is set).

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**REGISTER 13-6: NVMCON2: NONVOLATILE MEMORY CONTROL 2 REGISTER**

W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0
NVMCON2<7:0>							
bit 7							bit 0

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
S = Bit can only be set	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0      **NVMCON2<7:0>**: Flash Memory Unlock Pattern bits  
 To unlock writes, a 55h must be written first followed by an AAh before setting the WR bit of the NVMCON1 register. The value written to this register is used to unlock the writes.

**TABLE 13-5: SUMMARY OF REGISTERS ASSOCIATED WITH NONVOLATILE MEMORY (NVM)**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page	
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	119	
PIE7	—	—	NVMIE	NCO1IE	—	—	—	CWG1IE	127	
PIR7	—	—	NVMIF	NCO1IF	—	—	—	CWG1IF	135	
NVMCON1	—	NVMREGS	LWLO	FREE	WRERR	WREN	WR	RD	168	
NVMCON2	NVMCON2<7:0>								169	
NVMADRL	NVMADR<7:0>								167	
NVMADRH	— <sup>(1)</sup>	NVMADR<14:8>								167
NVMDATL	NVMDAT<7:0>								167	
NVMDATH	—	—	NVMDAT<13:8>						167	

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by NVM.

**Note 1:** Unimplemented, read as '1'.



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## REGISTER 14-20: ANSELC: PORTC ANALOG SELECT REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	ANSC1	ANSC0
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
u = Bit is unchanged                  x = Bit is unknown                  -n/n = Value at POR and BOR/Value at all other Resets  
'1' = Bit is set                          '0' = Bit is cleared

bit 7-0            **ANSC<7:0>**: Analog Select between Analog or Digital Function on Pins RC<7:0>, respectively<sup>(1)</sup>  
0 = Digital I/O. Pin is assigned to port or digital special function.  
1 = Analog input. Pin is assigned as analog input<sup>(1)</sup>. Digital input buffer disabled.

**Note 1:** When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

## REGISTER 14-21: WPUC: WEAK PULL-UP PORTC REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
WPUC7	WPUC6	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
u = Bit is unchanged                  x = Bit is unknown                  -n/n = Value at POR and BOR/Value at all other Resets  
'1' = Bit is set                          '0' = Bit is cleared

bit 7-0            **WPUC<7:0>**: Weak Pull-up Register bits  
1 = Pull-up enabled  
0 = Pull-up disabled

**TABLE 18-1: SUMMARY OF REGISTERS ASSOCIATED WITH FIXED VOLTAGE REFERENCE**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		216
ADCON0	CHS<5:0>						GO/DONE	ADON	229
ADCON1	ADFM	ADCS<2:0>			—	—	ADPREF<1:0>		230
DAC1CON0	DAC1EN	—	DAC1OE1	DAC1OE2	DAC1PSS<1:0>		—	DAC1NSS	238

**Legend:** — = unimplemented locations read as '0'. Shaded cells are not used with the Fixed Voltage Reference.

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## 22.1 NCO OPERATION

The NCO operates by repeatedly adding a fixed value to an accumulator. Additions occur at the input clock rate. The accumulator will overflow with a carry periodically, which is the raw NCO output (NCO\_overflow). This effectively reduces the input clock by the ratio of the addition value to the maximum accumulator value. See Equation 22-1.

The NCO output can be further modified by stretching the pulse or toggling a flip-flop. The modified NCO output is then distributed internally to other peripherals and can be optionally output to a pin. The accumulator overflow also generates an interrupt (NCO\_overflow).

The NCO period changes in discrete steps to create an average frequency.

### EQUATION 22-1: NCO OVERFLOW FREQUENCY

$$F_{OVERFLOW} = \frac{NCO \text{ Clock Frequency} \times \text{Increment Value}}{2^{20}}$$

#### 22.1.1 NCO CLOCK SOURCES

Clock sources available to the NCO include:

- HFINTOSC
- Fosc
- LC1\_out
- LC2\_out
- LC3\_out
- LC4\_out
- MFINTOSC (500 kHz)
- MFINTOSC (32 kHz)
- SOSC
- CLKR

The NCO clock source is selected by configuring the N1CKS<2:0> bits in the NCO1CLK register.

#### 22.1.2 ACCUMULATOR

The accumulator is a 20-bit register. Read and write access to the accumulator is available through three registers:

- NCO1ACCL
- NCO1ACCH
- NCO1ACCU

#### 22.1.3 ADDER

The NCO Adder is a full adder, which operates synchronously from the source clock. The addition of the previous result and the increment value replaces the accumulator value on the rising edge of each input clock.

#### 22.1.4 INCREMENT REGISTERS

The increment value is stored in three registers making up a 20-bit incrementer. In order of LSB to MSB they are:

- NCO1INCL
- NCO1INCH
- NCO1INCUI

When the NCO module is enabled, the NCO1INCUI and NCO1INCH registers should be written first, then the NCO1INCL register. Writing to the NCO1INCL register initiates the increment buffer registers to be loaded simultaneously on the second rising edge of the NCO\_clk signal.

The registers are readable and writable. The increment registers are double-buffered to allow value changes to be made without first disabling the NCO module.

When the NCO module is disabled, the increment buffers are loaded immediately after a write to the increment registers.

**Note:** The increment buffer registers are not user-accessible.

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## 23.2 Comparator Control

Each comparator has two control registers: CMxCON0 and CMxCON1.

The CMxCON0 register (see Register 23-1) contains Control and Status bits for the following:

- Enable
- Output
- Output polarity
- Hysteresis enable
- Timer1 output synchronization

The CMxCON1 register (see Register 23-2) contains Control bits for the following:

- Interrupt on positive/negative edge enables
- The CMxNSEL and CMxPSEL (Register 23-3 and Register 23-4) contain control bits for the following:
  - Positive input channel selection
  - Negative input channel selection

### 23.2.1 COMPARATOR ENABLE

Setting the CxON bit of the CMxCON0 register enables the comparator for operation. Clearing the CxON bit disables the comparator resulting in minimum current consumption.

### 23.2.2 COMPARATOR OUTPUT

The output of the comparator can be monitored by reading either the CxOUT bit of the CMxCON0 register or the MCxOUT bit of the CMOUT register.

The comparator output can also be routed to an external pin through the RxyPPS register (Register 15-2). The corresponding TRIS bit must be clear to enable the pin as an output.

**Note 1:** The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched.

### 23.2.3 COMPARATOR OUTPUT POLARITY

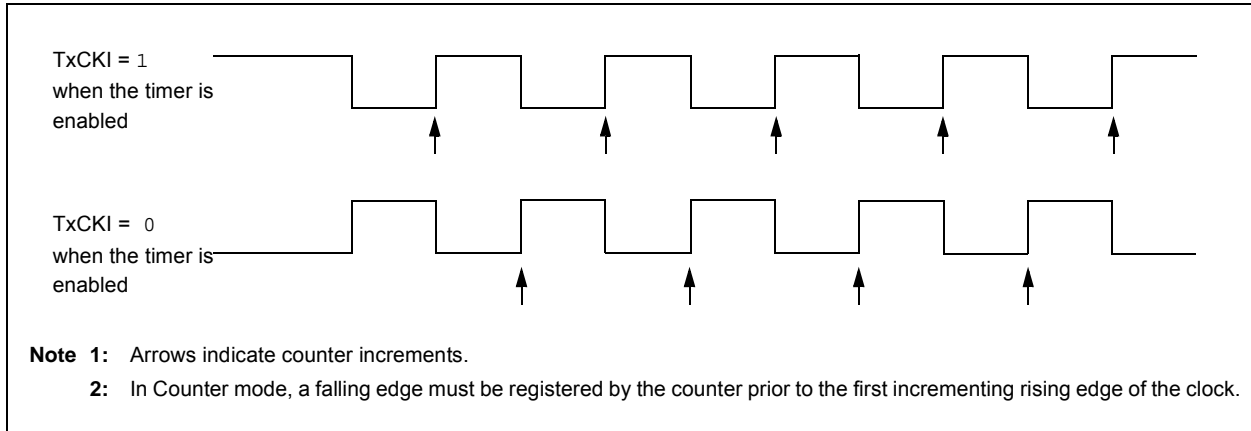
Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CxPOL bit of the CMxCON0 register. Clearing the CxPOL bit results in a non-inverted output.

Table 23-2 shows the output state versus input conditions, including polarity control.

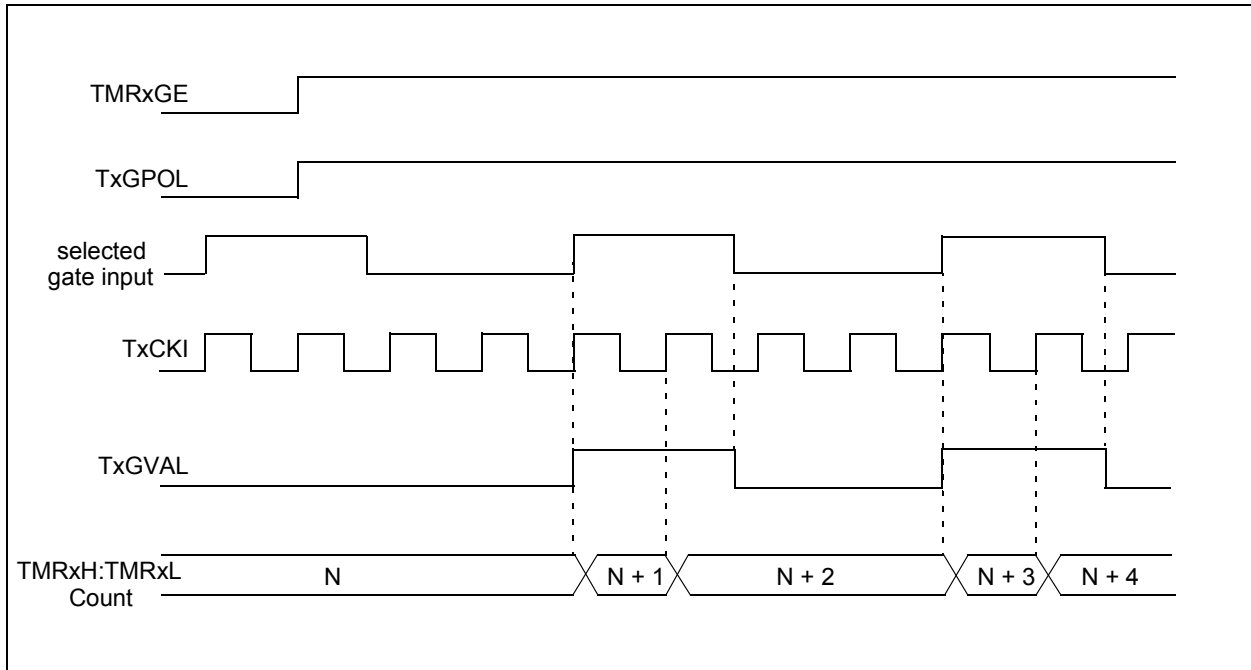
**TABLE 23-2: COMPARATOR OUTPUT STATE VS. INPUT CONDITIONS**

Input Condition	CxPOL	CxOUT
$CxVN > CxVP$	0	0
$CxVN < CxVP$	0	1
$CxVN > CxVP$	1	1
$CxVN < CxVP$	1	0

**FIGURE 26-2: TIMER1 INCREMENTING EDGE**



**FIGURE 26-3: TIMER1 GATE ENABLE MODE**



**TABLE 27-1: TIMER2 OPERATING MODES**

Mode	MODE<4:0>		Output Operation	Operation	Timer Control			
	<4:3>	<2:0>			Start	Reset	Stop	
Free Running Period	00	000	Period Pulse	Software gate (Figure 27-4)	ON = 1	—	ON = 0	
		001		Hardware gate, active-high (Figure 27-5)	ON = 1 and TMRx_ers = 1	—	ON = 0 or TMRx_ers = 0	
		010		Hardware gate, active-low	ON = 1 and TMRx_ers = 0	—	ON = 0 or TMRx_ers = 1	
		011	Period Pulse with Hardware Reset	Rising or falling edge Reset	ON = 1	TMRx_ers ↓	ON = 0	
		100		Rising edge Reset (Figure 27-6)		TMRx_ers ↑		
		101		Falling edge Reset		TMRx_ers ↓		
		110		Low level Reset		TMRx_ers = 0	ON = 0 or TMRx_ers = 0	
		111		High level Reset (Figure 27-7)		TMRx_ers = 1	ON = 0 or TMRx_ers = 1	
One-shot	01	000	One-shot	Software start (Figure 27-8)	ON = 1	—	ON = 0 or Next clock after TMRx = PRx (Note 2)	
		001	Edge triggered start (Note 1)	Rising edge start (Figure 27-9)	ON = 1 and TMRx_ers ↑	—		
		010		Falling edge start	ON = 1 and TMRx_ers ↓	—		
		011		Any edge start	ON = 1 and TMRx_ers ↓	—		
		100	Edge triggered start and hardware Reset (Note 1)	Rising edge start and Rising edge Reset (Figure 27-10)	ON = 1 and TMRx_ers ↑	TMRx_ers ↑		
		101		Falling edge start and Falling edge Reset	ON = 1 and TMRx_ers ↓	TMRx_ers ↓		
		110		Rising edge start and Low level Reset (Figure 27-11)	ON = 1 and TMRx_ers ↑	TMRx_ers = 0		
		111		Falling edge start and High level Reset	ON = 1 and TMRx_ers ↓	TMRx_ers = 1		
Mono-stable	10	000	Reserved					
		001	Edge triggered start (Note 1)	Rising edge start (Figure 27-12)	ON = 1 and TMRx_ers ↑	—	ON = 0 or Next clock after TMRx = PRx (Note 3)	
		010		Falling edge start	ON = 1 and TMRx_ers ↓	—		
		011		Any edge start	ON = 1 and TMRx_ers ↓	—		
		Reserved	100	Reserved				
		Reserved	101	Reserved				
		One-shot	11	110	Level triggered start and hardware Reset	High level start and Low level Reset (Figure 27-13)	ON = 1 and TMRx_ers = 1	TMRx_ers = 0
111	Low level start & High level Reset			ON = 1 and TMRx_ers = 0		TMRx_ers = 1		
Reserved	11	xxx	Reserved					

- Note 1:** If ON = 0 then an edge is required to restart the timer after ON = 1.  
**Note 2:** When TMRx = PRx then the next clock clears ON and stops TMRx at 00h.  
**Note 3:** When TMRx = PRx then the next clock stops TMRx at 00h but does not clear ON.

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## REGISTER 27-4: T2RST: TIMER2 EXTERNAL RESET SIGNAL SELECTION REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	RSEL<3:0>			
bit 7				bit 0			

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-4

**Unimplemented:** Read as '0'

bit 3-0

**RSEL<4:0>:** Timer2 External Reset Signal Source Selection bits

1111 = Reserved

1101 = LC4\_out

1100 = LC3\_out

1011 = LC2\_out

1010 = LC1\_out

1001 = ZCD1\_output

1000 = C2OUT\_sync

0111 = C1OUT\_sync

0110 = PWM6\_out

0101 = PWM5\_out

0100 = PWM4\_out

0011 = PWM3\_out

0010 = CCP2\_out

0001 = CCP1\_out

0000 = T2INPPS

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## REGISTER 29-2: PWMxDCH: PWM DUTY CYCLE HIGH BITS

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
PWMxDC<9:2>							
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
u = Bit is unchanged                  x = Bit is unknown                      -n/n = Value at POR and BOR/Value at all other Resets  
'1' = Bit is set                          '0' = Bit is cleared

bit 7-0                      **PWMxDC<9:2>**: PWM Duty Cycle Most Significant bits  
These bits are the MSBs of the PWM duty cycle. The two LSBs are found in PWMxDCL Register.

## REGISTER 29-3: PWMxDCL: PWM DUTY CYCLE LOW BITS

R/W-x/u	R/W-x/u	U-0	U-0	U-0	U-0	U-0	U-0
PWMxDC<1:0>		—	—	—	—	—	—
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
u = Bit is unchanged                  x = Bit is unknown                      -n/n = Value at POR and BOR/Value at all other Resets  
'1' = Bit is set                          '0' = Bit is cleared

bit 7-6                      **PWMxDC<1:0>**: PWM Duty Cycle Least Significant bits  
These bits are the LSBs of the PWM duty cycle. The MSBs are found in PWMxDCH Register.

bit 5-0                      **Unimplemented**: Read as '0'



## REGISTER 31-2: CLCxPOL: SIGNAL POLARITY CONTROL REGISTER

R/W-0/0	U-0	U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LCxPOL	—	—	—	LCxG4POL	LCxG3POL	LCxG2POL	LCxG1POL
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

- bit 7      **LCxPOL:** CLCxOUT Output Polarity Control bit  
1 = The output of the logic cell is inverted  
0 = The output of the logic cell is not inverted
- bit 6-4    **Unimplemented:** Read as '0'
- bit 3      **LCxG4POL:** Gate 3 Output Polarity Control bit  
1 = The output of gate 3 is inverted when applied to the logic cell  
0 = The output of gate 3 is not inverted
- bit 2      **LCxG3POL:** Gate 2 Output Polarity Control bit  
1 = The output of gate 2 is inverted when applied to the logic cell  
0 = The output of gate 2 is not inverted
- bit 1      **LCxG2POL:** Gate 1 Output Polarity Control bit  
1 = The output of gate 1 is inverted when applied to the logic cell  
0 = The output of gate 1 is not inverted
- bit 0      **LCxG1POL:** Gate 0 Output Polarity Control bit  
1 = The output of gate 0 is inverted when applied to the logic cell  
0 = The output of gate 0 is not inverted



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## 32.6.6 I<sup>2</sup>C MASTER MODE TRANSMISSION

Transmission of a data byte, a 7-bit address or the other half of a 10-bit address is accomplished by simply writing a value to the SSPxBUF register. This action will set the Buffer Full flag bit, BF, and allow the Baud Rate Generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDA pin after the falling edge of SCL is asserted. SCL is held low for one Baud Rate Generator rollover count (TBRG). Data should be valid before SCL is released high. When the SCL pin is released high, it is held that way for TBRG. The data on the SDA pin must remain stable for that duration and some hold time after the next falling edge of SCL. After the eighth bit is shifted out (the falling edge of the eighth clock), the BF flag is cleared and the master releases SDA. This allows the slave device being addressed to respond with an ACK bit during the ninth bit time if an address match occurred, or if data was received properly. The status of  $\overline{\text{ACK}}$  is written into the ACKSTAT bit on the rising edge of the ninth clock. If the master receives an Acknowledge, the Acknowledge Status bit, ACKSTAT, is cleared. If not, the bit is set. After the ninth clock, the SSPxIF bit is set and the master clock (Baud Rate Generator) is suspended until the next data byte is loaded into the SSPxBUF, leaving SCL low and SDA unchanged (Figure 32-28).

After the write to the SSPxBUF, each bit of the address will be shifted out on the falling edge of SCL until all seven address bits and the R/W bit are completed. On the falling edge of the eighth clock, the master will release the SDA pin, allowing the slave to respond with an Acknowledge. On the falling edge of the ninth clock, the master will sample the SDA pin to see if the address was recognized by a slave. The status of the ACK bit is loaded into the ACKSTAT Status bit of the SSPxCON2 register. Following the falling edge of the ninth clock transmission of the address, the SSPxIF is set, the BF flag is cleared and the Baud Rate Generator is turned off until another write to the SSPxBUF takes place, holding SCL low and allowing SDA to float.

### 32.6.6.1 BF Status Flag

In Transmit mode, the BF bit of the SSPxSTAT register is set when the CPU writes to SSPxBUF and is cleared when all eight bits are shifted out.

### 32.6.6.2 WCOL Status Flag

If the user writes the SSPxBUF when a transmit is already in progress (i.e., SSPxSR is still shifting out a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

WCOL must be cleared by software before the next transmission.

### 32.6.6.3 ACKSTAT Status Flag

In Transmit mode, the ACKSTAT bit of the SSPxCON2 register is cleared when the slave has sent an Acknowledge ( $\text{ACK} = 0$ ) and is set when the slave does not Acknowledge ( $\text{ACK} = 1$ ). A slave sends an Acknowledge when it has recognized its address (including a general call), or when the slave has properly received its data.

### 32.6.6.4 Typical transmit sequence:

1. The user generates a Start condition by setting the SEN bit of the SSPxCON2 register.
2. SSPxIF is set by hardware on completion of the Start.
3. SSPxIF is cleared by software.
4. The MSSP module will wait the required start time before any other operation takes place.
5. The user loads the SSPxBUF with the slave address to transmit.
6. Address is shifted out the SDA pin until all eight bits are transmitted. Transmission begins as soon as SSPxBUF is written to.
7. The MSSP module shifts in the  $\overline{\text{ACK}}$  bit from the slave device and writes its value into the ACKSTAT bit of the SSPxCON2 register.
8. The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSPxIF bit.
9. The user loads the SSPxBUF with eight bits of data.
10. Data is shifted out the SDA pin until all eight bits are transmitted.
11. The MSSP module shifts in the  $\overline{\text{ACK}}$  bit from the slave device and writes its value into the ACKSTAT bit of the SSPxCON2 register.
12. Steps 8-11 are repeated for all transmitted data bytes.
13. The user generates a Stop or Restart condition by setting the PEN or RSEN bits of the SSPxCON2 register. Interrupt is generated once the Stop/Restart condition is complete.

## REGISTER 32-3: SSPxCON2: SSPx CONTROL REGISTER 2 (I<sup>2</sup>C MODE ONLY)<sup>(1)</sup>

R/W-0/0	R/HS/HC-0	R/W-0/0	R/S/HC-0/0	R/S/HC-0/0	R/S/HC-0/0	R/S/HC-0/0	R/S/HC-0/0
GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

### Legend:

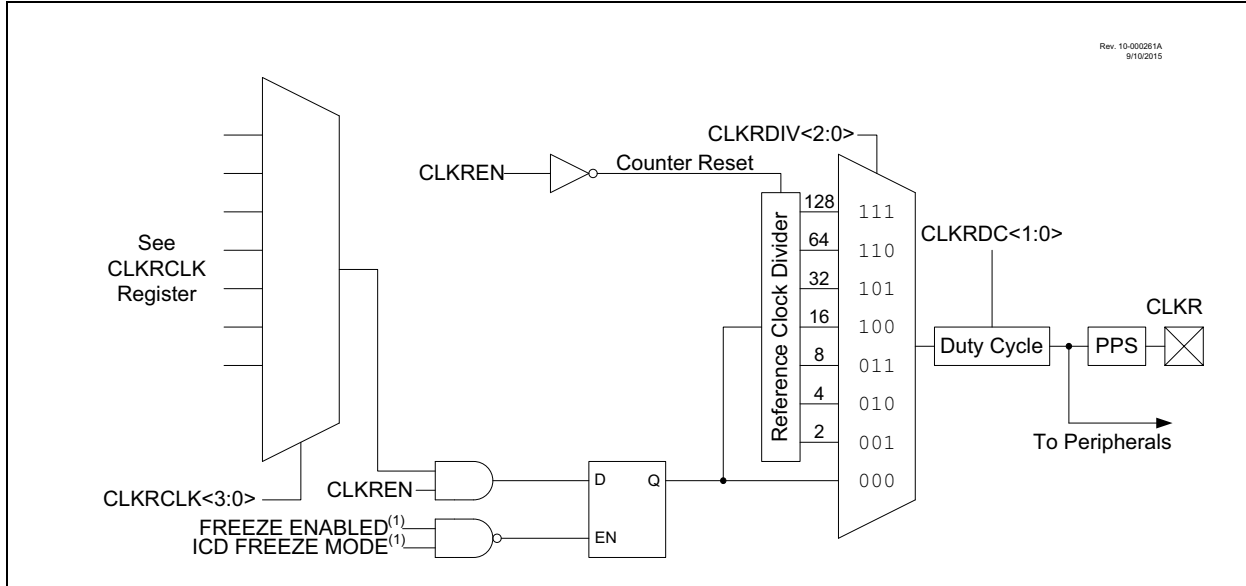
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Cleared by hardware S = User set

- bit 7      **GCEN:** General Call Enable bit (in I<sup>2</sup>C Slave mode only)  
 1 = Enable interrupt when a general call address (0x00 or 00h) is received in the SSPxSR  
 0 = General call address disabled
- bit 6      **ACKSTAT:** Acknowledge Status bit (in I<sup>2</sup>C mode only)  
 1 = Acknowledge was not received  
 0 = Acknowledge was received
- bit 5      **ACKDT:** Acknowledge Data bit (in I<sup>2</sup>C mode only)  
In Receive mode:  
 Value transmitted when the user initiates an Acknowledge sequence at the end of a receive  
 1 = Not Acknowledge  
 0 = Acknowledge
- bit 4      **ACKEN:** Acknowledge Sequence Enable bit (in I<sup>2</sup>C Master mode only)  
In Master Receive mode:  
 1 = Initiate Acknowledge sequence on SDA and SCL pins, and transmit ACKDT data bit.  
 Automatically cleared by hardware.  
 0 = Acknowledge sequence idle
- bit 3      **RCEN:** Receive Enable bit (in I<sup>2</sup>C Master mode only)  
 1 = Enables Receive mode for I<sup>2</sup>C  
 0 = Receive idle
- bit 2      **PEN:** Stop Condition Enable bit (in I<sup>2</sup>C Master mode only)  
SCKMSSP Release Control:  
 1 = Initiate Stop condition on SDA and SCL pins. Automatically cleared by hardware.  
 0 = Stop condition Idle
- bit 1      **RSEN:** Repeated Start Condition Enable bit (in I<sup>2</sup>C Master mode only)  
 1 = Initiate Repeated Start condition on SDA and SCL pins. Automatically cleared by hardware.  
 0 = Repeated Start condition Idle
- bit 0      **SEN:** Start Condition Enable/Stretch Enable bit  
In Master mode:  
 1 = Initiate Start condition on SDA and SCL pins. Automatically cleared by hardware.  
 0 = Start condition Idle  
In Slave mode:  
 1 = Clock stretching is enabled for both slave transmit and slave receive (stretch enabled)  
 0 = Clock stretching is disabled

**Note 1:** For bits ACKEN, RCEN, PEN, RSEN, SEN: If the I<sup>2</sup>C module is not in the IDLE mode, this bit may not be set (no spooling) and the SSPxBUF may not be written (or writes to the SSPxBUF are disabled).

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**FIGURE 34-1: CLOCK REFERENCE BLOCK DIAGRAM**



**FIGURE 34-2: CLOCK REFERENCE TIMING**

