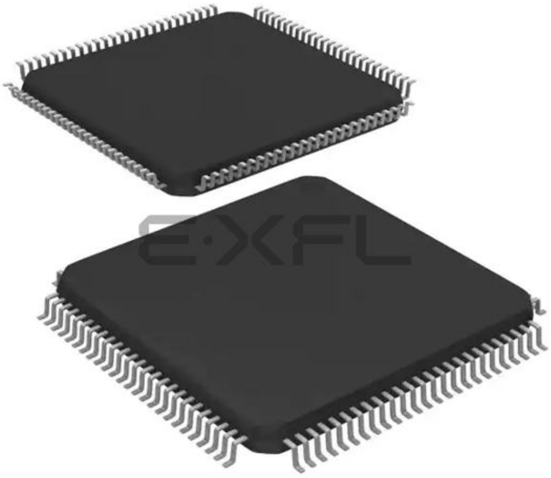

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32wg880f64-qfp100

2.1.19 Backup Real Time Counter (BURTC)

The Backup Real Time Counter (BURTC) contains a 32-bit counter and is clocked either by a 32.768 kHz crystal oscillator, a 32.768 kHz RC oscillator or a 1 kHz ULFRCO. The BURTC is available in all Energy Modes and it can also run in backup mode, making it operational even if the main power should drain out.

2.1.20 Low Energy Timer (LETIMER)

The unique LETIMER^{TM}, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

2.1.21 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 – EM3.

2.1.22 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.23 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.24 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 8 external pins and 6 internal signals.

2.1.25 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has two single ended output buffers which can be combined into one differential output. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

2.1.26 Operational Amplifier (OPAMP)

The EFM32WG880 features 3 Operational Amplifiers. The Operational Amplifier is a versatile general purpose amplifier with rail-to-rail differential input and rail-to-rail single ended output. The input can be set to pin, DAC or OPAMP, whereas the output can be pin, OPAMP or ADC. The current is programmable and the OPAMP has various internal configurations such as unity gain, programmable gain using internal resistors etc.

2.1.27 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface (LESENSE^{TM}), is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable FSM which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

2.1.28 Backup Power Domain

The backup power domain is a separate power domain containing a Backup Real Time Counter, BURTC, and a set of retention registers, available in all energy modes. This power domain can be configured to automatically change power source to a backup battery when the main power drains out. The backup power domain enables the EFM32WG880 to keep track of time and retain data, even if the main power source should drain out.

2.1.29 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

2.1.30 General Purpose Input/Output (GPIO)

In the EFM32WG880, there are 85 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

2.1.31 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x36 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

2.2 Configuration Summary

The features of the EFM32WG880 is a subset of the feature set described in the EFM32WG Reference Manual. Table 2.1 (p. 7) describes device specific implementation of the features.

Table 2.1. Configuration Summary

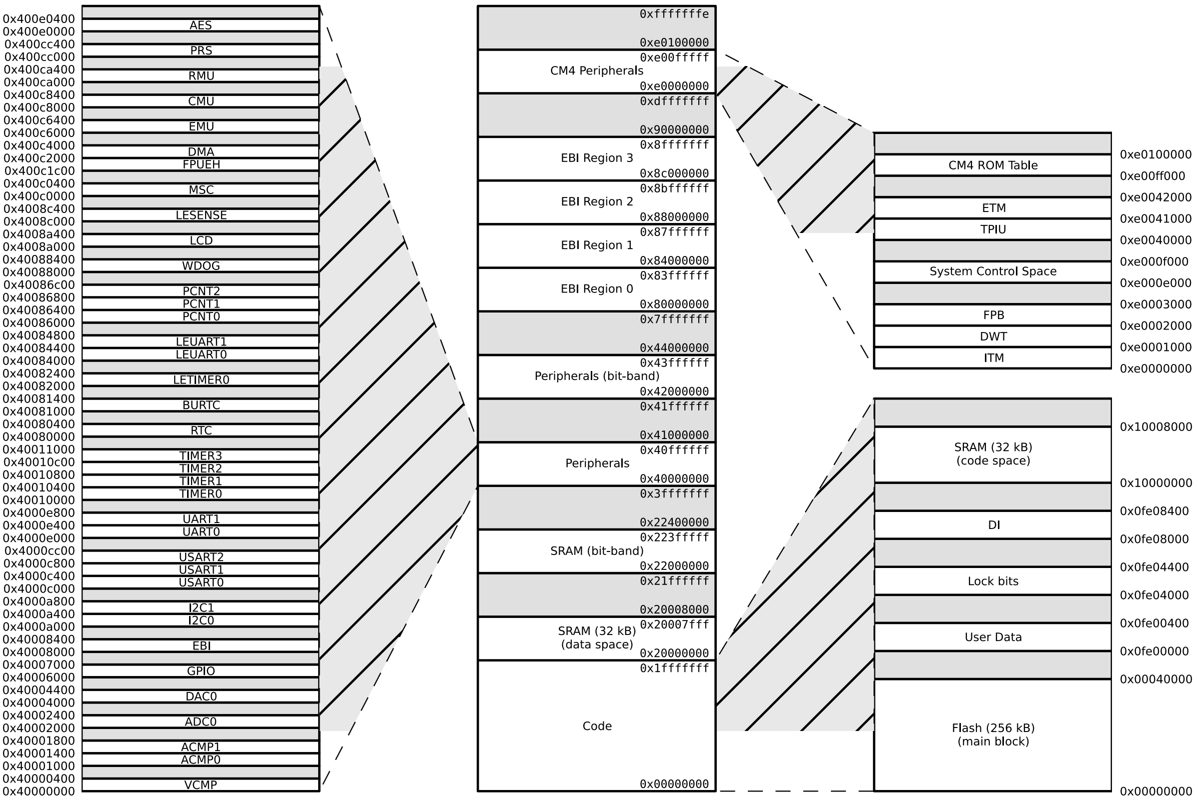
Module	Configuration	Pin Connections
Cortex-M4	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA

Module	Configuration	Pin Connections
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
EBI	Full configuration	EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
I2C1	Full configuration	I2C1_SDA, I2C1_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration with I2S	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
UART1	Full configuration	U1_TX, U1_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
TIMER3	Full configuration	TIM3_CC[2:0]
RTC	Full configuration	NA
BURTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	85 pins	Available pins are shown in Table 4.3 (p. 70)
LCD	Full configuration	LCD_SEG[35:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT

2.3 Memory Map

The *EFM32WG880* memory map is shown in Figure 2.2 (p. 9), with RAM and Flash sizes for the largest memory configuration.

Figure 2.2. EFM32WG880 Memory Map with largest RAM and Flash sizes



3.3.2 Environmental

Table 3.3. Environmental

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ESDHBM}	ESD (Human Body Model HBM)	T_{AMB}=25°C			2000	V
V_{ESDCDM}	ESD (Charged Device Model, CDM)	T_{AMB}=25°C			750	V

Latch-up sensitivity passed: ±100 mA/1.5 × V_{SUPPLY}(max) according to JEDEC JESD 78 method Class II, 85°C.

3.4 Current Consumption

Table 3.4. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{EM0}	EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz)	48 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		225	236	µA/MHz
		48 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		225		µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		226	238	µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		227		µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		228	240	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		229		µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		230	243	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		231		µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		232	245	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		233		µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25°C		238	250	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85°C		238		µA/MHz

Figure 3.5. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11MHz

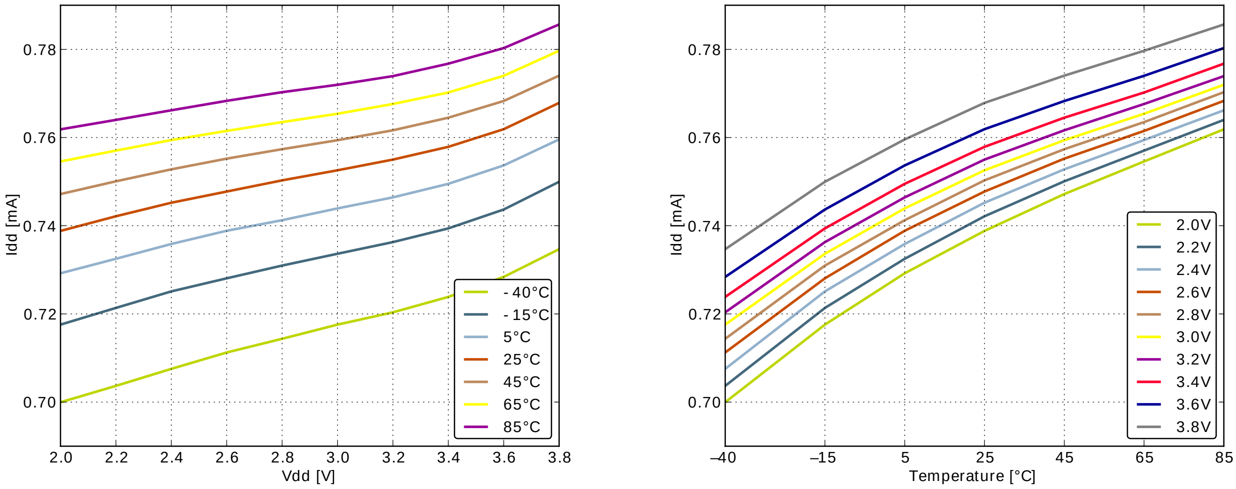


Figure 3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 6.6MHz

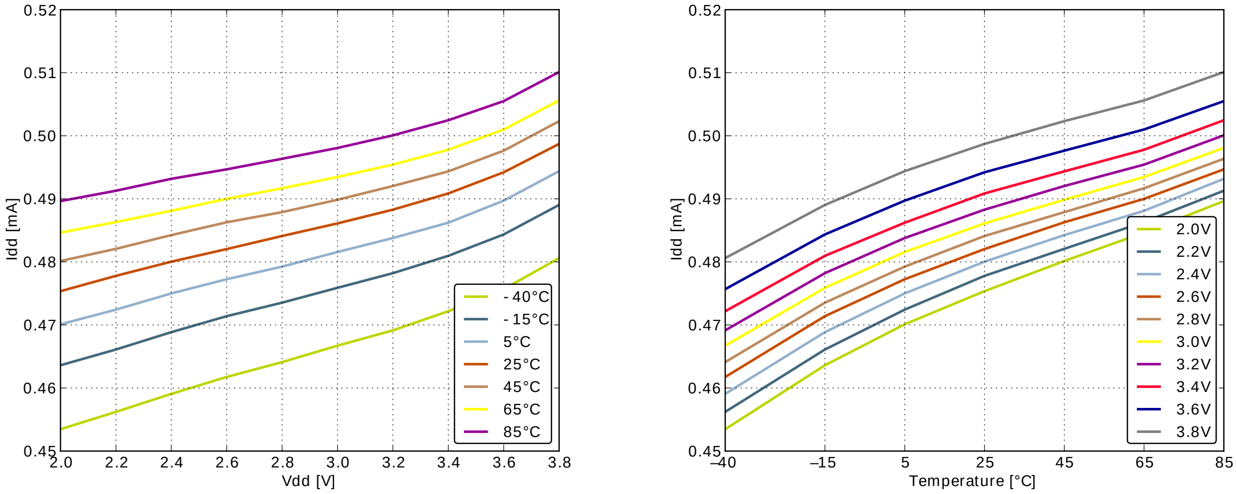
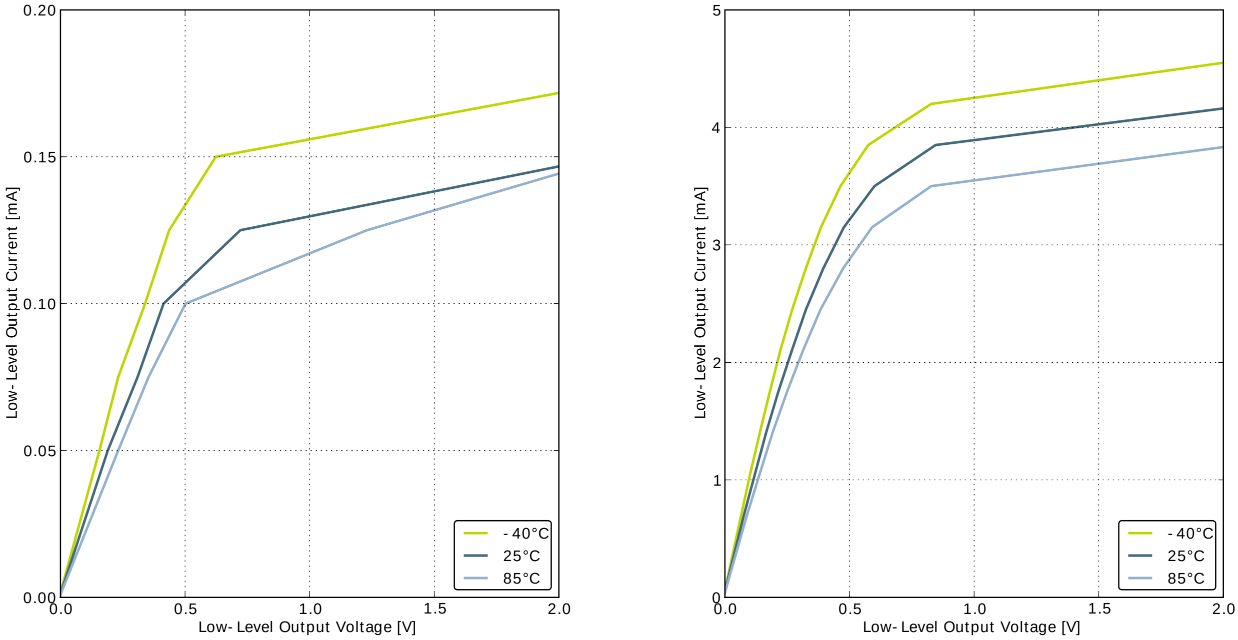
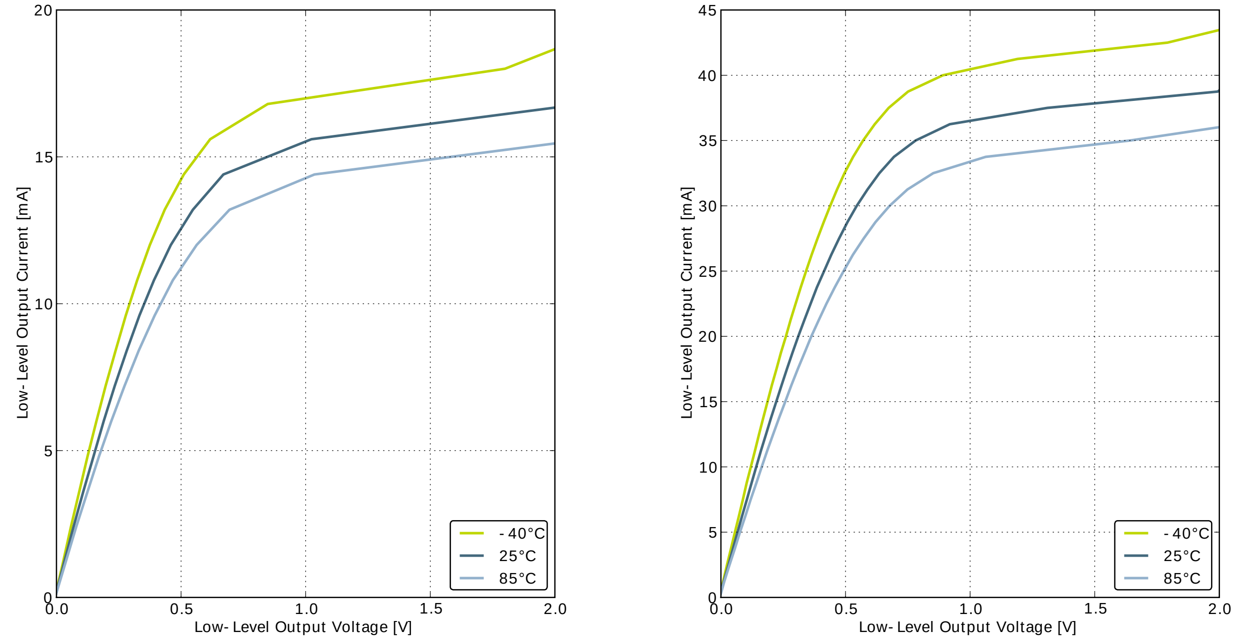


Figure 3.11. Typical Low-Level Output Current, 2V Supply Voltage



GPIO_Px_CTRL DRIVEMODE = LOWEST

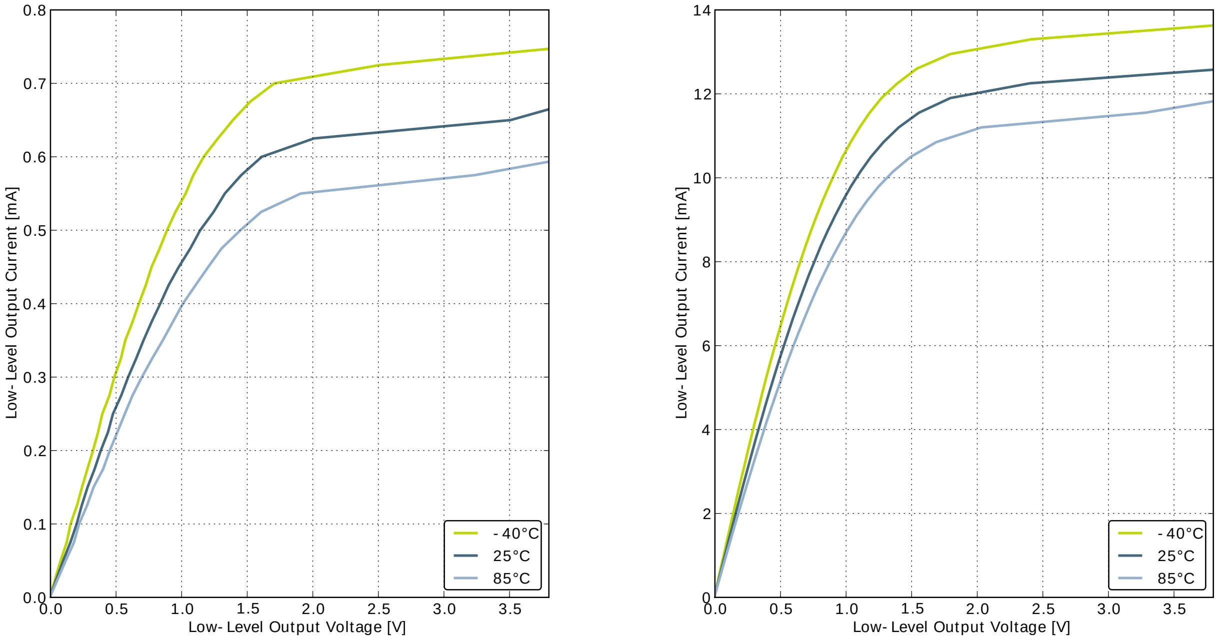
GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

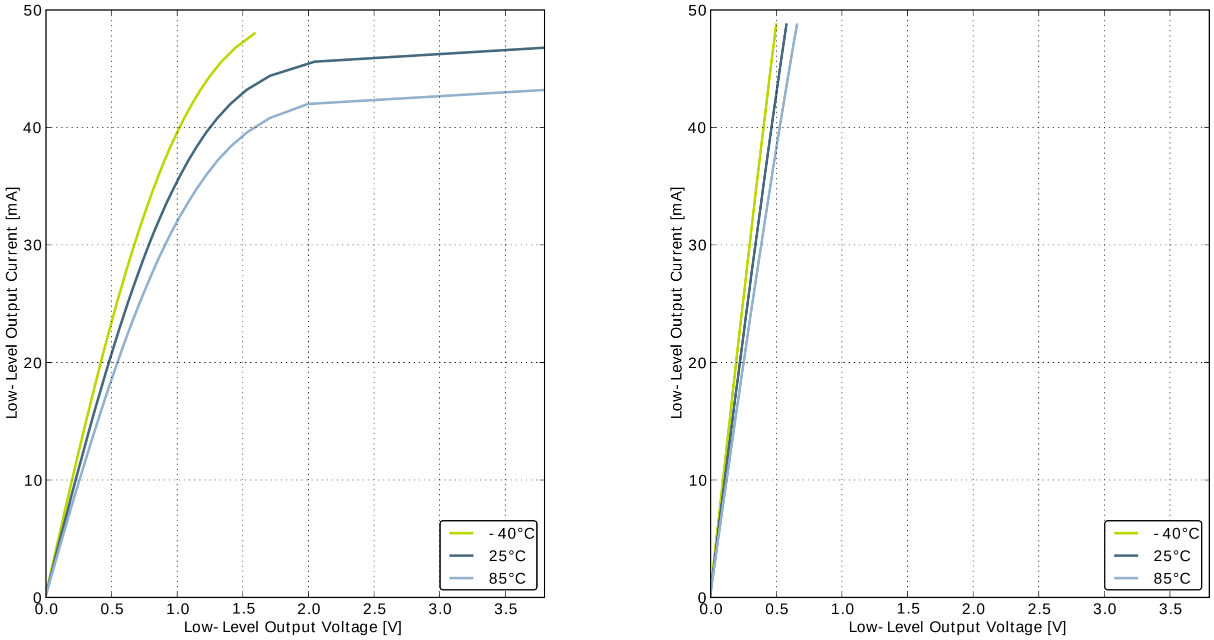
GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.15. Typical Low-Level Output Current, 3.8V Supply Voltage



GPIO_Px_CTRL DRIVEMODE = LOWEST

GPIO_Px_CTRL DRIVEMODE = LOW



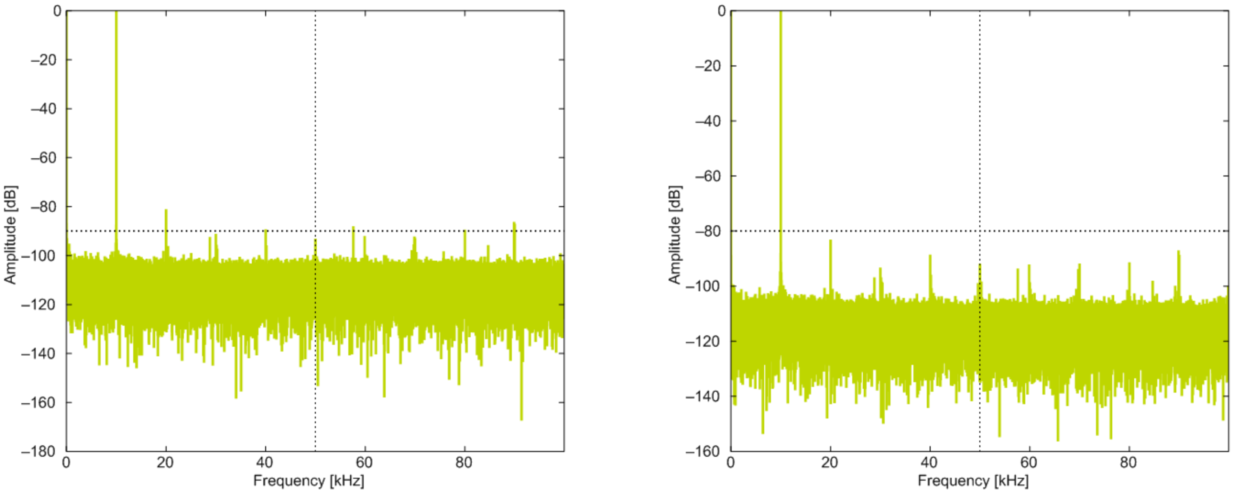
GPIO_Px_CTRL DRIVEMODE = STANDARD

GPIO_Px_CTRL DRIVEMODE = HIGH

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		68		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		66		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	62	66		dB
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference		69		dB
$SFDR_{ADC}$	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		73		dBc
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		77		dBc
		1 MSamples/s, 12 bit, differential, V_{DD} reference		76		dBc
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		75		dBc
		1 MSamples/s, 12 bit, differential, 5V reference		69		dBc
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		76		dBc

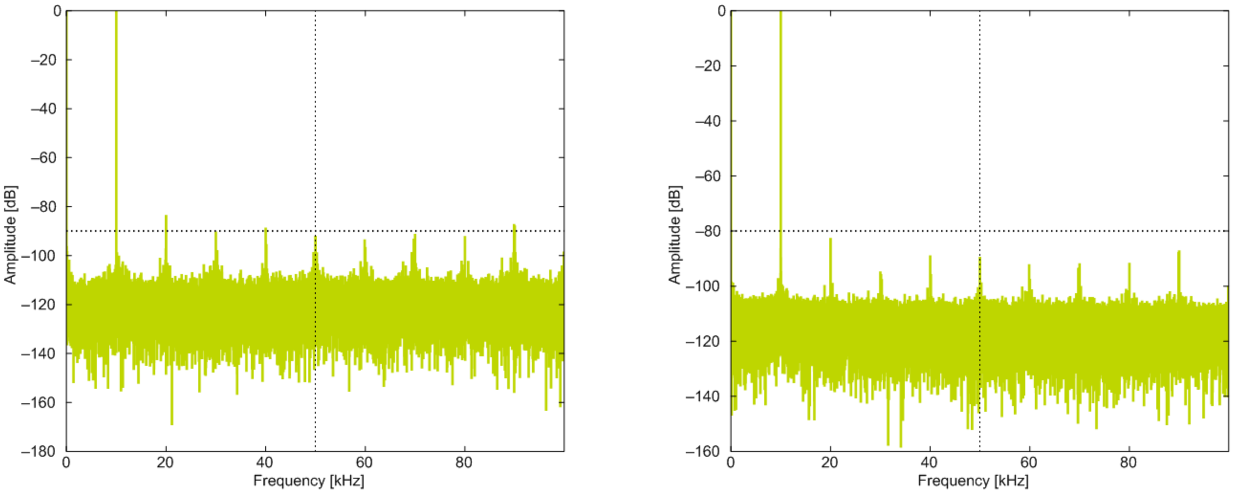
3.10.1 Typical performance

Figure 3.26. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°C



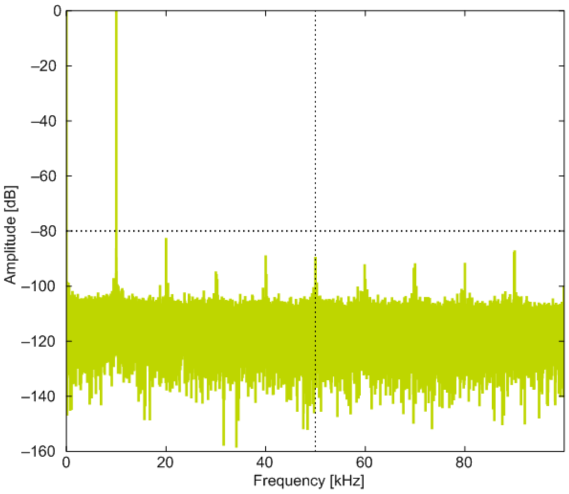
1.25V Reference

2.5V Reference



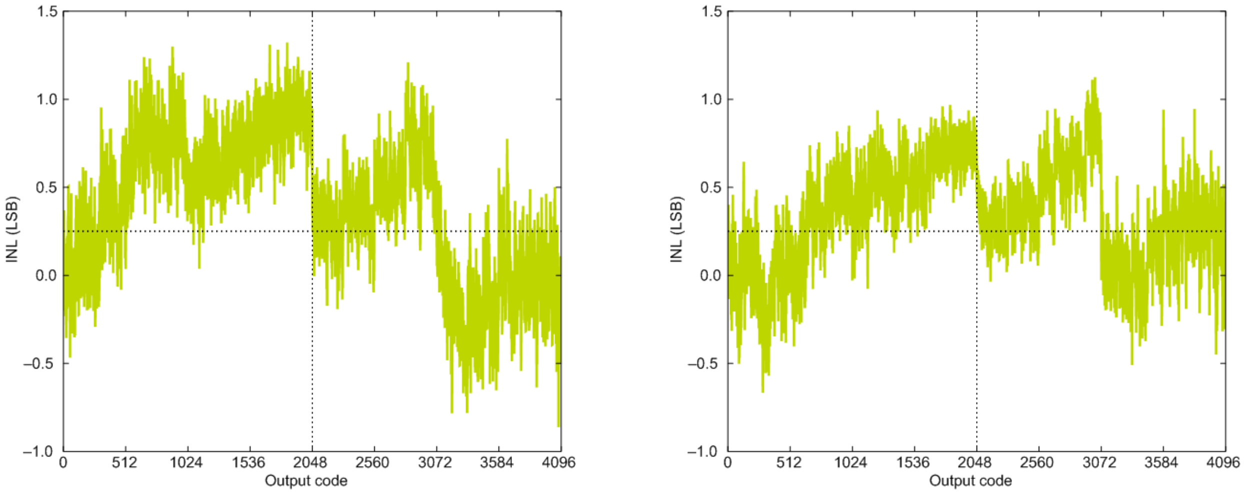
2XVDDVSS Reference

5VDIFF Reference



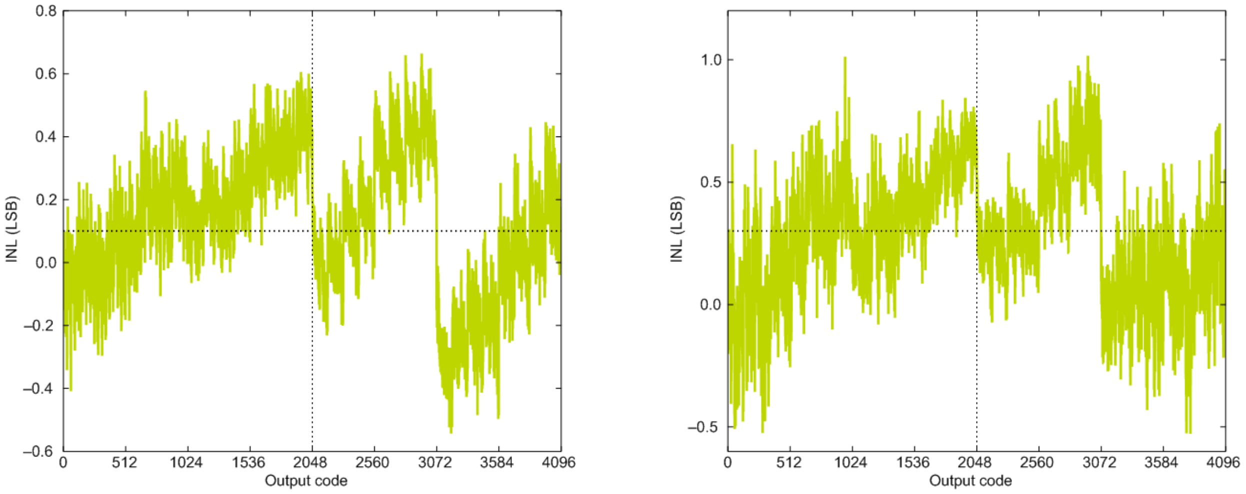
VDD Reference

Figure 3.27. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C



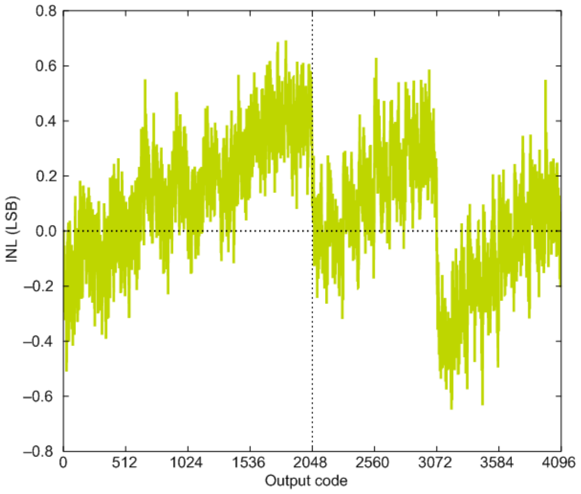
1.25V Reference

2.5V Reference



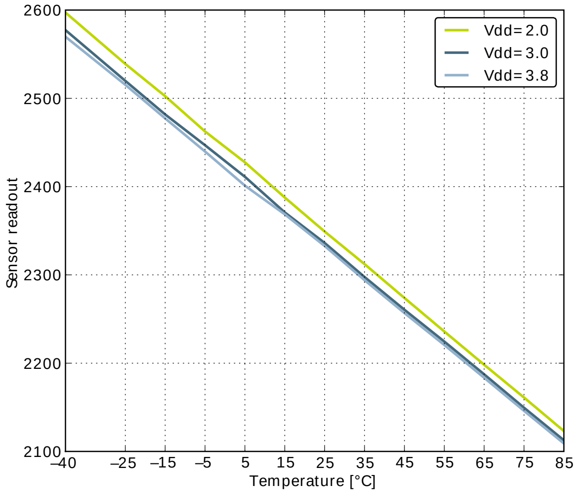
2XVDDVSS Reference

5VDIFF Reference



VDD Reference

Figure 3.31. ADC Temperature sensor readout



3.11 Digital Analog Converter (DAC)

Table 3.16. DAC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DACOUT}	Output voltage range	VDD voltage reference, single ended	0		V_{DD}	V
		VDD voltage reference, differential	$-V_{DD}$		V_{DD}	V
V_{DACCM}	Output common mode voltage range		0		V_{DD}	V
I_{DAC}	Active current including references for 2 channels	500 kSamples/s, 12 bit		400[1]		µA
		100 kSamples/s, 12 bit		200[1]		µA
		1 kSamples/s 12 bit NORMAL		17[1]		µA
SR_{DAC}	Sample rate				500	ksamples/s
f_{DAC}	DAC clock frequency	Continuous Mode			1000	kHz
		Sample/Hold Mode			250	kHz
		Sample/Off Mode			250	kHz
$CYC_{DACCONV}$	Clock cyckles per conversion			2		
$t_{DACCONV}$	Conversion time		2			µs
$t_{DACSETTLE}$	Settling time			5		µs
SNR_{DAC}	Signal to Noise Ratio (SNR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		59		dB
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		58		dB

Figure 3.40. EBI Read Enable Related Output Timing

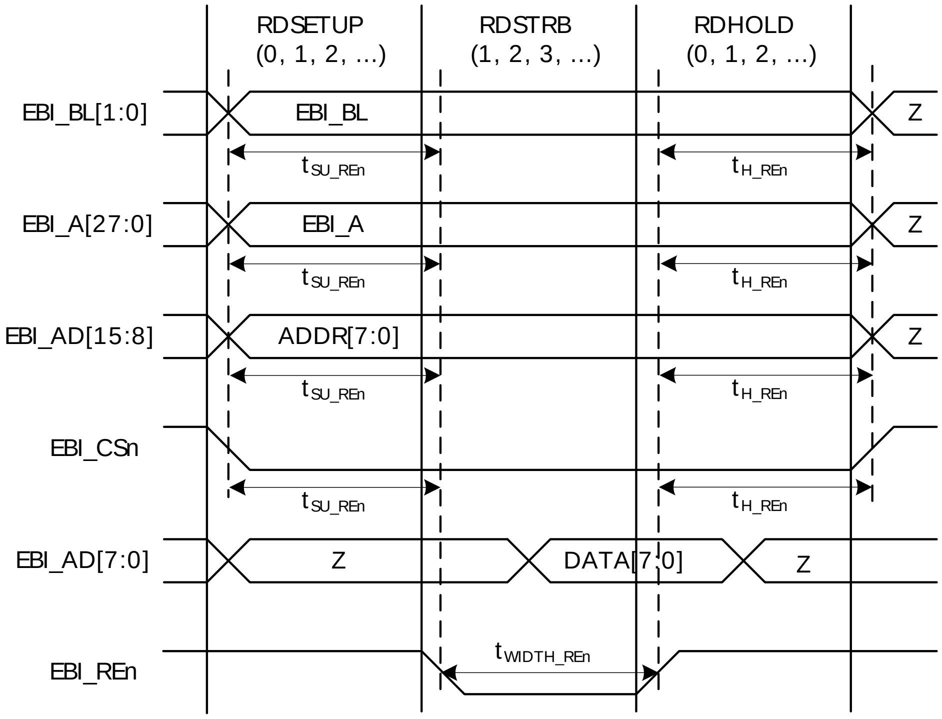


Table 3.22. EBI Read Enable Related Output Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{OH_REn} [1 2 3 4]	Output hold time, from trailing EBI_REn/ EBI_NANDREn edge to EBI_AD, EBI_A, EBI_CSn, EBI_BLn invalid	-10.00 + (RDHOLD * $t_{HFCORECLK}$)			ns
t_{OSU_REn} [1 2 3 4 5]	Output setup time, from EBI_AD, EBI_A, EBI_CSn, EBI_BLn valid to leading EBI_REn/EBI_NANDREn edge	-10.00 + (RDSETUP * $t_{HFCORECLK}$)			ns
t_{WIDTH_REn} [1 2 3 4 5 6]	EBI_REn pulse width	-9.00 + ((RDSTRB+1) * $t_{HFCORECLK}$)			ns

[1] Applies for all addressing modes (figure only shows D8A8. Output timing for EBI_AD only applies to multiplexed addressing modes D8A24ALE and D16A16ALE)

[2] Applies for both EBI_REn and EBI_NANDREn (figure only shows EBI_REn)

[3] Applies for all polarities (figure only shows active low signals)

[4] Measurement done at 10% and 90% of V_{DD} (figure shows 50% of $_{VDD}$)

[5] The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFRE=0. The leading edge of EBI_REn can be moved to the right by setting HALFRE=1. This decreases the length of t_{WIDTH_REn} and increases the length of t_{OSU_REn} by 1/2 * $t_{HFCLKNODIV}$.

[6] When page mode is used, RDSTRB is replaced by RDPA for page hits.

Table 3.30. SPI Master Timing with SSSEARLY and SMSDELAY

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{SCLK} [1] [2]	SCLK period		2 * $t_{HFPERCLK}$			ns
t_{CS_MO} [1] [2]	CS to MOSI		-2.00		2.00	ns
t_{SCLK_MO} [1] [2]	SCLK to MOSI		-1.00		3.00	ns
t_{SU_MI} [1] [2]	MISO setup time	IOVDD = 3.0 V	-32.00			ns
t_{H_MI} [1] [2]	MISO hold time		63.00			ns

[1] Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

[2] Measurement done at 10% and 90% of V_{DD} (figure shows 50% of $_{VDD}$)

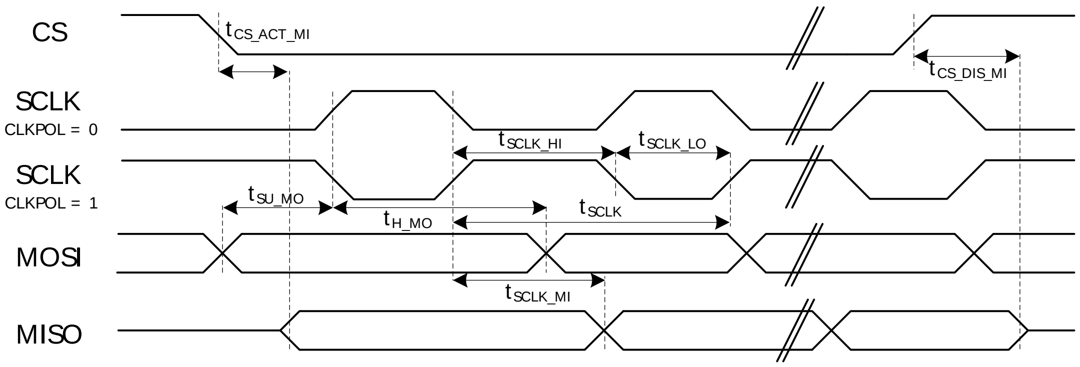


Figure 3.44. SPI Slave Timing

Table 3.31. SPI Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{SCLK_sl} [1] [2]	SCKL period	6 * $t_{HFPERCLK}$			ns
t_{SCLK_hi} [1] [2]	SCLK high period	3 * $t_{HFPERCLK}$			ns
t_{SCLK_lo} [1] [2]	SCLK low period	3 * $t_{HFPERCLK}$			ns
$t_{CS\_ACT\_MI}$ [1] [2]	CS active to MISO	5.00		35.00	ns
$t_{CS\_DIS\_MI}$ [1] [2]	CS disable to MISO	5.00		35.00	ns
t_{SU_MO} [1] [2]	MOSI setup time	5.00			ns
t_{H_MO} [1] [2]	MOSI hold time	2 + 2 * $t_{HFPERCLK}$			ns
t_{SCLK_MI} [1] [2]	SCLK to MISO	7 + $t_{HFPERCLK}$		42 + 2 * $t_{HFPERCLK}$	ns

[1] Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

[2] Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

Table 3.32. SPI Slave Timing with SSSEARLY and SMSDELAY

Symbol	Parameter	Min	Typ	Max	Unit
t_{SCLK_sl} [1] [2]	SCKL period	6 * $t_{HFPERCLK}$			ns

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
60	PE0		EBI_A07 #0/1/2	TIM3_CC0 #1 PCNT0_S0IN #1	U0_TX #1 I2C1_SDA #2	
61	PE1		EBI_A08 #0/1/2	TIM3_CC1 #1 PCNT0_S1IN #1	U0_RX #1 I2C1_SCL #2	
62	PE2	BU_VOUT	EBI_A09 #0	TIM3_CC2 #1	U1_TX #3	ACMP0_O #1
63	PE3	BU_STAT	EBI_A10 #0		U1_RX #3	ACMP1_O #1
64	PE4	LCD_COM0	EBI_A11 #0/1/2		US0_CS #1	
65	PE5	LCD_COM1	EBI_A12 #0/1/2		US0_CLK #1	
66	PE6	LCD_COM2	EBI_A13 #0/1/2		US0_RX #1	
67	PE7	LCD_COM3	EBI_A14 #0/1/2		US0_TX #1	
68	PC8	ACMP1_CH0	EBI_A15 #0/1/2	TIM2_CC0 #2	US0_CS #2	LES_CH8 #0
69	PC9	ACMP1_CH1	EBI_A09 #1/2	TIM2_CC1 #2	US0_CLK #2	LES_CH9 #0 GPIO_EM4WU2
70	PC10	ACMP1_CH2	EBI_A10 #1/2	TIM2_CC2 #2	US0_RX #2	LES_CH10 #0
71	PC11	ACMP1_CH3	EBI_ALE #1/2		US0_TX #2	LES_CH11 #0
72	PC12	ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT			U1_TX #0	CMU_CLK0 #1 LES_CH12 #0
73	PC13	ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT		TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0	U1_RX #0	LES_CH13 #0
74	PC14	ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3 U0_TX #3	LES_CH14 #0
75	PC15	ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT		TIM0_CDTI2 #1/3 TIM1_CC2 #0	US0_CLK #3 U0_RX #3	LES_CH15 #0 DBG_SWO #1
76	PF0			TIM0_CC0 #5 LETIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1/2/3
77	PF1			TIM0_CC1 #5 LETIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
78	PF2	LCD_SEG0	EBI_ARDY #0/1/2	TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4
79	PF3	LCD_SEG1	EBI_ALE #0	TIM0_CDTI0 #2/5		PRS_CH0 #1 ETM_TD3 #1
80	PF4	LCD_SEG2	EBI_WEn #0/2	TIM0_CDTI1 #2/5		PRS_CH1 #1
81	PF5	LCD_SEG3	EBI_REn #0/2	TIM0_CDTI2 #2/5		PRS_CH2 #1
82	IOVDD_5	Digital IO power supply 5.				
83	VSS	Ground				
84	PF6	LCD_SEG24	EBI_BL0 #0/1/2	TIM0_CC0 #2	U0_TX #0	
85	PF7	LCD_SEG25	EBI_BL1 #0/1/2	TIM0_CC1 #2	U0_RX #0	
86	PF8	LCD_SEG26	EBI_WEn #1	TIM0_CC2 #2		ETM_TCLK #1
87	PF9	LCD_SEG27	EBI_REn #1			ETM_TD0 #1
88	PD9	LCD_SEG28	EBI_CS0 #0/1/2			
89	PD10	LCD_SEG29	EBI_CS1 #0/1/2			

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
90	PD11	LCD_SEG30	EBI_CS2 #0/1/2			
91	PD12	LCD_SEG31	EBI_CS3 #0/1/2			
92	PE8	LCD_SEG4	EBI_AD00 #0/1/2	PCNT2_S0IN #1		PRS_CH3 #1
93	PE9	LCD_SEG5	EBI_AD01 #0/1/2	PCNT2_S1IN #1		
94	PE10	LCD_SEG6	EBI_AD02 #0/1/2	TIM1_CC0 #1	US0_TX #0	BOOT_TX
95	PE11	LCD_SEG7	EBI_AD03 #0/1/2	TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
96	PE12	LCD_SEG8	EBI_AD04 #0/1/2	TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
97	PE13	LCD_SEG9	EBI_AD05 #0/1/2		US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5
98	PE14	LCD_SEG10	EBI_AD06 #0/1/2	TIM3_CC0 #0	LEU0_TX #2	
99	PE15	LCD_SEG11	EBI_AD07 #0/1/2	TIM3_CC1 #0	LEU0_RX #2	
100	PA15	LCD_SEG12	EBI_AD08 #0/1/2	TIM3_CC2 #0		

4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 62). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 4.2. Alternate functionality overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2							Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3							Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5							Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6							Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7							Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2	PD6					Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8							Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9							Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10							Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11							Analog comparator ACMP1, channel 3.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LCD_SEG15	PA2							LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG16	PA3							LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG17	PA4							LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG18	PA5							LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG19	PA6							LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG20/ LCD_COM4	PB3							LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4
LCD_SEG21/ LCD_COM5	PB4							LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5
LCD_SEG22/ LCD_COM6	PB5							LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6
LCD_SEG23/ LCD_COM7	PB6							LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7
LCD_SEG24	PF6							LCD segment line 24. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG25	PF7							LCD segment line 25. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG26	PF8							LCD segment line 26. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG27	PF9							LCD segment line 27. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG28	PD9							LCD segment line 28. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG29	PD10							LCD segment line 29. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG30	PD11							LCD segment line 30. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG31	PD12							LCD segment line 31. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG32	PB0							LCD segment line 32. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG33	PB1							LCD segment line 33. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG34	PB2							LCD segment line 34. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG35	PA7							LCD segment line 35. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG36	PA8							LCD segment line 36. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG37	PA9							LCD segment line 37. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG38	PA10							LCD segment line 38. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG39	PA11							LCD segment line 39. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LES_ALTEX0	PD6							LESENSE alternate exite output 0.
LES_ALTEX1	PD7							LESENSE alternate exite output 1.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LES_ALTEX2	PA3							LESENSE alternate exite output 2.
LES_ALTEX3	PA4							LESENSE alternate exite output 3.
LES_ALTEX4	PA5							LESENSE alternate exite output 4.
LES_ALTEX5	PE11							LESENSE alternate exite output 5.
LES_ALTEX6	PE12							LESENSE alternate exite output 6.
LES_ALTEX7	PE13							LESENSE alternate exite output 7.
LES_CH0	PC0							LESENSE channel 0.
LES_CH1	PC1							LESENSE channel 1.
LES_CH2	PC2							LESENSE channel 2.
LES_CH3	PC3							LESENSE channel 3.
LES_CH4	PC4							LESENSE channel 4.
LES_CH5	PC5							LESENSE channel 5.
LES_CH6	PC6							LESENSE channel 6.
LES_CH7	PC7							LESENSE channel 7.
LES_CH8	PC8							LESENSE channel 8.
LES_CH9	PC9							LESENSE channel 9.
LES_CH10	PC10							LESENSE channel 10.
LES_CH11	PC11							LESENSE channel 11.
LES_CH12	PC12							LESENSE channel 12.
LES_CH13	PC13							LESENSE channel 13.
LES_CH14	PC14							LESENSE channel 14.
LES_CH15	PC15							LESENSE channel 15.
LETIM0_OUT0	PD6	PB11	PF0	PC4				Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5				Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15	PF1	PA0			LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14	PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6						LEUART1 Receive input.
LEU1_TX	PC6	PA5						LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13	PE0	PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14	PE1	PC1	PD7				Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3						Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4						Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8						Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9						Pulse Counter PCNT2 input number 1.
PRS_CH0	PA0	PF3						Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1	PF4						Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0	PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1	PE8						Peripheral Reflex System PRS, channel 3.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
								USART2 Synchronous mode Master Output / Slave Input (MOSI).

4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32WG880* is shown in Table 4.3 (p. 70). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port in indicated by a number from 15 down to 0.

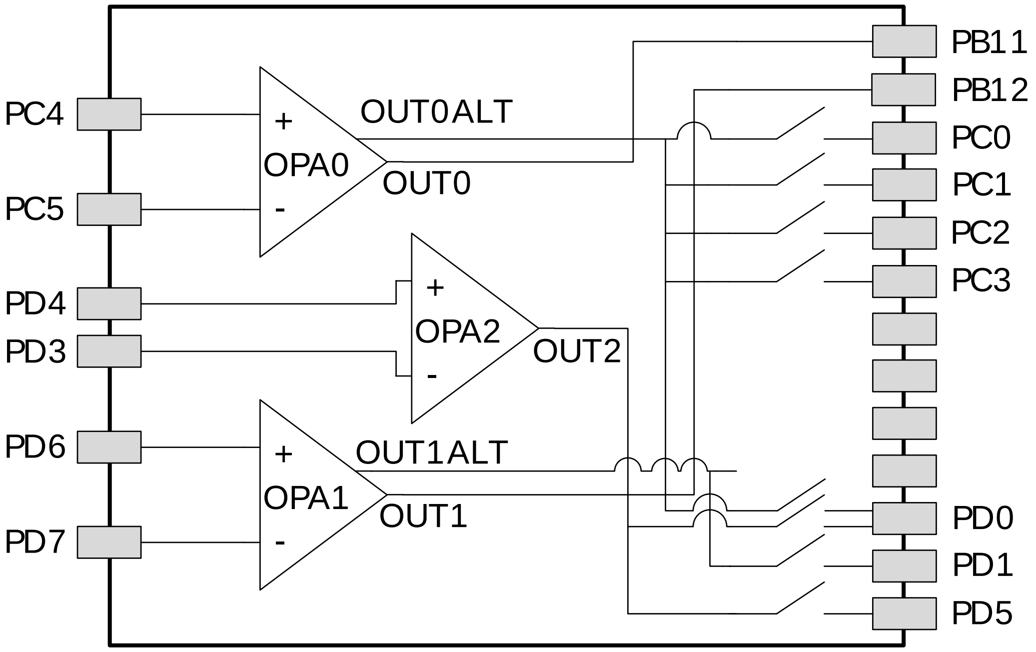
Table 4.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	-	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	-	-	-	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	-	-	-	-	-	-	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

4.4 Opamp Pinout Overview

The specific opamp terminals available in *EFM32WG880* is shown in Figure 4.2 (p. 70) .

Figure 4.2. Opamp Pinout



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