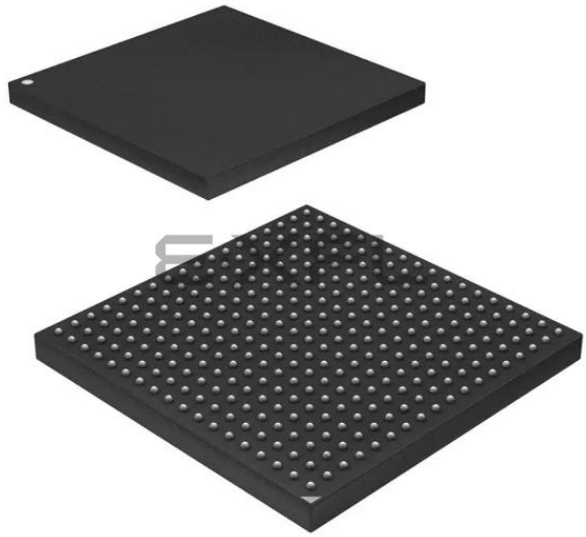

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM926EJ-S |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 400MHz |
| Co-Processors/DSP | - |
| RAM Controllers | LPDDR, LPSDR, DDR2, SDR, SRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | LCD, Touchscreen |
| Ethernet | 10/100Mbps |
| SATA | - |
| USB | USB 2.0 (3) |
| Voltage - I/O | 1.8V, 3.3V |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Security Features | - |
| Package / Case | 324-TFBGA |
| Supplier Device Package | 324-TFBGA (15x15) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/at91sam9g45b-cu |

# 1. Features

- 400 MHz ARM926EJ-S™ ARM® Thumb® Processor
  - 32 Kbytes Data Cache, 32 Kbytes Instruction Cache, MMU
- Memories
  - DDR2 Controller 4-bank DDR2/LPDDR, SDRAM/LPSDR
  - External Bus Interface supporting 4-bank DDR2/LPDDR, SDRAM/LPSDR, Static Memories, CompactFlash, SLC NAND Flash with ECC
  - One 64-Kbyte internal SRAM, single-cycle access at system speed or processor speed through TCM interface
  - One 64-Kbyte internal ROM, embedding bootstrap routine
- Peripherals
  - LCD Controller supporting STN and TFT displays up to 1280*860
  - ITU-R BT. 601/656 Image Sensor Interface
  - USB Device High Speed, USB Host High Speed and USB Host Full Speed with On-Chip Transceiver
  - 10/100 Mbps Ethernet MAC Controller
  - Two High Speed Memory Card Hosts (SDIO, SDCard, MMC)
  - AC'97 controller
  - Two Master/Slave Serial Peripheral Interfaces
  - Two Three-channel 16-bit Timer/Counters
  - Two Synchronous Serial Controllers (I2S mode)
  - Four-channel 16-bit PWM Controller
  - Two Two-wire Interfaces
  - Four USARTs with ISO7816, IrDA, Manchester and SPI modes
  - 8-channel 10-bit ADC with 4-wire Touch Screen support
  - Write Protected Registers
- System
  - 133 MHz twelve 32-bit layer AHB Bus Matrix
  - 37 DMA Channels
  - Boot from NAND Flash, SDCard, DataFlash® or serial DataFlash
  - Reset Controller with on-chip Power-on Reset
  - Selectable 32768 Hz Low-power and 12 MHz Crystal Oscillators
  - Internal Low-power 32 kHz RC Oscillator
  - One PLL for the system and one 480 MHz PLL optimized for USB High Speed
  - Two Programmable External Clock Signals
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer, Real Time Timer and Real Time Clock
- I/O
  - Five 32-bit Parallel Input/Output Controllers
  - 160 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os with Schmitt trigger input
- Package
  - 324-ball TFBGA, pitch 0.8 mm

## 4.2 324-ball TFBGA Package Pinout

**Table 4-1. SAM9G45 Pinout for 324-ball BGA Package**

| Pin | Signal Name |
|---|---|
| A1 | PC27 |
| A2 | PC28 |
| A3 | PC25 |
| A4 | PC20 |
| A5 | PC12 |
| A6 | PC7 |
| A7 | PC5 |
| A8 | PC0 |
| A9 | NWR3/NBS3 |
| A10 | NCS0 |
| A11 | DQS0 |
| A12 | RAS |
| A13 | SDCK |
| A14 | NSDCK |
| A15 | D7 |
| A16 | DDR_VREF |
| A17 | D0 |
| A18 | A14 |
| B1 | PC31 |
| B2 | PC29 |
| B3 | PC30 |
| B4 | PC22 |
| B5 | PC17 |
| B6 | PC10 |
| B7 | PC11 |
| B8 | PC2 |
| B9 | SDA10 |
| B10 | A17/BA1 |
| B11 | DQM0 |
| B12 | SDCKE |
| B13 | D12 |
| B14 | D8 |
| B15 | D4 |
| B16 | D3 |
| B17 | A15 |
| B18 | A13 |
| C1 | XIN32 |
| C2 | GNDANA |
| C3 | WKUP |
| C4 | PC26 |
| C5 | PC21 |
| C6 | PC15 |
| C7 | PC9 |
| C8 | PC3 |
| C9 | NWR0/NWE |
| C10 | A16/BA0 |
| C11 | CAS |
| C12 | D15 |
| C13 | D10 |
| C14 | D6 |
| E10 | NANDWE |
| E11 | DQS1 |
| E12 | D13 |
| E13 | D11 |
| E14 | A4 |
| E15 | A8 |
| E16 | A9 |
| E17 | A7 |
| E18 | VDDCORE |
| F1 | PD22 |
| F2 | PD24 |
| F3 | SHDN |
| F4 | PE1 |
| F5 | PE3 |
| F6 | VDDIOM1 |
| F7 | PC19 |
| F8 | PC14 |
| F9 | PC4 |
| F10 | NCS1/SDCS |
| F11 | NRD |
| F12 | SDWE |
| F13 | A0/NBS0 |
| F14 | A1/NBS2/NWR2 |
| F15 | A3 |
| F16 | A6 |
| F17 | A5 |
| F18 | A2 |
| G1 | PD25 |
| G2 | PD23 |
| G3 | PE6 |
| G4 | PE0 |
| G5 | PE2 |
| G6 | PE8 |
| G7 | PE4 |
| G8 | PE11 |
| G9 | GNDCORE |
| G10 | VDDIOM1 |
| G11 | VDDIOM1 |
| G12 | VDDCORE |
| G13 | VDDCORE |
| G14 | DDR_DQM0 |
| G15 | DDR_DQS1 |
| G16 | DDR_BA1 |
| G17 | DDR_BA0 |
| G18 | DDR_DQS0 |
| H1 | PD26 |
| H2 | PD27 |
| H3 | VDDIOP1 |
| H4 | PE13 |
| H5 | PE5 |
| K1 | PE21 |
| K2 | PE23 |
| K3 | PE26 |
| K4 | PE22 |
| K5 | PE24 |
| K6 | PE25 |
| K7 | PE27 |
| K8 | PE28 |
| K9 | VDDIOP0 |
| K10 | VDDIOP0 |
| K11 | GNDIOM |
| K12 | GNDIOM |
| K13 | VDDIOM0 |
| K14 | DDR_A7 |
| K15 | DDR_A8 |
| K16 | DDR_A9 |
| K17 | DDR_A11 |
| K18 | DDR_A10 |
| L1 | PA0 |
| L2 | PE30 |
| L3 | PE29 |
| L4 | PE31 |
| L5 | PA2 |
| L6 | PA4 |
| L7 | PA8 |
| L8 | PD2 |
| L9 | PD13 |
| L10 | PD29 |
| L11 | PD31 |
| L12 | VDDIOM0 |
| L13 | VDDIOM0 |
| L14 | DDR_A1 |
| L15 | DDR_A3 |
| L16 | DDR_A4 |
| L17 | DDR_A6 |
| L18 | DDR_A5 |
| M1 | PA1 |
| M2 | PA5 |
| M3 | PA6 |
| M4 | PA7 |
| M5 | PA10 |
| M6 | PA14 |
| M7 | PB14 |
| M8 | PD4 |
| M9 | PD15 |
| M10 | NRST |
| M11 | PB11 |
| M12 | PB25 |
| M13 | PB27 |
| M14 | VDDIOM0 |
| P10 | TMS |
| P11 | VDDPLLA |
| P12 | PB20 |
| P13 | PB31 |
| P14 | DDR_D7 |
| P15 | DDR_D3 |
| P16 | DDR_D4 |
| P17 | DDR_D5 |
| P18 | DDR_D10 |
| R1 | PA18 |
| R2 | PA20 |
| R3 | PA24 |
| R4 | PA30 |
| R5 | PB4 |
| R6 | PB13 |
| R7 | PD0 |
| R8 | PD9 |
| R9 | PD18 |
| R10 | TDI |
| R11 | RTCK |
| R12 | PB22 |
| R13 | PB29 |
| R14 | DDR_D6 |
| R15 | DDR_D1 |
| R16 | DDR_D0 |
| R17 | HHSDMA |
| R18 | HFSDMA |
| T1 | PA22 |
| T2 | PA25 |
| T3 | PA26 |
| T4 | PB0 |
| T5 | PB6 |
| T6 | PB16 |
| T7 | PD1 |
| T8 | PD11 |
| T9 | PD19 |
| T10 | PD30 |
| T11 | BMS |
| T12 | PB8 |
| T13 | PB30 |
| T14 | DDR_D2 |
| T15 | PB21 |
| T16 | PB23 |
| T17 | HHSDPA |
| T18 | HFSDPA |
| U1 | PA27 |
| U2 | PA29 |
| U3 | PA28 |
| U4 | PB3 |
| U5 | PB7 |

# 6. Processor and Architecture

## 6.1 ARM926EJ-S Processor

- RISC Processor Based on ARM v5TEJ Architecture with Jazelle technology for Java acceleration
- Two Instruction Sets
  - ARM High-performance 32-bit Instruction Set
  - Thumb High Code Density 16-bit Instruction Set
- DSP Instruction Extensions
- 5-Stage Pipeline Architecture:
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)
  - Data Memory (M)
  - Register Write (W)
- 32-KByte Data Cache, 32-KByte Instruction Cache
  - Virtually-addressed 4-way Associative Cache
  - Eight words per line
  - Write-through and Write-back Operation
  - Pseudo-random or Round-robin Replacement
- Write Buffer
  - Main Write Buffer with 16-word Data Buffer and 4-address Buffer
  - DCache Write-back Buffer with 8-word Entries and a Single Address Entry
  - Software Control Drain
- Standard ARM v4 and v5 Memory Management Unit (MMU)
  - Access Permission for Sections
  - Access Permission for large pages and small pages can be specified separately for each quarter of the page
  - 16 embedded domains
- Bus Interface Unit (BIU)
  - Arbitrates and Schedules AHB Requests
  - Separate Masters for both instruction and data access providing complete Matrix system flexibility
  - Separate Address and Data Buses for both the 32-bit instruction interface and the 32-bit data interface
  - On Address and Data Buses, data can be 8-bit (Bytes), 16-bit (Half-words) or 32-bit (Words)
- TCM Interface

## 6.2 Bus Matrix

- 12-layer Matrix, handling requests from 11 masters
- Programmable Arbitration strategy
  - Fixed-priority Arbitration
  - Round-Robin Arbitration, either with no default master, last accessed default master or fixed default master
- Burst Management
  - Breaking with Slot Cycle Limit Support
  - Undefined Burst Length Support
- One Address Decoder provided per Master
  - Three different slaves may be assigned to each decoded memory area: one for internal ROM boot, one for internal flash boot, one after remap
- Boot Mode Select
  - Non-volatile Boot Memory can be internal ROM or external memory on EBI_NCS0
  - Selection is made by General purpose NVM bit sampled at reset
- Remap Command
  - Allows Remapping of an Internal SRAM in Place of the Boot Non-Volatile Memory (ROM or External Flash)
  - Allows Handling of Dynamic Exception Vectors

### 6.2.1 Matrix Masters

The Bus Matrix of the SAM9G45 manages Masters, thus each master can perform an access concurrently with others, depending on whether the slave it accesses is available.

Each Master has its own decoder, which can be defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

**Table 6-1. List of Bus Matrix Masters**

| | |
|---|---|
| Master 0 | ARM926™ Instruction |
| Master 1 | ARM926 Data |
| Master 2 | Peripheral DMA Controller (PDC) |
| Master 3 | USB HOST OHCI |
| Master 4 | DMA |
| Master 5 | DMA |
| Master 6 | ISI Controller DMA |
| Master 7 | LCD DMA |
| Master 8 | Ethernet MAC DMA |
| Master 9 | USB Device High Speed DMA |
| Master 10 | USB Host High Speed EHCI DMA |

**Figure 6-1. DDR Multi-port**

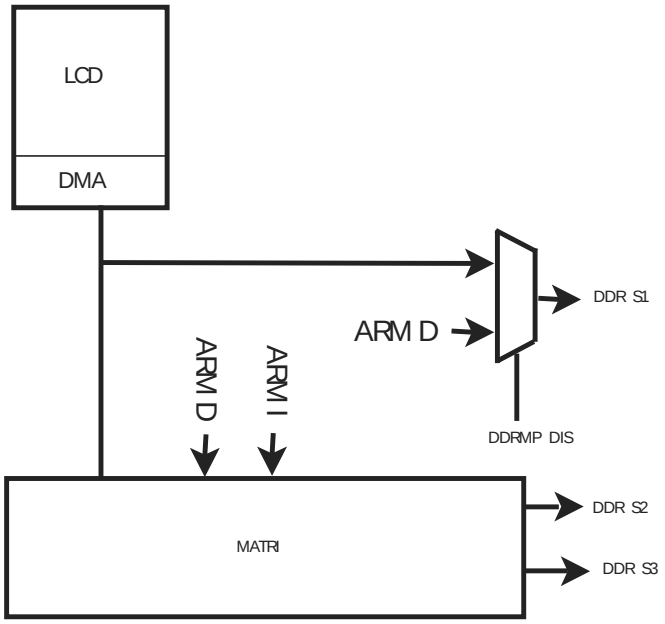



**Table 6-3. SAM9G45 Masters to Slaves Access DDRMP_DIS = 0**

| Master | | 0 | 1 | 2 | 3 | 4 & 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Slave | | ARM 926 Instr. | ARM 926 Data | PDC | USB Host OHCI | DMA | ISI DMA | LCD DMA | Ethernet MAC | USB Device HS | USB Host EHCI | Reserved |
| 0 | Internal SRAM 0 | X | X | X | X | X | X | - | X | X | X | - |
| 1 | Internal ROM | X | X | X | - | - | - | - | - | X | - | - |
| | UHP OHCI | X | X | - | - | - | - | - | - | - | - | - |
| | UHP EHCI | X | X | - | - | - | - | - | - | - | - | - |
| | LCD User Int. | X | X | - | - | - | - | - | - | - | - | - |
| | UDPHS RAM | X | X | - | - | - | - | - | - | - | - | - |
| | Reserved | X | X | - | - | - | - | - | - | - | - | - |
| 2 | DDR Port 0 | X | - | - | - | - | - | - | - | - | - | - |
| 3 | DDR Port 1 | - | X | - | - | - | - | - | - | - | - | - |
| 4 | DDR Port 2 | - | - | X | X | X | X | - | X | X | X | X |
| 5 | DDR Port 3 | - | - | X | X | X | X | X | X | X | X | - |
| 6 | EBI | X | X | X | X | X | X | X | X | X | X | X |
| 7 | Internal Periph. | X | X | X | - | X | - | - | - | - | - | - |

**Table 6-4. SAM9G45 Masters to Slaves Access with DDRMP_DIS = 1 (default)**

| Master | | 0 | 1 | 2 | 3 | 4 & 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Slave | | ARM 926 Instr. | ARM 926 Data | PDC | USB HOST OHCI | DMA | ISI DMA | LCD DMA | Ethernet MAC | USB Device HS | USB Host EHCI | Reserved |
| 0 | Internal SRAM 0 | X | X | X | X | X | X | - | X | X | X | - |
| 1 | Internal ROM | X | X | X | - | - | - | - | - | X | - | - |
| | UHP OHCI | X | X | - | - | - | - | - | - | - | - | - |
| | UHP EHCI | X | X | - | - | - | - | - | - | - | - | - |
| | LCD User Int. | X | X | - | - | - | - | - | - | - | - | - |
| | UDPHS RAM | X | X | - | - | - | - | - | - | - | - | - |
| | Reserved | X | X | - | - | - | - | - | - | - | - | - |
| 2 | DDR Port 0 | - | - | - | - | - | - | - | - | - | - | X |
| 3 | DDR Port 1 | - | - | - | - | - | - | X | - | - | - | - |
| 4 | DDR Port 2 | X | - | X | X | X | X | - | X | X | X | - |
| 5 | DDR Port 3 | - | X | X | X | X | X | - | X | X | X | - |
| 6 | EBI | X | X | X | X | X | X | X | X | X | X | X |
| 7 | Internal Periph. | X | X | X | - | X | - | - | - | - | - | - |

Table 6-5 summarizes the Slave Memory Mapping for each connected Master, depending on the Remap status (RCBx bit in Bus Matrix Master Remap Control Register MATRIX_MRCR) and the BMS state at reset.

**Table 6-5. Internal Memory Mapping**

| | Master | | |
|---|---|---|---|
| Slave Base Address | RCBx = 0 | | RCBx = 1 |
| | BMS = 1 | BMS = 0 | |
| 0x0000 0000 | Internal ROM | EBI NCS0 | Internal SRAM |

## 6.3 Peripheral DMA Controller (PDC)

- Acting as one AHB Bus Matrix Master
- Allows data transfers from/to peripheral to/from any memory space without any intervention of the processor.
- Next Pointer support, prevents strong real-time constraints on buffer management.

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

**Table 6-6. Peripheral DMA Controller**

| Instance name | Channel T/R |
|---|---|
| DBGU | Transmit |
| USART3 | Transmit |
| USART2 | Transmit |
| USART1 | Transmit |
| USART0 | Transmit |
| AC97C | Transmit |
| SPI1 | Transmit |
| SPI0 | Transmit |
| SSC1 | Transmit |
| SSC0 | Transmit |
| TSADCC | Receive |
| DBGU | Receive |
| USART3 | Receive |
| USART2 | Receive |
| USART1 | Receive |
| USART0 | Receive |
| AC97C | Receive |
| SPI1 | Receive |
| SPI0 | Receive |
| SSC1 | Receive |
| SSC0 | Receive |

## 6.4 USB

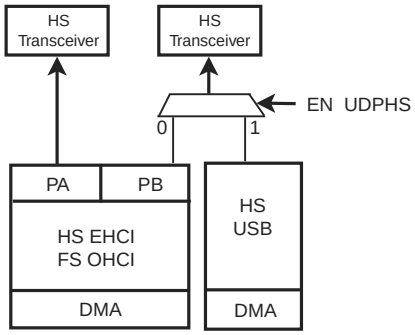
The SAM9G45 features USB communication ports as follows:

- 2 Ports USB Host full speed OHCI and High speed EHCI
- 1 Device High speed

USB Host Port A is directly connected to the first UTMI transceiver.

The Host Port B is multiplexed with the USB device High speed and connected to the second UTMI port. The selection between Host Port B and USB device high speed is controlled by a the bit UDPHS enable bit located in the UDPHS_CTRL control register.

**Figure 6-2. USB Selection**




## 6.5 DMA Controller

- Two Masters
- Embeds 8 channels
- 64 bytes/FIFO for Channel Buffering
- Linked List support with Status Write Back operation at End of Transfer
- Word, HalfWord, Byte transfer support.
- memory to memory transfer
- Peripheral to memory
- Memory to peripheral

The DMA controller can handle the transfer between peripherals and memory and so receives the triggers from the peripherals below. The hardware interface numbers are also given below in Table 6-7.

**Table 6-7. DMA Channel Definition**

| Instance Name | T/R | DMA Channel HW interface Number |
|---|---|---|
| MCI0 | TX/RX | 0 |
| SPI0 | TX | 1 |
| SPI0 | RX | 2 |
| SPI1 | TX | 3 |
| SPI1 | RX | 4 |
| SSC0 | TX | 5 |
| SSC0 | RX | 6 |
| SSC1 | TX | 7 |
| SSC1 | RX | 8 |
| AC97C | TX | 9 |
| AC97C | RX | 10 |
| MCI1 | TX/RX | 13 |

## 6.6 Debug and Test Features

- ARM926 Real-time In-circuit Emulator
  - Two real-time Watchpoint Units
  - Two Independent Registers: Debug Control Register and Debug Status Register
  - Test Access Port Accessible through JTAG Protocol
  - Debug Communications Channel
- Debug Unit
  - Two-pin UART
  - Debug Communication Channel Interrupt Handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on All Digital Pins.

- Internal SRAM B is the ARM926EJ-S Data TCM. The user can map this SRAM block anywhere in the ARM926 data memory space using CP15 instructions. This SRAM block is also accessible by the ARM926 Data Master and by the AHB Masters through the AHB bus.
- Internal SRAM C is only accessible by all the AHB Masters. After reset and until the Remap Command is performed, this SRAM block is accessible through the AHB bus at address 0x0030 0000 by all the AHB Masters. After Remap, this SRAM block also becomes accessible through the AHB bus at address 0x0 by the ARM926 Instruction and the ARM926 Data Masters.

Within the 64 Kbyte SRAM size available, the amount of memory assigned to each block is software programmable according to Table 7-1.

**Table 7-1. ITCM and DTCM Memory Configuration**

| SRAM A ITCM size (KBytes) seen at 0x100000 through AHB | SRAM B DTCM size (KBytes) seen at 0x200000 through AHB | SRAM C (KBytes) seen at 0x300000 through AHB |
|---|---|---|
| 0 | 0 | 64 |
| 0 | 64 | 0 |
| 32 | 32 | 0 |

### 7.2.3 Internal ROM

The SAM9G45 embeds an Internal ROM, which contains the Boot ROM and SAM-BA program.

At any time, the ROM is mapped at address 0x0040 0000. It is also accessible at address 0x0 (BMS =1) after the reset and before the Remap Command.

### 7.2.4 Boot Strategies

The system always boots at address 0x0. To ensure maximum boot possibilities the memory layout can be changed with two parameters.

REMAP allows the user to layout the internal SRAM bank to 0x0 to ease the development. This is done by software once the system has boot.

BMS allows the user to lay out to 0x0, when convenient, the ROM or an external memory. This is done by a hardware way at reset.

Note: All the memory blocks can always be seen at their specified base addresses that are not concerned by these parameters.

The SAM9G45 Bus Matrix manages a boot memory that depends on the level on the pin BMS at reset. The internal memory area mapped between address 0x0 and 0x000F FFFF is reserved to this effect.

If BMS is detected at 1, the boot memory is the embedded ROM.

If BMS is detected at 0, the boot memory is the memory connected on the Chip Select 0 of the External Bus Interface.

#### 7.2.4.1 BMS = 1, boot on embedded ROM

The system boots on Boot Program.

- Boot on on-chip RC
- Enable the 32768 Hz oscillator
- Auto baudrate detection
- Downloads and runs an application from external storage media into internal SRAM
- Downloaded code size depends on embedded SRAM size
- Automatic detection of valid application

- Bootloader on a non-volatile memory
  - SPI DataFlash/Serial Flash connected on NPCS0 of the SPI0
  - SDCard
  - Nand Flash
  - EEPROM connected on TWI0
- SAM-BA Boot in case no valid program is detected in external NVM, supporting
  - Serial communication on a DBGU
  - USB Device HS Port

#### 7.2.4.2 BMS = 0, boot on external memory

- Boot on on-chip RC
- Boot with the default configuration for the Static Memory Controller, byte select mode, 16-bit data bus, Read/Write controlled by Chip Select, allows boot on 16-bit non-volatile memory.

For optimization purpose, nothing else is done. To speed up the boot sequence user programmed software should perform a complete configuration:

- Enable the 32768 Hz oscillator if best accuracy needed
- Program the PMC (main oscillator enable or bypass mode)
- Program and Start the PLL
- Reprogram the SMC setup, cycle, hold, mode timings registers for EBI CS0 to adapt them to the new clock
- Switch the main clock to the new value

## 7.3 External Memories

The SAM9G45 features a Multi-port DDR2 Interface and an External Bus Interface allowing to connect to a wide range of external memories and to any parallel peripheral.

### 7.3.1 DDRSDRC0 Multi-port DDRSDR Controller

Four AHB Interfaces, Management of All Accesses Maximizes Memory Bandwidth and Minimizes Transaction Latency.

- Supports AHB Transfers:
  - Word, Half Word, Byte Access.
- Supports DDR2, LPDDR
- Numerous Configurations Supported
  - 2K, 4K, 8K, 16K Row Address Memory Parts
  - DDR2 with Four Internal Banks
  - DDR2/LPDDR with 16-bit Data Path
  - One Chip Select for DDR2/LPDDR Device (256 Mbytes Address Space)
- Programming Facilities
  - Multibank Ping-pong Access (Up to 4 Banks Opened at Same Time = Reduces Average Latency of Transactions)
  - Timing Parameters Specified by Software
  - Automatic Refresh Operation, Refresh Rate is Programmable
  - Automatic Update of DS, TCR and PASR Parameters
- Energy-saving Capabilities
  - Self-refresh, Power-down and Deep Power Modes Supported
- Power-up Initialization by Software
- CAS Latency of 2, 3 Supported
- Reset function supported (DDR2)
- Auto Precharge Command Not Used

- Wait internal RC Startup Time for clock stabilization (software loop).
- Switch from 32768 Hz oscillator to internal RC oscilllator by setting the bit OSCSEL to 0.
- Wait 5 slow clock cycles for internal resynchronization.
- Disable the 32768Hz oscillator by setting the bit OSC32EN to 0.

## 8.7 Power Management Controller

The Power Management Controller provides all the clock signals to the system.

PMC input clocks:

- UPLLCK: From UTMI PLL
- PLLACK From PLLA
- SLCK: slow clock from OSC32K or internal RC OSC
- MAINCK: from 12 MHz external oscillator

PMC output clocks

- Processor Clock PCK
- Master Clock MCK, in particular to the Matrix and the memory interfaces. The divider can be 1,2,3 or 4
- DDR system clock equal to 2xMCK

Note: DDR system clock is not available when Master Clock (MCK) equals Processor Clock (PCK).

- USB Host EHCI High speed clock (UPLLCK)
- USB OHCI clocks (UHP48M and UHP12M)
- Independent peripheral clocks, typically at the frequency of MCK
- Two programmable clock outputs: PCK0 and PCK1

This allows the software control of five flexible operating modes:

- Normal Mode, processor and peripherals running at a programmable frequency
- Idle Mode, processor stopped waiting for an interrupt
- Slow Clock Mode, processor and peripherals running at low frequency
- Standby Mode, mix of Idle and Backup Mode, peripheral running at low frequency, processor stopped waiting for an interrupt
- Backup Mode, Main Power Supplies off, VDDBU powered by a battery

## 9.3 Peripheral Interrupts and Clock Control

### 9.3.1 System Interrupt

The System Interrupt in Source 1 is the wired-OR of the interrupt signals coming from:

- the DDR2/LPDDR Controller
- the Debug Unit
- the Periodic Interval Timer
- the Real-Time Timer
- the Real-Time Clock
- the Watchdog Timer
- the Reset Controller
- the Power Management Controller

The clock of these peripherals cannot be deactivated and Peripheral ID 1 can only be used within the Advanced Interrupt Controller.

### 9.3.2 External Interrupts

All external interrupt signals, i.e., the Fast Interrupt signal FIQ or the Interrupt signal IRQ, use a dedicated Peripheral ID. However, there is no clock control associated with these peripheral IDs.

## 9.4 Peripheral Signals Multiplexing on I/O Lines

The SAM9G45 features 5 PIO controllers, PIOA, PIOB, PIOC, PIOD and PIOE, which multiplexes the I/O lines of the peripheral set.

Each PIO Controller controls up to 32 lines. Each line can be assigned to one of two peripheral functions, A or B. The multiplexing tables in the following paragraphs define how the I/O lines of the peripherals A and B are multiplexed on the PIO Controllers. The two columns “Function” and “Comments” have been inserted in this table for the user’s own comments; they may be used to track how pins are defined in an application.

Note that some peripheral function which are output only, might be duplicated within the both tables.

The column “Reset State” indicates whether the PIO Line resets in I/O mode or in peripheral mode. If I/O is mentioned, the PIO Line resets in input with the pull-up enabled, so that the device is maintained in a static state as soon as the reset is released. As a result, the bit corresponding to the PIO Line in the register PIO_PSR (Peripheral Status Register) resets low.

If a signal name is mentioned in the “Reset State” column, the PIO Line is assigned to this function and the corresponding bit in PIO_PSR resets high. This is the case of pins controlling memories, in particular the address lines, which require the pin to be driven as soon as the reset is released. Note that the pull-up resistor is also enabled in this case.

To amend EMC, programmable delay has been inserted on PIO lines able to run at high speed.

### 9.4.1 PIO Controller A Multiplexing

**Table 9-2. Multiplexing on PIO Controller A (PIOA)**

| I/O Line | Peripheral A | Peripheral B | Reset State | Power Supply | Function | Comments |
|---|---|---|---|---|---|---|
| PA0 | MCI0_CK | TCLK3 | I/O | VDDIOP0 | | |
| PA1 | MCI0_CDA | TIOA3 | I/O | VDDIOP0 | | |
| PA2 | MCI0_DA0 | TIOB3 | I/O | VDDIOP0 | | |
| PA3 | MCI0_DA1 | TCKL4 | I/O | VDDIOP0 | | |
| PA4 | MCI0_DA2 | TIOA4 | I/O | VDDIOP0 | | |
| PA5 | MCI0_DA3 | TIOB4 | I/O | VDDIOP0 | | |
| PA6 | MCI0_DA4 | ETX2 | I/O | VDDIOP0 | | |
| PA7 | MCI0_DA5 | ETX3 | I/O | VDDIOP0 | | |
| PA8 | MCI0_DA6 | ERX2 | I/O | VDDIOP0 | | |
| PA9 | MCI0_DA7 | ERX3 | I/O | VDDIOP0 | | |
| PA10 | ETX0 | | I/O | VDDIOP0 | | |
| PA11 | ETX1 | | I/O | VDDIOP0 | | |
| PA12 | ERX0 | | I/O | VDDIOP0 | | |
| PA13 | ERX1 | | I/O | VDDIOP0 | | |
| PA14 | ETXEN | | I/O | VDDIOP0 | | |
| PA15 | ERXDV | | I/O | VDDIOP0 | | |
| PA16 | ERXER | | I/O | VDDIOP0 | | |
| PA17 | ETXCK | | I/O | VDDIOP0 | | |
| PA18 | EMDC | | I/O | VDDIOP0 | | |
| PA19 | EMDIO | | I/O | VDDIOP0 | | |
| PA20 | TWD0 | | I/O | VDDIOP0 | | |
| PA21 | TWCK0 | | I/O | VDDIOP0 | | |
| PA22 | MCI1_CDA | SCK3 | I/O | VDDIOP0 | | |
| PA23 | MCI1_DA0 | RTS3 | I/O | VDDIOP0 | | |
| PA24 | MCI1_DA1 | CTS3 | I/O | VDDIOP0 | | |
| PA25 | MCI1_DA2 | PWM3 | I/O | VDDIOP0 | | |
| PA26 | MCI1_DA3 | TIOB2 | I/O | VDDIOP0 | | |
| PA27 | MCI1_DA4 | ETXER | I/O | VDDIOP0 | | |
| PA28 | MCI1_DA5 | ERXCK | I/O | VDDIOP0 | | |
| PA29 | MCI1_DA6 | ECRS | I/O | VDDIOP0 | | |
| PA30 | MCI1_DA7 | ECOL | I/O | VDDIOP0 | | |
| PA31 | MCI1_CK | PCK0 | I/O | VDDIOP0 | | |

### 9.4.3 PIO Controller C Multiplexing

**Table 9-4. Multiplexing on PIO Controller C (PIOC)**

| I/O Line | Peripheral A | Peripheral B | Reset State | Power Supply | Function | Comments |
|---|---|---|---|---|---|---|
| PC0 | DQM2 | | DQM2 | VDDIOM1 | | |
| PC1 | DQM3 | | DQM3 | VDDIOM1 | | |
| PC2 | A19 | | A19 | VDDIOM1 | | |
| PC3 | A20 | | A20 | VDDIOM1 | | |
| PC4 | A21/NANDALE | | A21 | VDDIOM1 | | |
| PC5 | A22/NANDCLE | | A22 | VDDIOM1 | | |
| PC6 | A23 | | A23 | VDDIOM1 | | |
| PC7 | A24 | | A24 | VDDIOM1 | | |
| PC8 | CFCE1 | | I/O | VDDIOM1 | | |
| PC9 | CFCE2 | RTS2 | I/O | VDDIOM1 | | |
| PC10 | NCS4/CFCS0 | TCLK2 | I/O | VDDIOM1 | | |
| PC11 | NCS5/CFCS1 | CTS2 | I/O | VDDIOM1 | | |
| PC12 | A25/CFRNW | | A25 | VDDIOM1 | | |
| PC13 | NCS2 | | I/O | VDDIOM1 | | |
| PC14 | NCS3/NANDCS | | I/O | VDDIOM1 | | |
| PC15 | NWAIT | | I/O | VDDIOM1 | | |
| PC16 | D16 | | I/O | VDDIOM1 | | |
| PC17 | D17 | | I/O | VDDIOM1 | | |
| PC18 | D18 | | I/O | VDDIOM1 | | |
| PC19 | D19 | | I/O | VDDIOM1 | | |
| PC20 | D20 | | I/O | VDDIOM1 | | |
| PC21 | D21 | | I/O | VDDIOM1 | | |
| PC22 | D22 | | I/O | VDDIOM1 | | |
| PC23 | D23 | | I/O | VDDIOM1 | | |
| PC24 | D24 | | I/O | VDDIOM1 | | |
| PC25 | D25 | | I/O | VDDIOM1 | | |
| PC26 | D26 | | I/O | VDDIOM1 | | |
| PC27 | D27 | | I/O | VDDIOM1 | | |
| PC28 | D28 | | I/O | VDDIOM1 | | |
| PC29 | D29 | | I/O | VDDIOM1 | | |
| PC30 | D30 | | I/O | VDDIOM1 | | |
| PC31 | D31 | | I/O | VDDIOM1 | | |

### 9.4.5 PIO Controller E Multiplexing

**Table 9-6. Multiplexing on PIO Controller E (PIOE)**

| I/O Line | Peripheral A | Peripheral B | Reset State | Power Supply | Function | Comments |
|---|---|---|---|---|---|---|
| PE0 | LCDPWR | PCK0 | I/O | VDDIOP1 | | |
| PE1 | LCDMOD | | I/O | VDDIOP1 | | |
| PE2 | LCDCC | | I/O | VDDIOP1 | | |
| PE3 | LCDVSYNC | | I/O | VDDIOP1 | | |
| PE4 | LCDHSYNC | | I/O | VDDIOP1 | | |
| PE5 | LCDDOTCK | | I/O | VDDIOP1 | | |
| PE6 | LCDDEN | | I/O | VDDIOP1 | | |
| PE7 | LCDD0 | LCDD2 | I/O | VDDIOP1 | | |
| PE8 | LCDD1 | LCDD3 | I/O | VDDIOP1 | | |
| PE9 | LCDD2 | LCDD4 | I/O | VDDIOP1 | | |
| PE10 | LCDD3 | LCDD5 | I/O | VDDIOP1 | | |
| PE11 | LCDD4 | LCDD6 | I/O | VDDIOP1 | | |
| PE12 | LCDD5 | LCDD7 | I/O | VDDIOP1 | | |
| PE13 | LCDD6 | LCDD10 | I/O | VDDIOP1 | | |
| PE14 | LCDD7 | LCDD11 | I/O | VDDIOP1 | | |
| PE15 | LCDD8 | LCDD12 | I/O | VDDIOP1 | | |
| PE16 | LCDD9 | LCDD13 | I/O | VDDIOP1 | | |
| PE17 | LCDD10 | LCDD14 | I/O | VDDIOP1 | | |
| PE18 | LCDD11 | LCDD15 | I/O | VDDIOP1 | | |
| PE19 | LCDD12 | LCDD18 | I/O | VDDIOP1 | | |
| PE20 | LCDD13 | LCDD19 | I/O | VDDIOP1 | | |
| PE21 | LCDD14 | LCDD20 | I/O | VDDIOP1 | | |
| PE22 | LCDD15 | LCDD21 | I/O | VDDIOP1 | | |
| PE23 | LCDD16 | LCDD22 | I/O | VDDIOP1 | | |
| PE24 | LCDD17 | LCDD23 | I/O | VDDIOP1 | | |
| PE25 | LCDD18 | | I/O | VDDIOP1 | | |
| PE26 | LCDD19 | | I/O | VDDIOP1 | | |
| PE27 | LCDD20 | | I/O | VDDIOP1 | | |
| PE28 | LCDD21 | | I/O | VDDIOP1 | | |
| PE29 | LCDD22 | | I/O | VDDIOP1 | | |
| PE30 | LCDD23 | | I/O | VDDIOP1 | | |
| PE31 | PWM2 | PCK1 | I/O | VDDIOP1 | | |

- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo

## 10.4 Serial Synchronous Controller (SSC)

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, $I^2S$, TDM Buses, Magnetic Card Reader,...)
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

## 10.5 AC97 Controller

- Compatible with AC97 Component Specification V2.2
- Capable to Interface with a Single Analog Front end
- Three independent RX Channels and three independent TX Channels
  - One RX and one TX channel dedicated to the AC97 Analog Front end control
  - One RX and one TX channel for data transfers, associated with a PDC
  - One RX and one TX channel for data transfers with no PDC
- Time Slot Assigner allowing to assign up to 12 time slots to a channel
- Channels support mono or stereo up to 20 bit sample length
  - Variable sampling rate AC97 Codec Interface (48KHz and below)

## 10.6 Timer Counter (TC)

- Three 16-bit Timer Counter Channels
- Wide range of functions including:
  - Frequency Measurement
  - Event Counting
  - Interval Measurement
  - Pulse Generation
  - Delay Timing
  - Pulse Width Modulation
  - Up/down Capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs
  - Five internal clock inputs
  - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels

## 10.7 Pulse Width Modulation Controller (PWM)

- Four channels, one 16-bit counter per channel

- 1, 2 bits per pixel (palletized), 4 bits per pixel (non-palletized) for mono STN
- 1, 2, 4, 8 bits per pixel (palletized), 16 bits per pixel (non-palletized) for color STN
- 1, 2, 4, 8 bits per pixel (palletized), 16, 24 bits per pixel (non-palletized) for TFT
- Single clock domain architecture
- Resolution supported up to 2048 x 2048

## 10.12 Touch Screen Analog-to-Digital Converter (TSADC)

- 8-channel ADC
- Support 4-wire resistive Touch Screen
- 10-bit 384 Ksamples/sec. Successive Approximation Register ADC
- -3/+3 LSB Integral Non Linearity, -2/+2 LSB Differential Non Linearity
- Integrated 8-to-1 multiplexer, offering eight independent 3.3V analog inputs
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger sources
    - Hardware or software trigger
    - External trigger pin
- Sleep Mode and conversion sequencer
    - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels

## 10.13 Ethernet 10/100 MAC (EMAC)

- Compatibility with IEEE Standard 802.3
- 10 and 100 MBits per second data throughput capability
- Full- and half-duplex operations
- MII or RMII interface to the physical layer
- Register Interface to address, data, status and control registers
- DMA Interface, operating as a master on the Memory Controller
- Interrupt generation to signal receive and transmit completion
- 128-byte transmit and 128-byte receive FIFOs
- Automatic pad and CRC generation on transmitted frames
- Address checking logic to recognize four 48-bit addresses
- Supports promiscuous mode where all valid frames are copied to memory
- Supports physical layer management through MDIO interface
- Supports Wake On Lan. The receiver supports Wake on LAN by detecting the following events on incoming receive frames:
    - Magic packet
    - ARP request to the device IP address
    - Specific address 1 filter match
    - Multicast hash filter match

## 10.14 Image Sensor Interface (ISI)

- ITU-R BT. 601/656 8-bit mode external interface support
- Support for ITU-R BT.656-4 SAV and EAV synchronization
- Vertical and horizontal resolutions up to 2048 x 2048
- Preview Path up to 640*480
- Support for packed data formatting for YCbCr 4:2:2 formats

# 12. SAM9G45 Ordering Information

**Table 12-1. AT91SAM9G45 Ordering Information**

| Ordering Code | MRL | Package | Package Type | Temperature Operating Range |
|---|---|---|---|---|
| AT91SAM9G45C-CU | C | TFBGA324 | Green | Industrial<br>-40°C to 85°C |
| AT91SAM9G45B-CU | B | TFBGA324 | Green | Industrial<br>-40°C to 85°C |
| AT91SAM9G45-CU | A | TFBGA324 | Green | Industrial<br>-40°C to 85°C |

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