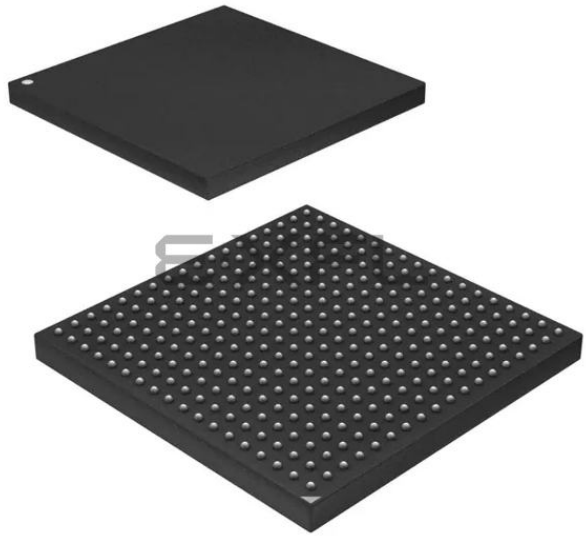

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, LPSDR, DDR2, SDR, SRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD, Touchscreen
Ethernet	10/100Mbps
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	324-TFBGA
Supplier Device Package	324-TFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam9g45c-cu-999

3. Signal Description

Table 3-1 gives details on the signal names classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
Power Supplies					
VDDIOM0	DDR2 I/O Lines Power Supply	Power			1.65V to 1.95V
VDDIOM1	EBI I/O Lines Power Supply	Power			1.65V to 1.95V or 3.0V to3.6V
VDDIOP0	Peripherals I/O Lines Power Supply	Power			1.65V to 3.6V
VDDIOP1	Peripherals I/O Lines Power Supply	Power			1.65V to 3.6V
VDDIOP2	ISI I/O Lines Power Supply	Power			1.65V to 3.6V
VDDBU	Backup I/O Lines Power Supply	Power			1.8V to 3.6V
VDDANA	Analog Power Supply	Power			3.0V to 3.6V
VDDPLLA	PLLA Power Supply	Power			0.9V to 1.1V
VDDPLLUTMI	PLLUTMI Power Supply	Power			0.9V to 1.1V
VDDOSC	Oscillator Power Supply	Power			1.65V to 3.6V
VDDCORE	Core Chip Power Supply	Power			0.9V to 1.1V
VDDUTMIC	UDPHS and UHPHS UTMI+ Core Power Supply	Power			0.9V to 1.1V
VDDUTMII	UDPHS and UHPHS UTMI+ interface Power Supply	Power			3.0V to 3.6V
GNDIOM	DDR2 and EBI I/O Lines Ground	Ground			
GNDIOP	Peripherals and ISI I/O lines Ground	Ground			
GNDCORE	Core Chip Ground	Ground			
GNDOSC	PLLA, PLLUTMI and Oscillator Ground	Ground			
GNDBU	Backup Ground	Ground			
GNDUTMI	UDPHS and UHPHS UTMI+ Core and interface Ground	Ground			
GNDANA	Analog Ground	Ground			
Clocks, Oscillators and PLLs					
XIN	Main Oscillator Input	Input			
XOUT	Main Oscillator Output	Output			
XIN32	Slow Clock Oscillator Input	Input			
XOUT32	Slow Clock Oscillator Output	Output			
VBG	Bias Voltage Reference for USB	Analog			
PCK0 - PCK1	Programmable Clock Output	Output		(1)	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
Shutdown, Wakeup Logic					
SHDN	Shut-Down Control	Output		VDDBU	Driven at 0V only. 0: The device is in backup mode 1: The device is running (not in backup mode).
WKUP	Wake-Up Input	Input		VDDBU	Accept between 0V and VDDBU.
ICE and JTAG					
TCK	Test Clock	Input		VDDIOP0	No pull-up resistor, Schmitt trigger
TDI	Test Data In	Input		VDDIOP0	No pull-up resistor, Schmitt trigger
TDO	Test Data Out	Output		VDDIOP0	
TMS	Test Mode Select	Input		VDDIOP0	No pull-up resistor, Schmitt trigger
JTAGSEL	JTAG Selection	Input		VDDBU	Pull-down resistor (15 kΩ).
RTCK	Return Test Clock	Output		VDDIOP0	
Reset/Test					
NRST	Microcontroller Reset[2]	I/O	Low	VDDIOP0	Open-drain output, Pull-Up resistor (100 kΩ), Schmitt trigger
TST	Test Mode Select	Input		VDDBU	Pull-down resistor (15 kΩ), Schmitt trigger
NTRST	Test Reset Signal	Input		VDDIOP0	Pull-Up resistor (100 kΩ), Schmitt trigger
BMS	Boot Mode Select	**Input**		VDDIOP0	must be connected to GND or VDDIOP.
Debug Unit - DBGU					
DRXD	Debug Receive Data	Input		[1]	
DTXD	Debug Transmit Data	Output		[1]	
Advanced Interrupt Controller - AIC					
IRQ	External Interrupt Input	Input		[1]	
FIQ	Fast Interrupt Input	Input		[1]	
PIO Controller - PIOA- PIOB - PIOC - PIOD - PIOE					
PA0 - PA31	Parallel IO Controller A	I/O		[1]	Pulled-up input at reset (100kΩ)[3], Schmitt trigger
PB0 - PB31	Parallel IO Controller B	I/O		[1]	Pulled-up input at reset (100kΩ)[3], Schmitt trigger
PC0 - PC31	Parallel IO Controller C	I/O		[1]	Pulled-up input at reset (100kΩ)[3], Schmitt trigger

4. Package and Pinout

The SAM9G45 is delivered in a 324-ball TFBGA package.

4.1 Mechanical Overview of the 324-ball TFBGA Package

Figure 4-1 shows the orientation of the 324-ball TFBGA Package

Figure 4-1. Orientation of the 324-ball TFBGA Package

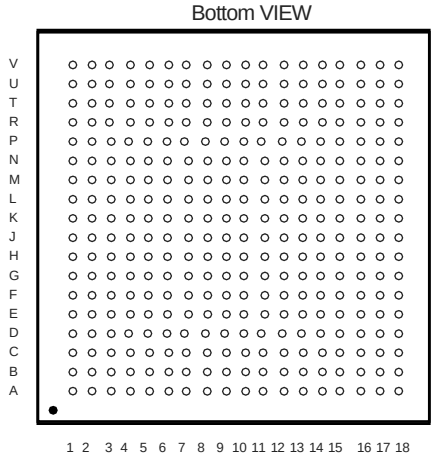


Table 4-1. SAM9G45 Pinout for 324-ball BGA Package (Continued)

Pin	Signal Name
C15	D2
C16	GNDIOM
C17	A18
C18	A12
D1	XOUT32
D2	PD20
D3	GNDBU
D4	VDDBU
D5	PC24
D6	PC18
D7	PC13
D8	PC6
D9	NWR1/NBS1
D10	NANDOE
D11	DQM1
D12	D14
D13	D9
D14	D5
D15	D1
D16	VDDIOM1
D17	A11
D18	A10
E1	PD21
E2	TSADVREF
E3	VDDANA
E4	JTAGSEL
E5	TST
E6	PC23
E7	PC16
E8	PC8
E9	PC1

Pin	Signal Name
H6	PE7
H7	PE9
H8	PE10
H9	GNDCORE
H10	GNDIOP
H11	VDDCORE
H12	GNDIOM
H13	GNDIOM
H14	DDR_CS
H15	DDR_WE
H16	DDR_DQM1
H17	DDR_CAS
H18	DDR_NCLK
J1	PE19
J2	PE16
J3	PE14
J4	PE15
J5	PE12
J6	PE17
J7	PE18
J8	PE20
J9	GNDCORE
J10	GNDCORE
J11	GNDIOP
J12	GNDIOM
J13	GNDIOM
J14	DDR_A12
J15	DDR_A13
J16	DDR_CKE
J17	DDR_RAS
J18	DDR_CLK

Pin	Signal Name
M15	DDR_D14
M16	DDR_D15
M17	DDR_A0
M18	DDR_A2
N1	PA3
N2	PA9
N3	PA12
N4	PA15
N5	PA16
N6	PA17
N7	PB18
N8	PD6
N9	PD16
N10	NTRST
N11	PB9
N12	PB24
N13	PB28
N14	DDR_D13
N15	DDR_D8
N16	DDR_D9
N17	DDR_D11
N18	DDR_D12
P1	PA11
P2	PA13
P3	PA19
P4	PA21
P5	PA23
P6	PB12
P7	PB19
P8	PD8
P9	PD28

Pin	Signal Name
U6	PB17
U7	PD7
U8	PD10
U9	PD14
U10	TCK
U11	VDDOSC
U12	GNDOSC
U13	PB10
U14	PB26
U15	HHSDPB/DHSDP
U16	HHSDMB/DHSDM
U17	GNDUTMI
U18	VDDUTMIC
V1	PA31
V2	PB1
V3	PB2
V4	PB5
V5	PB15
V6	PD3
V7	PD5
V8	PD12
V9	PD17
V10	TDO
V11	XOUT
V12	XIN
V13	VDDPLLUTMI
V14	VDDIOP2
V15	HFSDPB/DFSDP
V16	HFSDMB/DFSDM
V17	VDDUTMII
V18	VBG

5. Power Considerations

5.1 Power Supplies

The SAM9G45 has several types of power supply pins:

- VDDCORE pins: Power the core, including the processor, the embedded memories and the peripherals; voltage ranges from 0.9V to 1.1V, 1.0V typical.
- VDDIOM0 pins: Power the DDR2/LPDDR I/O lines; voltage ranges between 1.65V and 1.95V (1.8V typical).
- VDDIOM1 pins: Power the External Bus Interface 1 I/O lines; voltage ranges between 1.65V and 1.95V (1.8V typical) or between 3.0V and 3.6V (3.3V typical).
- VDDIOP0, VDDIOP1, VDDIOP2 pins: Power the Peripherals I/O lines; voltage ranges from 1.65V to 3.6V.
- VDDBU pin: Powers the Slow Clock oscillator, the internal RC oscillator and a part of the System Controller; voltage ranges from 1.8V to 3.6V.
- VDDPLLUTMI pin: Powers the PLLUTMI cell; voltage range from 0.9V to 1.1V.
- VDDUTMIC pin: Powers the USB device and host UTMI+ core; voltage range from 0.9V to 1.1V, 1.0V typical.
- VDDUTMII pin: Powers the USB device and host UTMI+ interface; voltage range from 3.0V to 3.6V, 3.3V typical.
- VDDPLLA pin: Powers the PLLA cell; voltage ranges from 0.9V to 1.1V.
- VDDOSC pin: Powers the Main Oscillator cells; voltage ranges from 1.65V to 3.6V
- VDDANA pin: Powers the Analog to Digital Converter; voltage ranges from 3.0V to 3.6V, 3.3V typical.

Some supply pins share common ground (GND) pins whereas others have separate grounds.

The respective power/ground pin assignments are as follows:

VDDCORE	GNDCORE
VDDIOM0, VDDIOM1	GNDIOM
VDDIOP0, VDDIOP1, VDDIOP2	GNDIOP
VDDBU	GNDBU
VDDUTMIC, VDDUTMII	GNDUTMI
VDDPLLUTMI, VDDPLLA, VDDOSC,	GNDOSC
VDDANA	GNDANA

6. Processor and Architecture

6.1 ARM926EJ-S Processor

- RISC Processor Based on ARM v5TEJ Architecture with Jazelle technology for Java acceleration
- Two Instruction Sets
  - ARM High-performance 32-bit Instruction Set
  - Thumb High Code Density 16-bit Instruction Set
- DSP Instruction Extensions
- 5-Stage Pipeline Architecture:
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)
  - Data Memory (M)
  - Register Write (W)
- 32-KByte Data Cache, 32-KByte Instruction Cache
  - Virtually-addressed 4-way Associative Cache
  - Eight words per line
  - Write-through and Write-back Operation
  - Pseudo-random or Round-robin Replacement
- Write Buffer
  - Main Write Buffer with 16-word Data Buffer and 4-address Buffer
  - DCache Write-back Buffer with 8-word Entries and a Single Address Entry
  - Software Control Drain
- Standard ARM v4 and v5 Memory Management Unit (MMU)
  - Access Permission for Sections
  - Access Permission for large pages and small pages can be specified separately for each quarter of the page
  - 16 embedded domains
- Bus Interface Unit (BIU)
  - Arbitrates and Schedules AHB Requests
  - Separate Masters for both instruction and data access providing complete Matrix system flexibility
  - Separate Address and Data Buses for both the 32-bit instruction interface and the 32-bit data interface
  - On Address and Data Buses, data can be 8-bit (Bytes), 16-bit (Half-words) or 32-bit (Words)
- TCM Interface

Table 6-4. SAM9G45 Masters to Slaves Access with DDRMP_DIS = 1 (default)

Master		0	1	2	3	4 & 5	6	7	8	9	10	11
Slave		ARM 926 Instr.	ARM 926 Data	PDC	USB HOST OHCI	DMA	ISI DMA	LCD DMA	Ethernet MAC	USB Device HS	USB Host EHCI	Reserved
0	Internal SRAM 0	X	X	X	X	X	X	-	X	X	X	-
1	Internal ROM	X	X	X	-	-	-	-	-	X	-	-
	UHP OHCI	X	X	-	-	-	-	-	-	-	-	-
	UHP EHCI	X	X	-	-	-	-	-	-	-	-	-
	LCD User Int.	X	X	-	-	-	-	-	-	-	-	-
	UDPHS RAM	X	X	-	-	-	-	-	-	-	-	-
	Reserved	X	X	-	-	-	-	-	-	-	-	-
2	DDR Port 0	-	-	-	-	-	-	-	-	-	-	X
3	DDR Port 1	-	-	-	-	-	-	X	-	-	-	-
4	DDR Port 2	X	-	X	X	X	X	-	X	X	X	-
5	DDR Port 3	-	X	X	X	X	X	-	X	X	X	-
6	EBI	X	X	X	X	X	X	X	X	X	X	X
7	Internal Periph.	X	X	X	-	X	-	-	-	-	-	-

Table 6-5 summarizes the Slave Memory Mapping for each connected Master, depending on the Remap status (RCBx bit in Bus Matrix Master Remap Control Register MATRIX_MRCR) and the BMS state at reset.

Table 6-5. Internal Memory Mapping

	Master		
Slave Base Address	RCBx = 0		RCBx = 1
	BMS = 1	BMS = 0	
0x0000 0000	Internal ROM	EBI NCS0	Internal SRAM

6.3 Peripheral DMA Controller (PDC)

- Acting as one AHB Bus Matrix Master
- Allows data transfers from/to peripheral to/from any memory space without any intervention of the processor.
- Next Pointer support, prevents strong real-time constraints on buffer management.

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

Table 6-6. Peripheral DMA Controller

Instance name	Channel T/R
DBGU	Transmit
USART3	Transmit
USART2	Transmit
USART1	Transmit
USART0	Transmit
AC97C	Transmit
SPI1	Transmit
SPI0	Transmit
SSC1	Transmit
SSC0	Transmit
TSADCC	Receive
DBGU	Receive
USART3	Receive
USART2	Receive
USART1	Receive
USART0	Receive
AC97C	Receive
SPI1	Receive
SPI0	Receive
SSC1	Receive
SSC0	Receive

6.4 USB

The SAM9G45 features USB communication ports as follows:

- 2 Ports USB Host full speed OHCI and High speed EHCI
- 1 Device High speed

USB Host Port A is directly connected to the first UTMI transceiver.

The Host Port B is multiplexed with the USB device High speed and connected to the second UTMI port. The selection between Host Port B and USB device high speed is controlled by a the bit UDPHS enable bit located in the UDPHS_CTRL control register.

7.1 Memory Mapping

A first level of address decoding is performed by the AHB Bus Matrix, i.e., the implementation of the Advanced High performance Bus (AHB) for its Master and Slave interfaces with additional features.

Decoding breaks up the 4 Gbytes of address space into 16 banks of 256 Mbytes. The banks 1 to 6 are directed to the EBI that associates these banks to the external chip selects NCS0 to NCS5.

The bank 7 is directed to the DDRSDRC0 that associates this bank to DDR_NCS chip select and so dedicated to the 4-port DDR2/LPDDR controller.

The bank 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1 Mbyte of internal memory area. The bank 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

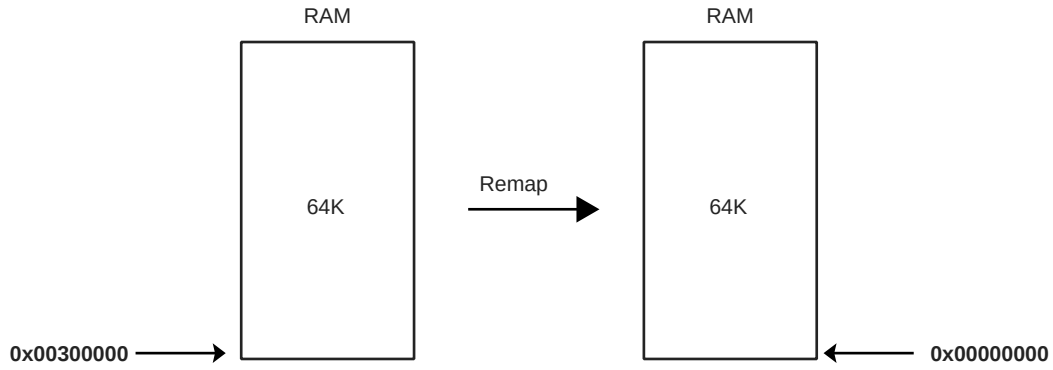
Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

7.2 Embedded Memories

7.2.1 Internal SRAM

The SAM9G45 product embeds a total of 64 Kbytes high-speed SRAM split in 4 blocks of 16 KBytes connected to one slave of the matrix. After reset and until the Remap Command is performed, the four SRAM blocks are contiguous and only accessible at address 0x00300000. After Remap, the SRAM also becomes available at address 0x0.

Figure 7-2. Internal SRAM Reset



The SAM9G45 device embeds two memory features. The processor Tightly Coupled Memory Interface (TCM) that allows the processor to access the memory up to processor speed (PCK) and the interface on the AHB side allowing masters to access the memory at AHB speed (MCK).

A wait state is necessary to access the TCM at 400 MHz. Setting the bit NWS_TCM in the bus Matrix TCM Configuration Register of the matrix inserts a wait state on the ITCM and DTCM accesses.

7.2.2 TCM Interface

On the processor side, this Internal SRAM can be allocated to two areas.

- Internal SRAM A is the ARM926EJ-S Instruction TCM. The user can map this SRAM block anywhere in the ARM926 instruction memory space using CP15 instructions and the TCR configuration register located in the Chip Configuration User Interface. This SRAM block is also accessible by the ARM926 Masters and by the AHB Masters through the AHB bus

- Internal SRAM B is the ARM926EJ-S Data TCM. The user can map this SRAM block anywhere in the ARM926 data memory space using CP15 instructions. This SRAM block is also accessible by the ARM926 Data Master and by the AHB Masters through the AHB bus.
- Internal SRAM C is only accessible by all the AHB Masters. After reset and until the Remap Command is performed, this SRAM block is accessible through the AHB bus at address 0x0030 0000 by all the AHB Masters. After Remap, this SRAM block also becomes accessible through the AHB bus at address 0x0 by the ARM926 Instruction and the ARM926 Data Masters.

Within the 64 Kbyte SRAM size available, the amount of memory assigned to each block is software programmable according to Table 7-1.

Table 7-1. ITCM and DTCM Memory Configuration

SRAM A ITCM size (KBytes) seen at 0x100000 through AHB	SRAM B DTCM size (KBytes) seen at 0x200000 through AHB	SRAM C (KBytes) seen at 0x300000 through AHB
0	0	64
0	64	0
32	32	0

7.2.3 Internal ROM

The SAM9G45 embeds an Internal ROM, which contains the Boot ROM and SAM-BA program.

At any time, the ROM is mapped at address 0x0040 0000. It is also accessible at address 0x0 (BMS =1) after the reset and before the Remap Command.

7.2.4 Boot Strategies

The system always boots at address 0x0. To ensure maximum boot possibilities the memory layout can be changed with two parameters.

REMAP allows the user to layout the internal SRAM bank to 0x0 to ease the development. This is done by software once the system has boot.

BMS allows the user to lay out to 0x0, when convenient, the ROM or an external memory. This is done by a hardware way at reset.

Note: All the memory blocks can always be seen at their specified base addresses that are not concerned by these parameters.

The SAM9G45 Bus Matrix manages a boot memory that depends on the level on the pin BMS at reset. The internal memory area mapped between address 0x0 and 0x000F FFFF is reserved to this effect.

If BMS is detected at 1, the boot memory is the embedded ROM.

If BMS is detected at 0, the boot memory is the memory connected on the Chip Select 0 of the External Bus Interface.

7.2.4.1 BMS = 1, boot on embedded ROM

The system boots on Boot Program.

- Boot on on-chip RC
- Enable the 32768 Hz oscillator
- Auto baudrate detection
- Downloads and runs an application from external storage media into internal SRAM
- Downloaded code size depends on embedded SRAM size
- Automatic detection of valid application

- SDRAM Power-up Initialization by Software
- CAS Latency of 2, 3 Supported
- Auto Precharge Command Not Used
- SDR-SDRAM with 16-bit Datapath and Eight Columns Not Supported
    - Clock Frequency Change in Precharge Power-down Mode Not Supported

7.3.2.3 NAND Flash Error Corrected Code Controller

- Tracking the accesses to a NAND Flash device by triggering on the corresponding chip select
- Single bit error correction and 2-bit Random detection.
- Automatic Hamming Code Calculation while writing
    - ECC value available in a register
- Automatic Hamming Code Calculation while reading
    - Error Report, including error flag, correctable error flag and word address being detected erroneous
    - Support 8- or 16-bit NAND Flash devices with 512-, 1024-, 2048- or 4096-bytes pages

8.3 Reset Controller

The Reset Controller is based on two Power-on-Reset cells, one on VDDBU and one on VDDCORE.

The Reset Controller is capable to return to the software the source of the last reset, either a general reset (VDDBU rising), a wake-up reset (VDDCORE rising), a software reset, a user reset or a watchdog reset.

The Reset Controller controls the internal resets of the system and the NRST pin output. It is capable to shape a reset signal for the external devices, simplifying to a minimum connection of a push-button on the NRST pin to implement a manual reset.

The configuration of the Reset Controller is saved as supplied on VDDBU.

8.4 Shut Down Controller

The Shut Down Controller is supplied on VDDBU and allows a software-controllable shut down of the system through the pin SHDN. An input change of the WKUP pin or an alarm releases the SHDN pin, and thus wakes up the system power supply.

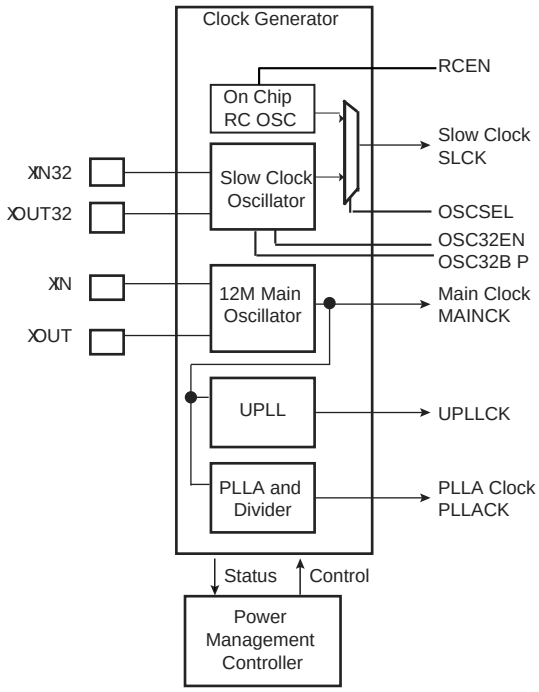
8.5 Clock Generator

The Clock Generator is made up of:

- One Low Power 32768 Hz Slow Clock Oscillator with bypass mode
- One Low-Power RC oscillator
- One 12 MHz Main Oscillator, which can be bypassed
- One 400 to 800 MHz programmable PLLA, capable to provide the clock MCK to the processor and to the peripherals. This PLL has an input divider to offer a wider range of output frequencies from the 12 MHz input, the only limitation being the lowest input frequency shall be higher or equal to 2 MHz.

The USB Device and Host HS Clocks are provided by a the dedicated UTMI PLL (UPLL) embedded in the UTMI macro.

Figure 8-2. Clock Generator Block Diagram



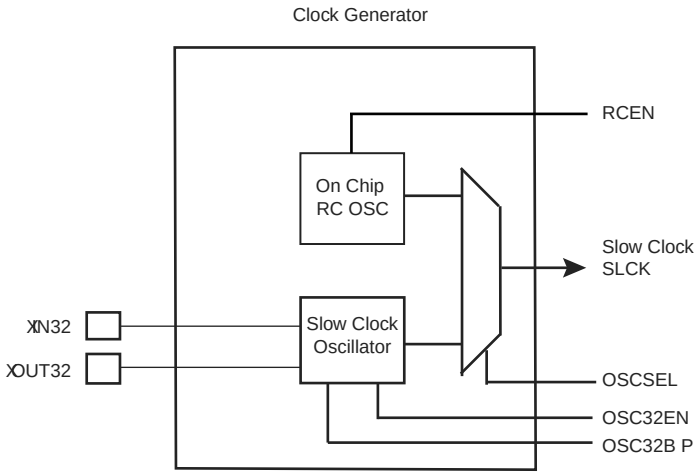
8.6 Slow Clock Selection

The SAM9G45 slow clock can be generated either by an external 32768Hz crystal or the on-chip RC oscillator. The 32768 Hz crystal oscillator can be bypassed, by setting the bit OSC32BYP, to accept an external slow clock on XIN32.

The internal RC oscillator and the 32768 Hz oscillator can be enabled by setting to 1 respectively RCEN bit and OSC32EN bit in the system controller user interface. OSCSEL command selects the slow clock source.

RCEN, OSC32EN,OSCSEL and OSC32BYP bits are located in the slow clock control register (SCKCR) located at address 0xFFFFFD50 in the backup part of the system controller and so are preserved while VDDBU is present.

Figure 8-3. Slow Clock



After a VDDBU power on reset, the default configuration is RCEN = 1, OSC32EN = 0 and OSCSEL = 0 allowing the system to start on the internal RC oscillator.

The programmer controls by software the slow clock switching and so must take precautions during the switching phase.

8.6.1 Switch from Internal RC Oscillator to the 32768 Hz Crystal

To switch from internal RC oscillator to the 32768 Hz crystal, the programmer must execute the following sequence:

- Switch the master clock to a source different from slow clock (PLLA or PLLB or Main Oscillator) through the Power Management Controller.
- Enable the 32768 Hz oscillator by setting the bit OSCEN to 1.
- Wait 32768 Hz startup time for clock stabilization (software loop).
- Switch from internal RC to 32768 Hz by setting the bit OSCSEL to 1.
- Wait 5 slow clock cycles for internal resynchronization.
- Disable the RC oscillator by setting the bit RCEN to 0.

8.6.2 Bypass the 32768 Hz Oscillator

The following step must be added to bypass the 32768 Hz Oscillator.

- An external clock must be connected on XIN32.
- Enable the bypass path OSC32BYP bit set to 1.
- Disable the 32768 Hz oscillator by setting the bit OSC32EN to 0.

8.6.3 Switch from 32768 Hz Crystal to the Internal RC Oscillator

The same procedure must be followed to switch from 32768 Hz crystal to the internal RC oscillator.

- Switch the master clock to a source different from slow clock (PLLA or PLLB or Main Oscillator).
- Enable the internal RC oscillator by setting the bit RCEN to 1.

- USB Device High Speed and Host EHCI High Speed operations are NOT allowed
- Full Speed OHCI input clock is PLLACK, USBDIV is 7 (division by 8)
- System Input clock is PLLACK, PCK is 384 MHz
- MDIV is ‘11’, MCK is 128 MHz
- DDR2 can be used at up to 128 MHz

8.8 Periodic Interval Timer

- Includes a 20-bit Periodic Counter, with less than 1µs accuracy
- Includes a 12-bit Interval Overlay Counter
- Real Time OS or Linux/WinCE compliant tick generator

8.9 Watchdog Timer

- 16-bit key-protected only-once-Programmable Counter
- Windowed, prevents the processor to be in a dead-lock on the watchdog access

8.10 Real-Time Timer

- Real-Time Timer, allowing backup of time with different accuracies
  - 32-bit Free-running back-up Counter
  - Integrates a 16-bit programmable prescaler running on slow clock
  - Alarm Register capable to generate a wake-up of the system through the Shut Down Controller

8.11 Real Time Clock

- Low power consumption
- Full asynchronous design
- Two hundred year calendar
- Programmable Periodic Interrupt
- Alarm and update parallel load
- Control of alarm and update Time/Calendar Data In

8.12 General-Purpose Backup Registers

- Four 32-bit backup general-purpose registers

8.13 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of the ARM Processor
- Thirty-two individually maskable and vectored interrupt sources
  - Source 0 is reserved for the Fast Interrupt Input (FIQ)
  - Source 1 is reserved for system peripherals (PIT, RTT, PMC, DBGU, etc.)
  - Programmable Edge-triggered or Level-sensitive Internal Sources
  - Programmable Positive/Negative Edge-triggered or High/Low Level-sensitive
- One External Sources plus the Fast Interrupt signal
- 8-level Priority Controller
  - Drives the Normal Interrupt of the processor
  - Handles priority of the interrupt sources 1 to 31
  - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
  - Optimizes Interrupt Service Routine Branch and Execution

9.4.1 PIO Controller A Multiplexing

Table 9-2. Multiplexing on PIO Controller A (PIOA)

I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PA0	MCI0_CK	TCLK3	I/O	VDDIOP0		
PA1	MCI0_CDA	TIOA3	I/O	VDDIOP0		
PA2	MCI0_DA0	TIOB3	I/O	VDDIOP0		
PA3	MCI0_DA1	TCKL4	I/O	VDDIOP0		
PA4	MCI0_DA2	TIOA4	I/O	VDDIOP0		
PA5	MCI0_DA3	TIOB4	I/O	VDDIOP0		
PA6	MCI0_DA4	ETX2	I/O	VDDIOP0		
PA7	MCI0_DA5	ETX3	I/O	VDDIOP0		
PA8	MCI0_DA6	ERX2	I/O	VDDIOP0		
PA9	MCI0_DA7	ERX3	I/O	VDDIOP0		
PA10	ETX0		I/O	VDDIOP0		
PA11	ETX1		I/O	VDDIOP0		
PA12	ERX0		I/O	VDDIOP0		
PA13	ERX1		I/O	VDDIOP0		
PA14	ETXEN		I/O	VDDIOP0		
PA15	ERXDV		I/O	VDDIOP0		
PA16	ERXER		I/O	VDDIOP0		
PA17	ETXCK		I/O	VDDIOP0		
PA18	EMDC		I/O	VDDIOP0		
PA19	EMDIO		I/O	VDDIOP0		
PA20	TWD0		I/O	VDDIOP0		
PA21	TWCK0		I/O	VDDIOP0		
PA22	MCI1_CDA	SCK3	I/O	VDDIOP0		
PA23	MCI1_DA0	RTS3	I/O	VDDIOP0		
PA24	MCI1_DA1	CTS3	I/O	VDDIOP0		
PA25	MCI1_DA2	PWM3	I/O	VDDIOP0		
PA26	MCI1_DA3	TIOB2	I/O	VDDIOP0		
PA27	MCI1_DA4	ETXER	I/O	VDDIOP0		
PA28	MCI1_DA5	ERXCK	I/O	VDDIOP0		
PA29	MCI1_DA6	ECRS	I/O	VDDIOP0		
PA30	MCI1_DA7	ECOL	I/O	VDDIOP0		
PA31	MCI1_CK	PCK0	I/O	VDDIOP0		

9.4.2 PIO Controller B Multiplexing

Table 9-3. Multiplexing on PIO Controller B (PIOB)

I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PB0	SPI0_MISO		I/O	VDDIOP0		
PB1	SPI0_MOSI		I/O	VDDIOP0		
PB2	SPI0_SPCK		I/O	VDDIOP0		
PB3	SPI0_NPCS0		I/O	VDDIOP0		
PB4	TXD1		I/O	VDDIOP0		
PB5	RXD1		I/O	VDDIOP0		
PB6	TXD2		I/O	VDDIOP0		
PB7	RXD2		I/O	VDDIOP0		
PB8	TXD3	ISI_D8	I/O	VDDIOP2		
PB9	RXD3	ISI_D9	I/O	VDDIOP2		
PB10	TWD1	ISI_D10	I/O	VDDIOP2		
PB11	TWCK1	ISI_D11	I/O	VDDIOP2		
PB12	DRXD		I/O	VDDIOP0		
PB13	DTXD		I/O	VDDIOP0		
PB14	SPI1_MISO		I/O	VDDIOP0		
PB15	SPI1_MOSI	CTS0	I/O	VDDIOP0		
PB16	SPI1_SPCK	SCK0	I/O	VDDIOP0		
PB17	SPI1_NPCS0	RTS0	I/O	VDDIOP0		
PB18	RXD0	SPI0_NPCS1	I/O	VDDIOP0		
PB19	TXD0	SPI0_NPCS2	I/O	VDDIOP0		
PB20	ISI_D0		I/O	VDDIOP2		
PB21	ISI_D1		I/O	VDDIOP2		
PB22	ISI_D2		I/O	VDDIOP2		
PB23	ISI_D3		I/O	VDDIOP2		
PB24	ISI_D4		I/O	VDDIOP2		
PB25	ISI_D5		I/O	VDDIOP2		
PB26	ISI_D6		I/O	VDDIOP2		
PB27	ISI_D7		I/O	VDDIOP2		
PB28	ISI_PCK		I/O	VDDIOP2		
PB29	ISI_VSYNC		I/O	VDDIOP2		
PB30	ISI_HSYNC		I/O	VDDIOP2		
PB31	ISI_MCK	PCK1	I/O	VDDIOP2		

9.4.3 PIO Controller C Multiplexing

Table 9-4. Multiplexing on PIO Controller C (PIOC)

I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PC0	DQM2		DQM2	VDDIOM1		
PC1	DQM3		DQM3	VDDIOM1		
PC2	A19		A19	VDDIOM1		
PC3	A20		A20	VDDIOM1		
PC4	A21/NANDALE		A21	VDDIOM1		
PC5	A22/NANDCLE		A22	VDDIOM1		
PC6	A23		A23	VDDIOM1		
PC7	A24		A24	VDDIOM1		
PC8	CFCE1		I/O	VDDIOM1		
PC9	CFCE2	RTS2	I/O	VDDIOM1		
PC10	NCS4/CFCS0	TCLK2	I/O	VDDIOM1		
PC11	NCS5/CFCS1	CTS2	I/O	VDDIOM1		
PC12	A25/CFRNW		A25	VDDIOM1		
PC13	NCS2		I/O	VDDIOM1		
PC14	NCS3/NANDCS		I/O	VDDIOM1		
PC15	NWAIT		I/O	VDDIOM1		
PC16	D16		I/O	VDDIOM1		
PC17	D17		I/O	VDDIOM1		
PC18	D18		I/O	VDDIOM1		
PC19	D19		I/O	VDDIOM1		
PC20	D20		I/O	VDDIOM1		
PC21	D21		I/O	VDDIOM1		
PC22	D22		I/O	VDDIOM1		
PC23	D23		I/O	VDDIOM1		
PC24	D24		I/O	VDDIOM1		
PC25	D25		I/O	VDDIOM1		
PC26	D26		I/O	VDDIOM1		
PC27	D27		I/O	VDDIOM1		
PC28	D28		I/O	VDDIOM1		
PC29	D29		I/O	VDDIOM1		
PC30	D30		I/O	VDDIOM1		
PC31	D31		I/O	VDDIOM1		

- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo

10.4 Serial Synchronous Controller (SSC)

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I^2S, TDM Buses, Magnetic Card Reader,...)
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

10.5 AC97 Controller

- Compatible with AC97 Component Specification V2.2
- Capable to Interface with a Single Analog Front end
- Three independent RX Channels and three independent TX Channels
  - One RX and one TX channel dedicated to the AC97 Analog Front end control
  - One RX and one TX channel for data transfers, associated with a PDC
  - One RX and one TX channel for data transfers with no PDC
- Time Slot Assigner allowing to assign up to 12 time slots to a channel
- Channels support mono or stereo up to 20 bit sample length
  - Variable sampling rate AC97 Codec Interface (48KHz and below)

10.6 Timer Counter (TC)

- Three 16-bit Timer Counter Channels
- Wide range of functions including:
  - Frequency Measurement
  - Event Counting
  - Interval Measurement
  - Pulse Generation
  - Delay Timing
  - Pulse Width Modulation
  - Up/down Capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs
  - Five internal clock inputs
  - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels

10.7 Pulse Width Modulation Controller (PWM)

- Four channels, one 16-bit counter per channel

- Common clock generator, providing Thirteen Different Clocks
  - A Modulo n counter providing eleven clocks
  - Two independent Linear Dividers working on modulo n counter outputs
- Independent channel programming
  - Independent Enable Disable Commands
  - Independent Clock Selection
  - Independent Period and Duty Cycle, with Double Buffering
  - Programmable selection of the output waveform polarity
  - Programmable center or left aligned output waveform

10.8 High Speed Multimedia Card Interface (MCI)

- Compatibility with MultiMedia Card Specification Version 4.3
- Compatibility with SD Memory Card Specification Version 2.0
- Compatibility with SDIO Specification Version V2.0.
- Compatibility with Memory Stick PRO
- Compatibility with CE ATA

10.9 USB High Speed Host Port (UHPHS)

- Compliant with Enhanced HCI Rev 1.0 Specification
  - Compliant with USB V2.0 High-speed and Full-speed Specification
  - Supports Both High-speed 480Mbps and Full-speed 12 Mbps USB devices
- Compliant with Open HCI Rev 1.0 Specification
  - Compliant with USB V2.0 Full-speed and Low-speed Specification
  - Supports Both Low-speed 1.5 Mbps and Full-speed 12 Mbps USB devices
- Root Hub Integrated with 2 Downstream USB Ports
- Shared Embedded USB Transceivers

10.10 USB High Speed Device Port (UDPHS)

- USB V2.0 high-speed compliant, 480 MBits per second
- Embedded USB V2.0 UTMI+ high-speed transceiver shared with UHP HS.
- Embedded 4-KByte dual-port RAM for endpoints
- Embedded 6 channels DMA controller
- Suspend/Resume logic
- Up to 2 or 3 banks for isochronous and bulk endpoints
- Seven endpoints:
  - Endpoint 0: 64 bytes, 1 bank mode
  - Endpoint 1 & 2: 1024 bytes, 2 banks mode, High Bandwidth, DMA
  - Endpoint 3 & 4: 1024 bytes, 3 banks mode, DMA
  - Endpoint 5 & 6: 1024 bytes, 3 banks mode, High Bandwidth, DMA

10.11 LCD Controller (LCDC)

- Single and Dual scan color and monochrome passive STN LCD panels supported
- Single scan active TFT LCD panels supported.
- 4-bit single scan, 8-bit single or dual scan, 16-bit dual scan STN interfaces supported
- Up to 24-bit single scan TFT interfaces supported
- Up to 16 gray levels for mono STN and up to 4096 colors for color STN displays

Revision History

In the table that follows, the initials “rfo” indicate changes requested by product experts, or made during proof reading as part of the approval process.

Doc. Rev	Comments	Change Request Ref.
6438AS	First issue	
6438BS	Section 3. “Signal Description”, Table 3-1 in “Reset/Test” description, NRST pin updated with note concerning NRST configuration. Section 4. “Package and Pinout”, Table 4-1, updated.	6600 6669
6438CS	Introduction: “Features” part was edited.	6715
	LFBGA replaced by TFBGA in “Features” part and Section 4.1 “Mechanical Overview of the 324-ball TFBGA Package”	RFO
	Section 3. “Signal Description”, Table 3-1, Touch Screen Analog-to-Digital Converter on page 9 part was edited.	6647
	VDDCORE removed from “Ground pins GND are common to...” sentence in Section 5.1 “Power Supplies”	RFO
	Figure 6.3 was removed. 0x00500000 changed into 0x00400000 in Section 7.2.3 “Internal ROM”.	6715
6438DS	“Two Three-channel 16-bit Timer/Counters” peripheral feature changed into “Two Three-channel 16-bit Timer/Counters” .	6828
	ECC row added to Figure 7-1 “SAM9G45 Memory Mapping”	6842
	Section 6.2 “Bus Matrix”, Figure 6-1 “DDR Multi-port”, and text above and below added. 1 row and 1 column added to Table 6-3 and Table 6-4.	6797
	Typos corrected in Table 6-6, Table 6-7, Table 9-1 and Figure 2-1: RNG --> TRNG, PWMC --> PWM, AC97 --> AC97C, TSDAC --> TSADCC.	RFO
6438ES	Section 7.3 “External Memories” reorganized.	RFO
	New Figure 11-1 “324-ball TFBGA Package Drawing”.	6954
	‘11-layer’ --> ‘12-layer’ in Section 6.2 “Bus Matrix”.	7171
	Section 10.16 “True Random Number Generator (TRNG)” added.	7172
6438FS	1st Page/headers & footers: (text where found) Product Line/Product naming convention changed - **AT91SAM ARM-based MPU / SAM9G45**	Marcom
	Section 5.1 “Power Supplies”, replaced ground pin names by GNDIOM, GNDCORE, GNDANA, GNDIOP, GNDBU, GNDOSC, GNDUTMI. Reorganized text describing GND association to power supply pins.	7322 rfo
	Section 1. “Description”, updated 2nd paragraph, 1st sentence. “...SAM9G45 supports DDR2...”	rfo