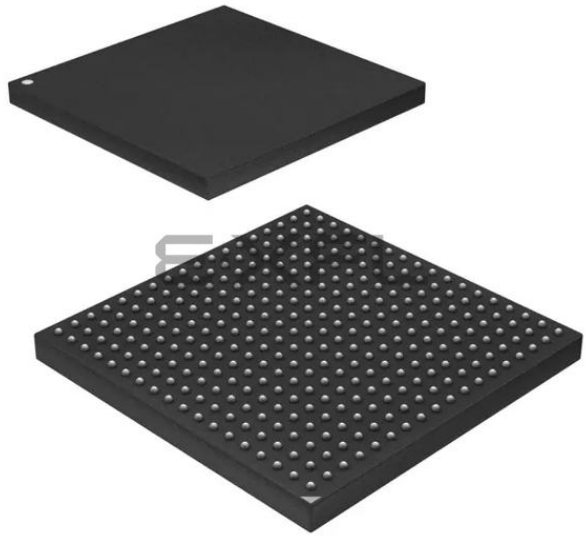

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, LPSDR, DDR2, SDR, SRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD, Touchscreen
Ethernet	10/100Mbps
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	324-TFBGA
Supplier Device Package	324-TFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam9g45c-cu

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
Shutdown, Wakeup Logic					
SHDN	Shut-Down Control	Output		VDDBU	Driven at 0V only. 0: The device is in backup mode 1: The device is running (not in backup mode).
WKUP	Wake-Up Input	Input		VDDBU	Accept between 0V and VDDBU.
ICE and JTAG					
TCK	Test Clock	Input		VDDIOP0	No pull-up resistor, Schmitt trigger
TDI	Test Data In	Input		VDDIOP0	No pull-up resistor, Schmitt trigger
TDO	Test Data Out	Output		VDDIOP0	
TMS	Test Mode Select	Input		VDDIOP0	No pull-up resistor, Schmitt trigger
JTAGSEL	JTAG Selection	Input		VDDBU	Pull-down resistor (15 kΩ).
RTCK	Return Test Clock	Output		VDDIOP0	
Reset/Test					
NRST	Microcontroller Reset[2]	I/O	Low	VDDIOP0	Open-drain output, Pull-Up resistor (100 kΩ), Schmitt trigger
TST	Test Mode Select	Input		VDDBU	Pull-down resistor (15 kΩ), Schmitt trigger
NTRST	Test Reset Signal	Input		VDDIOP0	Pull-Up resistor (100 kΩ), Schmitt trigger
BMS	Boot Mode Select	**Input**		VDDIOP0	must be connected to GND or VDDIOP.
Debug Unit - DBGU					
DRXD	Debug Receive Data	Input		[1]	
DTXD	Debug Transmit Data	Output		[1]	
Advanced Interrupt Controller - AIC					
IRQ	External Interrupt Input	Input		[1]	
FIQ	Fast Interrupt Input	Input		[1]	
PIO Controller - PIOA- PIOB - PIOC - PIOD - PIOE					
PA0 - PA31	Parallel IO Controller A	I/O		[1]	Pulled-up input at reset (100kΩ)[3], Schmitt trigger
PB0 - PB31	Parallel IO Controller B	I/O		[1]	Pulled-up input at reset (100kΩ)[3], Schmitt trigger
PC0 - PC31	Parallel IO Controller C	I/O		[1]	Pulled-up input at reset (100kΩ)[3], Schmitt trigger

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
AC97 Controller - AC97C					
AC97RX	AC97 Receive Signal	Input		(1)	
AC97TX	AC97 Transmit Signal	Output		(1)	
AC97FS	AC97 Frame Synchronization Signal	Output		(1)	
AC97CK	AC97 Clock signal	Input		(1)	
Time Counter - TCx					
TCLKx	TC Channel x External Clock Input	Input		(1)	
TIOAx	TC Channel x I/O Line A	I/O		(1)	
TIOBx	TC Channel x I/O Line B	I/O		(1)	
Pulse Width Modulation Controller - PWM					
PWMx	Pulse Width Modulation Output	Output		(1)	
Serial Peripheral Interface - SPIx_					
SPIx_MISO	Master In Slave Out	I/O		(1)	
SPIx_MOSI	Master Out Slave In	I/O		(1)	
SPIx_SPCK	SPI Serial Clock	I/O		(1)	
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low	(1)	
SPIx_NPCS1-SPIx_NPCS3	SPI Peripheral Chip Select	Output	Low	(1)	
Two-Wire Interface					
TWDx	Two-wire Serial Data	I/O		(1)	
TWCKx	Two-wire Serial Clock	I/O		(1)	
USB Host High Speed Port - UHPHS					
HFSDPA	USB Host Port A Full Speed Data +	Analog		VDDUTMII	
HFSDMA	USB Host Port A Full Speed Data -	Analog		VDDUTMII	
HHSDPA	USB Host Port A High Speed Data +	Analog		VDDUTMII	
HHSDMA	USB Host Port A High Speed Data -	Analog		VDDUTMII	
HFSDPB	USB Host Port B Full Speed Data +	Analog		VDDUTMII	Multiplexed with DFSDP
HFSDMB	USB Host Port B Full Speed Data -	Analog		VDDUTMII	Multiplexed with DFSDM
HHSDPB	USB Host Port B High Speed Data +	Analog		VDDUTMII	Multiplexed with DHSDP
HHSDMB	USB Host Port B High Speed Data -	Analog		VDDUTMII	Multiplexed with DHSDM
USB Device High Speed Port - UDPHS					
DFSDM	USB Device Full Speed Data -	Analog		VDDUTMII	
DFSDP	USB Device Full Speed Data +	Analog		VDDUTMII	
DHSDM	USB Device High Speed Data -	Analog		VDDUTMII	
DHSDP	USB Device High Speed Data +	Analog		VDDUTMII	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
Ethernet 10/100					
ETXCK	Transmit Clock or Reference Clock	Input		(1)	MII only, REFCK in RMII
ERXCK	Receive Clock	Input		(1)	MII only
ETXEN	Transmit Enable	Output		(1)	
ETX0-ETX3	Transmit Data	Output		(1)	ETX0-ETX1 only in RMII
ETXER	Transmit Coding Error	Output		(1)	MII only
ERXDV	Receive Data Valid	Input		(1)	RXDV in MII, CRSDV in RMII
ERX0-ERX3	Receive Data	Input		(1)	ERX0-ERX1 only in RMII
ERXER	Receive Error	Input		(1)	
ECRS	Carrier Sense and Data Valid	Input		(1)	MII only
ECOL	Collision Detect	Input		(1)	MII only
EMDC	Management Data Clock	Output		(1)	
EMDIO	Management Data Input/Output	I/O		(1)	
Image Sensor Interface					
ISI_D0-ISI_D11	Image Sensor Data	Input		VDDIOP2	
ISI_MCK	Image sensor Reference clock	output		VDDIOP2	
ISI_HSYNC	Image Sensor Horizontal Synchro	input		VDDIOP2	
ISI_VSYNC	Image Sensor Vertical Synchro	input		VDDIOP2	
ISI_PCK	Image Sensor Data clock	input		VDDIOP2	
LCD Controller - LCDC					
LCDD0 - LCDD23	LCD Data Bus	Output		VDDIOP1	
LCDVSYNC	LCD Vertical Synchronization	Output		VDDIOP1	
LCDHSYNC	LCD Horizontal Synchronization	Output		VDDIOP1	
LCDDOTCK	LCD Dot Clock	Output		VDDIOP1	
LCDDEN	LCD Data Enable	Output		VDDIOP1	
LCDCC	LCD Contrast Control	Output		VDDIOP1	
LCDPWR	LCD panel Power enable control	Output		VDDIOP1	
LCDMOD	LCD Modulation signal	Output		VDDIOP1	
Touch Screen Analog-to-Digital Converter					
$AD0X_P$	Analog input channel 0 or Touch Screen Top channel	Analog		VDDANA	Multiplexed with AD0
$AD1X_M$	Analog input channel 1 or Touch Screen Bottom channel	Analog		VDDANA	Multiplexed with AD1
$AD2Y_P$	Analog input channel 2 or Touch Screen Right channel	Analog		VDDANA	Multiplexed with AD2
$AD3Y_M$	Analog input channel 3 or Touch Screen Left channel	Analog		VDDANA	Multiplexed with AD3

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Reference Voltage	Comments
GPAD4-GPAD7	Analog Inputs	Analog		VDDANA	
TSADTRG	ADC Trigger	Input		VDDANA	
TSADVREF	ADC Reference	Analog		VDDANA	

Notes:
1. Refer to peripheral multiplexing tables in Section 9.4 “Peripheral Signals Multiplexing on I/O Lines” for these signals.
2. When configured as an input, the NRST pin enables asynchronous reset of the device when asserted low. This allows connection of a simple push button on the NRST pin as a system-user reset.
3. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers. After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals that require to be enabled as Peripheral at reset. This is explicitly indicated in the column “Reset State” of the peripheral multiplexing tables.

Table 4-1. SAM9G45 Pinout for 324-ball BGA Package (Continued)

Pin	Signal Name
C15	D2
C16	GNDIOM
C17	A18
C18	A12
D1	XOUT32
D2	PD20
D3	GNDBU
D4	VDDBU
D5	PC24
D6	PC18
D7	PC13
D8	PC6
D9	NWR1/NBS1
D10	NANDOE
D11	DQM1
D12	D14
D13	D9
D14	D5
D15	D1
D16	VDDIOM1
D17	A11
D18	A10
E1	PD21
E2	TSADVREF
E3	VDDANA
E4	JTAGSEL
E5	TST
E6	PC23
E7	PC16
E8	PC8
E9	PC1

Pin	Signal Name
H6	PE7
H7	PE9
H8	PE10
H9	GNDCORE
H10	GNDIOP
H11	VDDCORE
H12	GNDIOM
H13	GNDIOM
H14	DDR_CS
H15	DDR_WE
H16	DDR_DQM1
H17	DDR_CAS
H18	DDR_NCLK
J1	PE19
J2	PE16
J3	PE14
J4	PE15
J5	PE12
J6	PE17
J7	PE18
J8	PE20
J9	GNDCORE
J10	GNDCORE
J11	GNDIOP
J12	GNDIOM
J13	GNDIOM
J14	DDR_A12
J15	DDR_A13
J16	DDR_CKE
J17	DDR_RAS
J18	DDR_CLK

Pin	Signal Name
M15	DDR_D14
M16	DDR_D15
M17	DDR_A0
M18	DDR_A2
N1	PA3
N2	PA9
N3	PA12
N4	PA15
N5	PA16
N6	PA17
N7	PB18
N8	PD6
N9	PD16
N10	NTRST
N11	PB9
N12	PB24
N13	PB28
N14	DDR_D13
N15	DDR_D8
N16	DDR_D9
N17	DDR_D11
N18	DDR_D12
P1	PA11
P2	PA13
P3	PA19
P4	PA21
P5	PA23
P6	PB12
P7	PB19
P8	PD8
P9	PD28

Pin	Signal Name
U6	PB17
U7	PD7
U8	PD10
U9	PD14
U10	TCK
U11	VDDOSC
U12	GNDOSC
U13	PB10
U14	PB26
U15	HHSDPB/DHSDP
U16	HHSDMB/DHSDM
U17	GNDUTMI
U18	VDDUTMIC
V1	PA31
V2	PB1
V3	PB2
V4	PB5
V5	PB15
V6	PD3
V7	PD5
V8	PD12
V9	PD17
V10	TDO
V11	XOUT
V12	XIN
V13	VDDPLLUTMI
V14	VDDIOP2
V15	HFSDPB/DFSDP
V16	HFSDMB/DFSDM
V17	VDDUTMII
V18	VBG

6. Processor and Architecture

6.1 ARM926EJ-S Processor

- RISC Processor Based on ARM v5TEJ Architecture with Jazelle technology for Java acceleration
- Two Instruction Sets
  - ARM High-performance 32-bit Instruction Set
  - Thumb High Code Density 16-bit Instruction Set
- DSP Instruction Extensions
- 5-Stage Pipeline Architecture:
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)
  - Data Memory (M)
  - Register Write (W)
- 32-KByte Data Cache, 32-KByte Instruction Cache
  - Virtually-addressed 4-way Associative Cache
  - Eight words per line
  - Write-through and Write-back Operation
  - Pseudo-random or Round-robin Replacement
- Write Buffer
  - Main Write Buffer with 16-word Data Buffer and 4-address Buffer
  - DCache Write-back Buffer with 8-word Entries and a Single Address Entry
  - Software Control Drain
- Standard ARM v4 and v5 Memory Management Unit (MMU)
  - Access Permission for Sections
  - Access Permission for large pages and small pages can be specified separately for each quarter of the page
  - 16 embedded domains
- Bus Interface Unit (BIU)
  - Arbitrates and Schedules AHB Requests
  - Separate Masters for both instruction and data access providing complete Matrix system flexibility
  - Separate Address and Data Buses for both the 32-bit instruction interface and the 32-bit data interface
  - On Address and Data Buses, data can be 8-bit (Bytes), 16-bit (Half-words) or 32-bit (Words)
- TCM Interface

6.2 Bus Matrix

- 12-layer Matrix, handling requests from 11 masters
- Programmable Arbitration strategy
  - Fixed-priority Arbitration
  - Round-Robin Arbitration, either with no default master, last accessed default master or fixed default master
- Burst Management
  - Breaking with Slot Cycle Limit Support
  - Undefined Burst Length Support
- One Address Decoder provided per Master
  - Three different slaves may be assigned to each decoded memory area: one for internal ROM boot, one for internal flash boot, one after remap
- Boot Mode Select
  - Non-volatile Boot Memory can be internal ROM or external memory on EBI_NCS0
  - Selection is made by General purpose NVM bit sampled at reset
- Remap Command
  - Allows Remapping of an Internal SRAM in Place of the Boot Non-Volatile Memory (ROM or External Flash)
  - Allows Handling of Dynamic Exception Vectors

6.2.1 Matrix Masters

The Bus Matrix of the SAM9G45 manages Masters, thus each master can perform an access concurrently with others, depending on whether the slave it accesses is available.

Each Master has its own decoder, which can be defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 6-1. List of Bus Matrix Masters

Master 0	ARM926™ Instruction
Master 1	ARM926 Data
Master 2	Peripheral DMA Controller (PDC)
Master 3	USB HOST OHCI
Master 4	DMA
Master 5	DMA
Master 6	ISI Controller DMA
Master 7	LCD DMA
Master 8	Ethernet MAC DMA
Master 9	USB Device High Speed DMA
Master 10	USB Host High Speed EHCI DMA

6.2.2 Matrix Slaves

Each Slave has its own arbiter, thus allowing a different arbitration per Slave to be programmed.

Table 6-2. List of Bus Matrix Slaves

Slave 0	Internal SRAM
Slave 1	Internal ROM
	USB OHCI
	USB EHCI
	UDP High Speed RAM
	LCD User Interface
Slave 2	DDR Port 0
Slave 3	DDR Port 1
Slave 4	DDR Port 2
Slave 5	DDR Port 3
Slave 6	External Bus Interface
Slave 7	Internal Peripherals

6.2.3 Masters to Slaves Access

All the Masters can normally access all the Slaves. However, some paths do not make sense, such as allowing access from the Ethernet MAC to the internal peripherals. Thus, these paths are forbidden or simply not wired, and shown “-” in the following tables.

The four DDR ports are connected differently according to the application device.

The user can disable the DDR multi-port in the DDR multi-port Register (bit DDRMP_DIS) in the Chip Configuration User Interface.

- When the DDR multi-port is enabled (DDRMP_DIS=0), the ARM instruction and data are respectively connected to DDR Port 0 and DDR Port 1. The other masters share DDR Port 2 and DDR Port 3.
- When the DDR multi-port is disabled (DDRMP_DIS=1), DDR Port 1 is dedicated to the LCD controller. The remaining masters share DDR Port 2 and DDR Port 3.

6.6 Debug and Test Features

- ARM926 Real-time In-circuit Emulator
  - Two real-time Watchpoint Units
  - Two Independent Registers: Debug Control Register and Debug Status Register
  - Test Access Port Accessible through JTAG Protocol
  - Debug Communications Channel
- Debug Unit
  - Two-pin UART
  - Debug Communication Channel Interrupt Handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on All Digital Pins.

- Internal SRAM B is the ARM926EJ-S Data TCM. The user can map this SRAM block anywhere in the ARM926 data memory space using CP15 instructions. This SRAM block is also accessible by the ARM926 Data Master and by the AHB Masters through the AHB bus.
- Internal SRAM C is only accessible by all the AHB Masters. After reset and until the Remap Command is performed, this SRAM block is accessible through the AHB bus at address 0x0030 0000 by all the AHB Masters. After Remap, this SRAM block also becomes accessible through the AHB bus at address 0x0 by the ARM926 Instruction and the ARM926 Data Masters.

Within the 64 Kbyte SRAM size available, the amount of memory assigned to each block is software programmable according to Table 7-1.

Table 7-1. ITCM and DTCM Memory Configuration

SRAM A ITCM size (KBytes) seen at 0x100000 through AHB	SRAM B DTCM size (KBytes) seen at 0x200000 through AHB	SRAM C (KBytes) seen at 0x300000 through AHB
0	0	64
0	64	0
32	32	0

7.2.3 Internal ROM

The SAM9G45 embeds an Internal ROM, which contains the Boot ROM and SAM-BA program.

At any time, the ROM is mapped at address 0x0040 0000. It is also accessible at address 0x0 (BMS =1) after the reset and before the Remap Command.

7.2.4 Boot Strategies

The system always boots at address 0x0. To ensure maximum boot possibilities the memory layout can be changed with two parameters.

REMAP allows the user to layout the internal SRAM bank to 0x0 to ease the development. This is done by software once the system has boot.

BMS allows the user to lay out to 0x0, when convenient, the ROM or an external memory. This is done by a hardware way at reset.

Note: All the memory blocks can always be seen at their specified base addresses that are not concerned by these parameters.

The SAM9G45 Bus Matrix manages a boot memory that depends on the level on the pin BMS at reset. The internal memory area mapped between address 0x0 and 0x000F FFFF is reserved to this effect.

If BMS is detected at 1, the boot memory is the embedded ROM.

If BMS is detected at 0, the boot memory is the memory connected on the Chip Select 0 of the External Bus Interface.

7.2.4.1 BMS = 1, boot on embedded ROM

The system boots on Boot Program.

- Boot on on-chip RC
- Enable the 32768 Hz oscillator
- Auto baudrate detection
- Downloads and runs an application from external storage media into internal SRAM
- Downloaded code size depends on embedded SRAM size
- Automatic detection of valid application

- Bootloader on a non-volatile memory
  - SPI DataFlash/Serial Flash connected on NPCS0 of the SPI0
  - SDCard
  - Nand Flash
  - EEPROM connected on TWI0
- SAM-BA Boot in case no valid program is detected in external NVM, supporting
  - Serial communication on a DBGU
  - USB Device HS Port

7.2.4.2 BMS = 0, boot on external memory

- Boot on on-chip RC
- Boot with the default configuration for the Static Memory Controller, byte select mode, 16-bit data bus, Read/Write controlled by Chip Select, allows boot on 16-bit non-volatile memory.

For optimization purpose, nothing else is done. To speed up the boot sequence user programmed software should perform a complete configuration:

- Enable the 32768 Hz oscillator if best accuracy needed
- Program the PMC (main oscillator enable or bypass mode)
- Program and Start the PLL
- Reprogram the SMC setup, cycle, hold, mode timings registers for EBI CS0 to adapt them to the new clock
- Switch the main clock to the new value

7.3 External Memories

The SAM9G45 features a Multi-port DDR2 Interface and an External Bus Interface allowing to connect to a wide range of external memories and to any parallel peripheral.

7.3.1 DDRSDRC0 Multi-port DDRSDR Controller

Four AHB Interfaces, Management of All Accesses Maximizes Memory Bandwidth and Minimizes Transaction Latency.

- Supports AHB Transfers:
  - Word, Half Word, Byte Access.
- Supports DDR2, LPDDR
- Numerous Configurations Supported
  - 2K, 4K, 8K, 16K Row Address Memory Parts
  - DDR2 with Four Internal Banks
  - DDR2/LPDDR with 16-bit Data Path
  - One Chip Select for DDR2/LPDDR Device (256 Mbytes Address Space)
- Programming Facilities
  - Multibank Ping-pong Access (Up to 4 Banks Opened at Same Time = Reduces Average Latency of Transactions)
  - Timing Parameters Specified by Software
  - Automatic Refresh Operation, Refresh Rate is Programmable
  - Automatic Update of DS, TCR and PASR Parameters
- Energy-saving Capabilities
  - Self-refresh, Power-down and Deep Power Modes Supported
- Power-up Initialization by Software
- CAS Latency of 2, 3 Supported
- Reset function supported (DDR2)
- Auto Precharge Command Not Used

- SDRAM Power-up Initialization by Software
- CAS Latency of 2, 3 Supported
- Auto Precharge Command Not Used
- SDR-SDRAM with 16-bit Datapath and Eight Columns Not Supported
    - Clock Frequency Change in Precharge Power-down Mode Not Supported

7.3.2.3 NAND Flash Error Corrected Code Controller

- Tracking the accesses to a NAND Flash device by triggering on the corresponding chip select
- Single bit error correction and 2-bit Random detection.
- Automatic Hamming Code Calculation while writing
    - ECC value available in a register
- Automatic Hamming Code Calculation while reading
    - Error Report, including error flag, correctable error flag and word address being detected erroneous
    - Support 8- or 16-bit NAND Flash devices with 512-, 1024-, 2048- or 4096-bytes pages

8.3 Reset Controller

The Reset Controller is based on two Power-on-Reset cells, one on VDDBU and one on VDDCORE.

The Reset Controller is capable to return to the software the source of the last reset, either a general reset (VDDBU rising), a wake-up reset (VDDCORE rising), a software reset, a user reset or a watchdog reset.

The Reset Controller controls the internal resets of the system and the NRST pin output. It is capable to shape a reset signal for the external devices, simplifying to a minimum connection of a push-button on the NRST pin to implement a manual reset.

The configuration of the Reset Controller is saved as supplied on VDDBU.

8.4 Shut Down Controller

The Shut Down Controller is supplied on VDDBU and allows a software-controllable shut down of the system through the pin SHDN. An input change of the WKUP pin or an alarm releases the SHDN pin, and thus wakes up the system power supply.

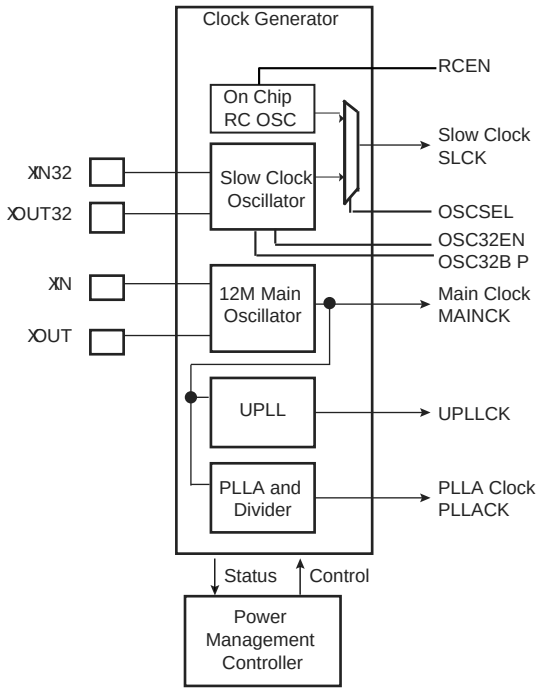
8.5 Clock Generator

The Clock Generator is made up of:

- One Low Power 32768 Hz Slow Clock Oscillator with bypass mode
- One Low-Power RC oscillator
- One 12 MHz Main Oscillator, which can be bypassed
- One 400 to 800 MHz programmable PLLA, capable to provide the clock MCK to the processor and to the peripherals. This PLL has an input divider to offer a wider range of output frequencies from the 12 MHz input, the only limitation being the lowest input frequency shall be higher or equal to 2 MHz.

The USB Device and Host HS Clocks are provided by a the dedicated UTMI PLL (UPLL) embedded in the UTMI macro.

Figure 8-2. Clock Generator Block Diagram



- Wait internal RC Startup Time for clock stabilization (software loop).
- Switch from 32768 Hz oscillator to internal RC oscilllator by setting the bit OSCSEL to 0.
- Wait 5 slow clock cycles for internal resynchronization.
- Disable the 32768Hz oscillator by setting the bit OSC32EN to 0.

8.7 Power Management Controller

The Power Management Controller provides all the clock signals to the system.

PMC input clocks:

- UPLLCK: From UTMI PLL
- PLLACK From PLLA
- SLCK: slow clock from OSC32K or internal RC OSC
- MAINCK: from 12 MHz external oscillator

PMC output clocks

- Processor Clock PCK
- Master Clock MCK, in particular to the Matrix and the memory interfaces. The divider can be 1,2,3 or 4
- DDR system clock equal to 2xMCK

Note: DDR system clock is not available when Master Clock (MCK) equals Processor Clock (PCK).

- USB Host EHCI High speed clock (UPLLCK)
- USB OHCI clocks (UHP48M and UHP12M)
- Independent peripheral clocks, typically at the frequency of MCK
- Two programmable clock outputs: PCK0 and PCK1

This allows the software control of five flexible operating modes:

- Normal Mode, processor and peripherals running at a programmable frequency
- Idle Mode, processor stopped waiting for an interrupt
- Slow Clock Mode, processor and peripherals running at low frequency
- Standby Mode, mix of Idle and Backup Mode, peripheral running at low frequency, processor stopped waiting for an interrupt
- Backup Mode, Main Power Supplies off, VDDBU powered by a battery

9. Peripherals

9.1 Peripheral Mapping

As shown in Figure 7-1, the Peripherals are mapped in the upper 256 Mbytes of the address space between the addresses 0xFFF7 8000 and 0xFFFC FFFF.

Each User Peripheral is allocated 16K bytes of address space.

9.2 Peripheral Identifiers

Table 9-1 defines the Peripheral Identifiers of the SAM9G45. A peripheral identifier is required for the control of the peripheral interrupt with the Advanced Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 9-1. SAM9G45 Peripheral Identifiers

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
0	**AIC**	Advanced Interrupt Controller	FIQ
1	**SYSC**	System Controller Interrupt	
2	**PIOA**	Parallel I/O Controller A,	
3	**PIOB**	Parallel I/O Controller B	
4	**PIOC**	Parallel I/O Controller C	
5	**PIOD/PIOE**	Parallel I/O Controller D/E	
6	**TRNG**	True Random Number Generator	
7	**US0**	USART 0	
8	**US1**	USART 1	
9	**US2**	USART 2	
10	**US3**	USART 3	
11	**MCI0**	High Speed Multimedia Card Interface 0	
12	**TWI0**	Two-Wire Interface 0	
13	**TWI1**	Two-Wire Interface 1	
14	**SPI0**	Serial Peripheral Interface	
15	**SPI1**	Serial Peripheral Interface	
16	**SSC0**	Synchronous Serial Controller 0	
17	**SSC1**	Synchronous Serial Controller 1	
18	**TC0..TC5**	Timer Counter 0,1,2,3,4,5	
19	**PWM**	Pulse Width Modulation Controller	
20	**TSADCC**	Touch Screen ADC Controller	
21	**DMA**	DMA Controller	
22	**UHPHS**	USB Host High Speed	
23	**LCDC**	LCD Controller	
24	**AC97C**	AC97 Controller	
25	**EMAC**	Ethernet MAC	
26	**ISI**	Image Sensor Interface	
27	**UDPHS**	USB Device High Speed	
29	**MCI1**	High Speed Multimedia Card Interface 1	
30	**Reserved**		
31	**AIC**	Advanced Interrupt Controller	IRQ

9.4.1 PIO Controller A Multiplexing

Table 9-2. Multiplexing on PIO Controller A (PIOA)

I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PA0	MCI0_CK	TCLK3	I/O	VDDIOP0		
PA1	MCI0_CDA	TIOA3	I/O	VDDIOP0		
PA2	MCI0_DA0	TIOB3	I/O	VDDIOP0		
PA3	MCI0_DA1	TCKL4	I/O	VDDIOP0		
PA4	MCI0_DA2	TIOA4	I/O	VDDIOP0		
PA5	MCI0_DA3	TIOB4	I/O	VDDIOP0		
PA6	MCI0_DA4	ETX2	I/O	VDDIOP0		
PA7	MCI0_DA5	ETX3	I/O	VDDIOP0		
PA8	MCI0_DA6	ERX2	I/O	VDDIOP0		
PA9	MCI0_DA7	ERX3	I/O	VDDIOP0		
PA10	ETX0		I/O	VDDIOP0		
PA11	ETX1		I/O	VDDIOP0		
PA12	ERX0		I/O	VDDIOP0		
PA13	ERX1		I/O	VDDIOP0		
PA14	ETXEN		I/O	VDDIOP0		
PA15	ERXDV		I/O	VDDIOP0		
PA16	ERXER		I/O	VDDIOP0		
PA17	ETXCK		I/O	VDDIOP0		
PA18	EMDC		I/O	VDDIOP0		
PA19	EMDIO		I/O	VDDIOP0		
PA20	TWD0		I/O	VDDIOP0		
PA21	TWCK0		I/O	VDDIOP0		
PA22	MCI1_CDA	SCK3	I/O	VDDIOP0		
PA23	MCI1_DA0	RTS3	I/O	VDDIOP0		
PA24	MCI1_DA1	CTS3	I/O	VDDIOP0		
PA25	MCI1_DA2	PWM3	I/O	VDDIOP0		
PA26	MCI1_DA3	TIOB2	I/O	VDDIOP0		
PA27	MCI1_DA4	ETXER	I/O	VDDIOP0		
PA28	MCI1_DA5	ERXCK	I/O	VDDIOP0		
PA29	MCI1_DA6	ECRS	I/O	VDDIOP0		
PA30	MCI1_DA7	ECOL	I/O	VDDIOP0		
PA31	MCI1_CK	PCK0	I/O	VDDIOP0		

9.4.3 PIO Controller C Multiplexing

Table 9-4. Multiplexing on PIO Controller C (PIOC)

I/O Line	Peripheral A	Peripheral B	Reset State	Power Supply	Function	Comments
PC0	DQM2		DQM2	VDDIOM1		
PC1	DQM3		DQM3	VDDIOM1		
PC2	A19		A19	VDDIOM1		
PC3	A20		A20	VDDIOM1		
PC4	A21/NANDALE		A21	VDDIOM1		
PC5	A22/NANDCLE		A22	VDDIOM1		
PC6	A23		A23	VDDIOM1		
PC7	A24		A24	VDDIOM1		
PC8	CFCE1		I/O	VDDIOM1		
PC9	CFCE2	RTS2	I/O	VDDIOM1		
PC10	NCS4/CFCS0	TCLK2	I/O	VDDIOM1		
PC11	NCS5/CFCS1	CTS2	I/O	VDDIOM1		
PC12	A25/CFRNW		A25	VDDIOM1		
PC13	NCS2		I/O	VDDIOM1		
PC14	NCS3/NANDCS		I/O	VDDIOM1		
PC15	NWAIT		I/O	VDDIOM1		
PC16	D16		I/O	VDDIOM1		
PC17	D17		I/O	VDDIOM1		
PC18	D18		I/O	VDDIOM1		
PC19	D19		I/O	VDDIOM1		
PC20	D20		I/O	VDDIOM1		
PC21	D21		I/O	VDDIOM1		
PC22	D22		I/O	VDDIOM1		
PC23	D23		I/O	VDDIOM1		
PC24	D24		I/O	VDDIOM1		
PC25	D25		I/O	VDDIOM1		
PC26	D26		I/O	VDDIOM1		
PC27	D27		I/O	VDDIOM1		
PC28	D28		I/O	VDDIOM1		
PC29	D29		I/O	VDDIOM1		
PC30	D30		I/O	VDDIOM1		
PC31	D31		I/O	VDDIOM1		

10. Embedded Peripherals

10.1 Serial Peripheral Interface (SPI)

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to MCK
  - The chip select line may be left active to speed up transfers on the same device

10.2 Two Wire Interface (TWI)

- Compatibility with standard two-wire serial memory
- One, two or three bytes for slave address
- Sequential read/write operations
- Supports either master or slave modes
- Compatible with Standard Two-wire Serial Memories
- Master, Multi-master and Slave Mode Operation
- Bit Rate: Up to 400 Kbits
- General Call Supported in Slave mode
- Connection to Peripheral DMA Controller (PDC) Channel Capabilities Optimizes Data Transfers in Master Mode Only
  - One Channel for the Receiver, One Channel for the Transmitter
  - Next Buffer Support

10.3 Universal Synchronous Asynchronous Receiver Transmitter (USART)

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB- or LSB-first
  - Optional break generation and detection
  - By 8 or by-16 over-sampling receiver frequency
  - Hardware handshaking RTS-CTS
  - Receiver time-out and transmitter timeguard
  - Optional Multi-drop Mode with address generation and detection
  - Optional Manchester Encoding

- 1, 2 bits per pixel (palletized), 4 bits per pixel (non-palletized) for mono STN
- 1, 2, 4, 8 bits per pixel (palletized), 16 bits per pixel (non-palletized) for color STN
- 1, 2, 4, 8 bits per pixel (palletized), 16, 24 bits per pixel (non-palletized) for TFT
- Single clock domain architecture
- Resolution supported up to 2048 x 2048

10.12 Touch Screen Analog-to-Digital Converter (TSADC)

- 8-channel ADC
- Support 4-wire resistive Touch Screen
- 10-bit 384 Ksamples/sec. Successive Approximation Register ADC
- -3/+3 LSB Integral Non Linearity, -2/+2 LSB Differential Non Linearity
- Integrated 8-to-1 multiplexer, offering eight independent 3.3V analog inputs
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger sources
    - Hardware or software trigger
    - External trigger pin
- Sleep Mode and conversion sequencer
    - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels

10.13 Ethernet 10/100 MAC (EMAC)

- Compatibility with IEEE Standard 802.3
- 10 and 100 MBits per second data throughput capability
- Full- and half-duplex operations
- MII or RMII interface to the physical layer
- Register Interface to address, data, status and control registers
- DMA Interface, operating as a master on the Memory Controller
- Interrupt generation to signal receive and transmit completion
- 128-byte transmit and 128-byte receive FIFOs
- Automatic pad and CRC generation on transmitted frames
- Address checking logic to recognize four 48-bit addresses
- Supports promiscuous mode where all valid frames are copied to memory
- Supports physical layer management through MDIO interface
- Supports Wake On Lan. The receiver supports Wake on LAN by detecting the following events on incoming receive frames:
    - Magic packet
    - ARP request to the device IP address
    - Specific address 1 filter match
    - Multicast hash filter match

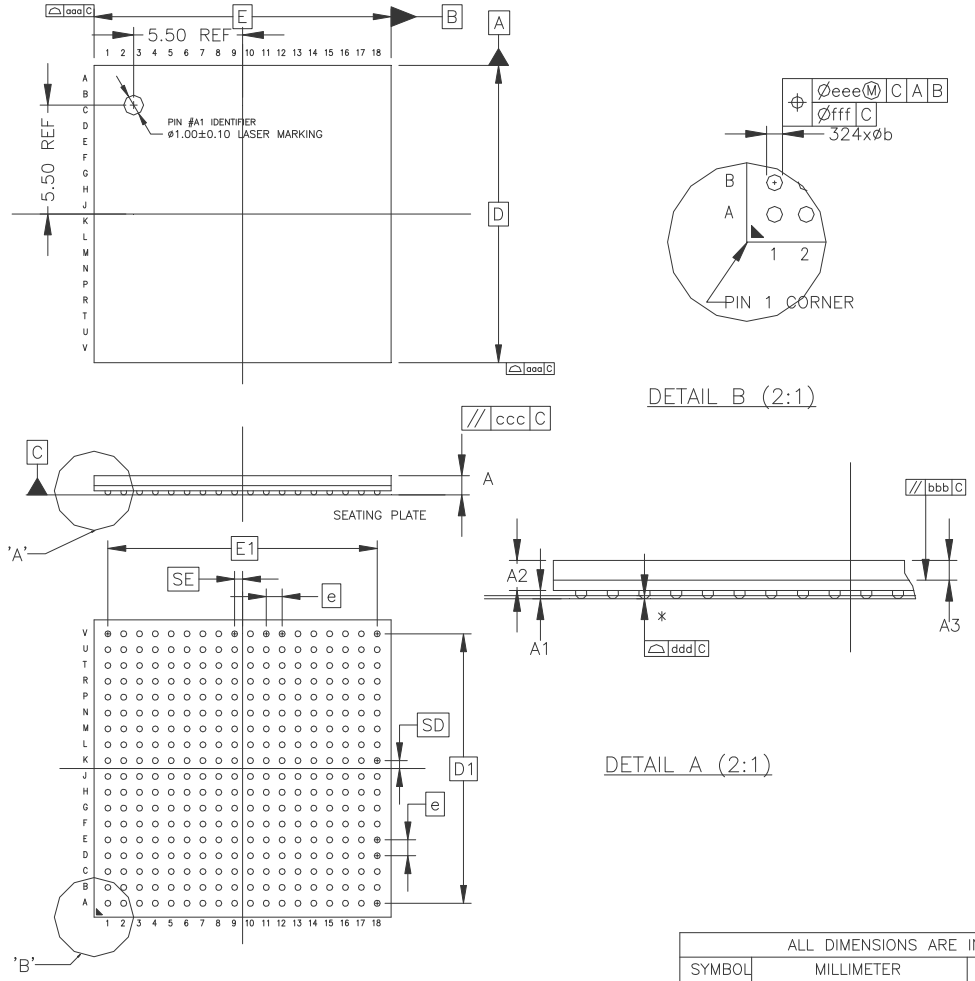
10.14 Image Sensor Interface (ISI)

- ITU-R BT. 601/656 8-bit mode external interface support
- Support for ITU-R BT.656-4 SAV and EAV synchronization
- Vertical and horizontal resolutions up to 2048 x 2048
- Preview Path up to 640*480
- Support for packed data formatting for YCbCr 4:2:2 formats

11. Mechanical Characteristics

11.1 Package Drawings

Figure 11-1. 324-ball TFBGA Package Drawing



NOTES :

1. DIMENSIONS ARE IN MILLIMETERS.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE CONTACT BALLS.
3. DIMENSION 'A' INCLUDES STANDOFF HEIGHT 'A1', PACKAGE BODY THICKNESS AND LID HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES.
4. DIMENSION 'b' IS MEASURED AT THE MAXIMUM BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
5. PARALLELISM MEASURMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

ALL DIMENSIONS ARE IN MILLIMETERS.						
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.20	---	----	0.0472
A1	0.16	0.21	0.26	0.0063	0.0083	0.0102
A2	0.72	0.76	0.80	0.0283	0.0299	0.0315
A3	0.50 BASIC			0.0197 BASIC		
D	14.95	15.00	15.05	0.5886	0.5906	0.5926
D1	13.60 BASIC			0.5354 BASIC		
E	14.95	15.00	15.05	0.5866	0.5906	0.5926
E1	13.60 BASIC			0.5354 BASIC		
SD	0.40 BASIC			0.0157 BASIC		
SE	0.40 BASIC			0.0157 BASIC		
e	0.80 BASIC			0.0315		
b	0.25	0.30	0.35	0.0098	0.0118	0.0138
aaa	0.15			0.0059		
bbb	0.20			0.0079		
ccc	0.20			0.0079		
ddd	0.08			0.0031		
eee	0.15			0.0059		
fff	0.08			0.0031		