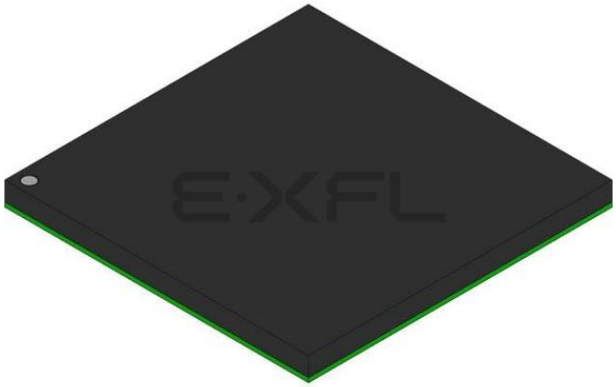

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.42GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BCBGA, FCCBGA
Supplier Device Package	360-FCCBGA (25x25)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc7447ahx1420lb

  - Guarantees sequential programming model (precise exception model)
  - Monitors all dispatched instructions and retires them in order
  - Tracks unresolved branches and flushes instructions after a mispredicted branch
  - Retires as many as three instructions per clock cycle
- Separate on-chip L1 instruction and data caches (Harvard architecture)
  - 32-Kbyte, eight-way set-associative instruction and data caches
  - Pseudo least-recently-used (PLRU) replacement algorithm
  - 32-byte (eight-word) L1 cache block
  - Physically indexed/physical tags
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - Instruction cache can provide four instructions per clock cycle; data cache can provide four words per clock cycle
  - Caches can be disabled in software.
  - Caches can be locked in software.
  - MESI data cache coherency maintained in hardware
  - Separate copy of data cache tags for efficient snooping
  - Parity support on cache and tags
  - No snooping of instruction cache except for **icbi** instruction
  - Data cache supports AltiVec LRU and transient instructions
  - Critical double- and/or quad-word forwarding is performed as needed. Critical quad-word forwarding is used for AltiVec loads and instruction fetches. Other accesses use critical double-word forwarding.
- Level 2 (L2) cache interface
  - On-chip, 512-Kbyte, eight-way set-associative unified instruction and data cache
  - Fully pipelined to provide 32 bytes per clock cycle to the L1 caches
  - A total 9-cycle load latency for an L1 data cache miss that hits in L2
  - Cache write-back or write-through operation programmable on a per-page or per-block basis
  - 64-byte, two-sectored line size
  - Parity support on cache
- Separate memory management units (MMUs) for instructions and data
  - 52-bit virtual address, 32- or 36-bit physical address
  - Address translation for 4-Kbyte pages, variable-sized blocks, and 256-Mbyte segments
  - Memory programmable as write-back/write-through, caching-inhibited/caching-allowed, and memory coherency enforced/memory coherency not enforced on a page or block basis
  - Separate IBATs and DBATs (eight each) also defined as SPRs
  - Separate instruction and data translation lookaside buffers (TLBs)
    - Both TLBs are 128-entry, two-way set-associative, and use an LRU replacement algorithm.

Table 1. Microarchitecture Comparison (continued)

Microarchitectural Specs	MPC7447A	MPC7447	MPC7445	MPC7441
BHT size	2K-entry			
Link stack depth	8			
Unresolved branches supported	3			
Branch taken penalty (BTIC hit)	1			
Minimum misprediction penalty	6			
Execution Unit Timings (Latency-Throughput)				
Aligned load (integer, float, vector)	3-1, 4-1, 3-1			
Misaligned load (integer, float, vector)	4-2, 5-2, 4-2			
L1 miss, L2 hit latency	9 data/13 instruction			
SFX (aDd Sub, Shift, Rot, Cmp, logicals)	1-1			
Integer multiply (32×8, 32×16, 32×32)	3-1, 3-1, 4-2			
Scalar float	5-1			
VSFX (vector simple)	1-1			
VCFX (vector complex)	4-1			
VFPU (vector float)	4-1			
VPER (vector permute)	2-1			
MMUs				
TLBs (instruction and data)	128-entry, 2-way			
Tablewalk mechanism	Hardware + software			
Instruction BATs/data BATs	8/8	8/8	8/8	4/4
L1 I Cache/D Cache Features				
Size	32K/32K			
Associativity	8-way			
Locking granularity	Way			
Parity on Instruction cache	Word			
Parity on data cache	Byte			
Number of data cache misses (load/store)	5/1			
Data stream touch engines	4 streams			
On-Chip Cache Features				
Cache level	L2			
Size/associativity	512-Kbyte/8-way		256-Kbyte/8-way	
Access width	256 bits			

Storage temperature range	T_{stg}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 4. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution**: V_{DD}/AV_{DD} must not exceed OV_{DD} by more than 1.0 V during normal operation; this limit may be exceeded for a maximum of 20 ms during the power-on reset and power-down sequences.
3. **Caution**: OV_{DD} must not exceed V_{DD}/AV_{DD} by more than 2.0 V during normal operation; this limit may be exceeded for a maximum of 20 ms during the power-on reset and power-down sequences.
4. BVSEL must be set to 0, such that the bus is in 1.8-V mode.
5. BVSEL must be set to $\overline{\text{HRESET}}$ or 1, such that the bus is in 2.5-V mode.
6. **Caution**: $V_{in1(xef(i)1er)2}$ 1eref4.8(s)-1 mo5.45 s83 .8(odcn183 .8(odcn183 .8(odcn183 .8(ocn183 .8(ocn.783824.5(1.9191 10in)Tjt0

Figure 2 shows the undershoot and overshoot voltage on the MPC7447A.

Figure 2. Overshoot/Undershoot Voltage

The MPC7447A provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7447A core voltage must always be provided at the nominal voltage (see Table 4) or at the supported derated voltage (see Section 5.3, “Voltage and Frequency Derating”). The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal $\overline{\text{HRESET}}$. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} power pins. Table 3 provides the input threshold voltage settings. Because these settings may change in future products, it is recommended that BVSEL be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future if necessary.

Table 6 provides the DC electrical

Typical	4.1	4.0	3.2	4.0	W	1, 2

Notes:

1. These values specify the power consumption for the core power supply (V_{DD}) at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include I/O supply power (OV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} power is system dependent but is typically < 5% of V_{DD} power. Worst case power consumption for AV_{DD} < 3 mW.
2. Typical power is an average value measured at the nominal recommended V

5.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC7447A. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Section 5.2.1, "Clock AC Specifications," and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:4] signals, and can be dynamically modified using dynamic frequency switching (DFS). Parts are sold by maximum processor core frequency; see Section 11, "Ordering Information," for information on ordering parts. DFS is described in Section 9.8.5, "Dynamic Frequency Switching (DFS)."

5.2.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications as defined in Figure 3 and represents the tested operating frequencies of the devices. The maximum system bus frequency, f_{SYSCLK}, given in Table 8, is considered a practical maximum in a typical single-processor system. The actual maximum SYSCLK frequency for any application of the MPC7447A will be a function of the AC timings of the MPC7447A, the AC timings for the system controller, bus loading, printed-circuit board topology, trace lengths, and so forth, and may be less than the value given in Table 8.

NOTE

The core frequency information in this table applies when operating the device at the nominal core voltage indicated in Table 4. For core frequency specifications at derated core voltage conditions, see Section 5.3, "Voltage and Frequency Derating."

5.2.2 Processor Bus AC Specifications

Table 9 provides the processor bus AC timing specifications for the MPC7447A as defined in Figure 4 and Figure 5.

Table 9. Processor Bus AC Timing Specifications[1]

At recommended operating conditions. See

Figure 8 provides the JTAG clock input timing diagram.

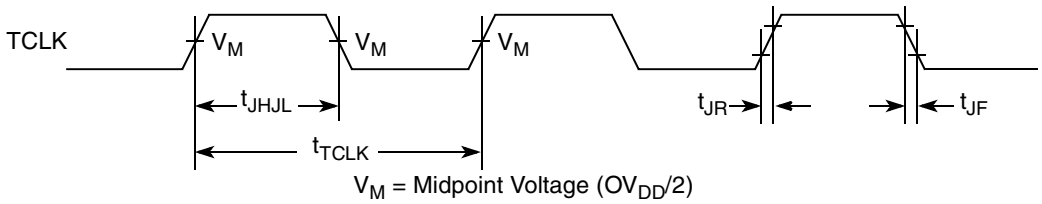


Figure 8. JTAG Clock Input Timing Diagram

Figure 9 provides the $\overline{\text{TRST}}$ timing diagram.

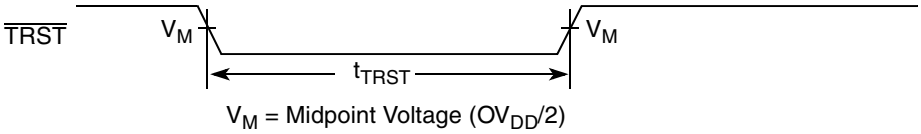


Figure 9. $\overline{\text{TRST}}$ Timing Diagram

Figure 10 provides the boundary-scan timing diagram.

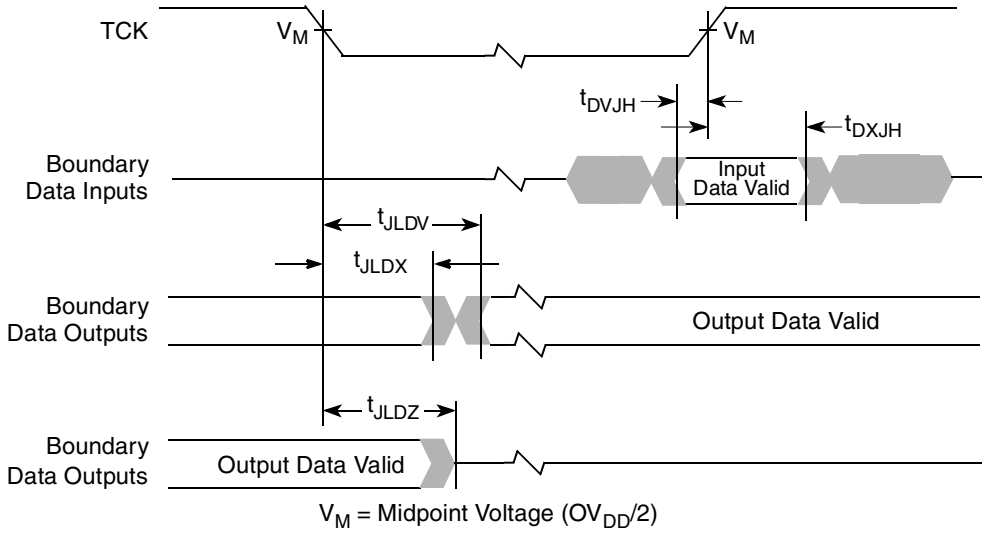


Figure 10. Boundary-Scan Timing Diagram

6 Pin Assignments

Figure 12 (in Part A) shows the pinout of the MPC7447A, 360 high coefficient of thermal expansion ceramic ball grid array (HCTE) package as viewed from the top surface. Part B shows the side profile of the HCTE package to indicate the direction of the top surface view.

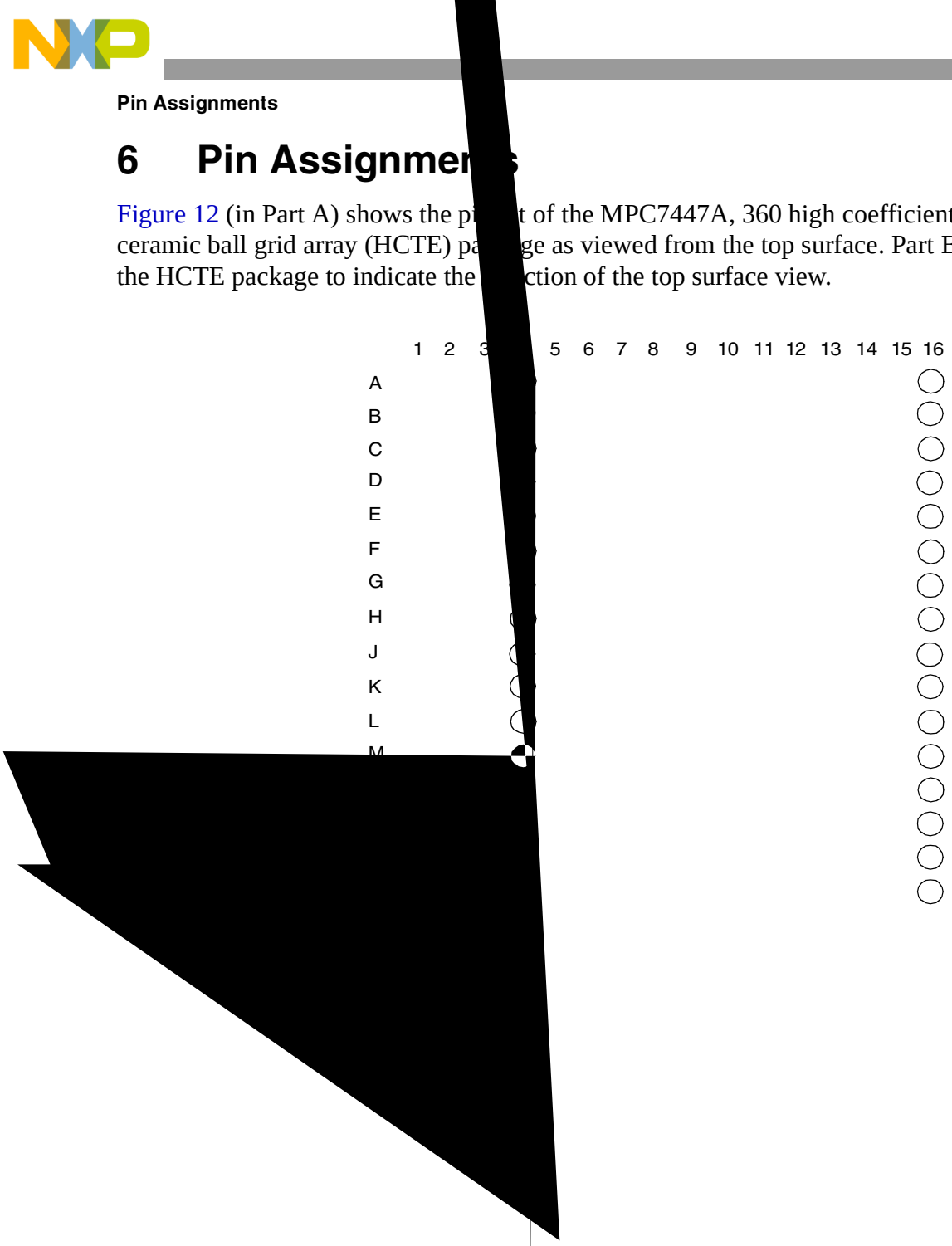


Figure 12. Pinout of the MPC7447A, 360 HCTE Package as Viewed from the Top Surface

7 Pinout Listings

Table 12 provides the pinout listing for the MPC7447A, 360 HCTE package. The pinouts of the MPC7447A and MPC7447 are pin compatible, but there have been some changes. An MPC7447A may be populated on a board designed for a MPC7447 provided all pins defined as ‘no connect’ for the MPC7447 are unterminated as required by the *MPC7457 RISC Microprocessor Hardware Specifications*. The MPC7447A uses pins previously marked ‘no connect’ for the temperature diode pins and for additional power and ground connections. Because these ‘no connect’ pins in the MPC7447 360 pin package are not driven in functional mode, an MPC7447 can be populated in an MPC7447A board. See Section 9.4, “Connection Recommendations,” for additional information.

NOTE

Caution must be exercised when performing boundary scan test operations on a board designed for an MPC7447A but populated with an MPC7447. This is because in the MPC7447 it is possible to drive the latches associated with the former ‘no connect’ pins in the MPC7447, potentially causing contention on those pins. To prevent this, ensure that these pins are not connected on the board or, if they are connected, ensure that the states of internal MPC7447 latches do not cause these pins to be driven during board testing.

NOTE

This pinout is not compatible with the MPC750, MPC7400, or MPC7410 360 BGA and LGA package.

Table 12. Pinout Listing for the MPC7447A, 360 HCTE Package

Signal Name	Pin Number	Active	I/O	I/F Select[1]	Notes
A[0:35]	E11, H1, C11, G3, F10, L2, D11, D1, C10, G2, D12, L3, G4, T2, F4, V1, J4, R2, K5, W2, J2, K4, N4, J3, M5, P5, N3, T1, V2, U1, N5, W1, B12, C4, G10, B11	High	I/O	BVSEL	2
$\overline{\text{AACK}}$	R1	Low	Input	BVSEL	
AP[0:4]	C1, E3, H6, F5, G7	High	I/O	BVSEL	2
$\overline{\text{ARTRY}}$	N2	Low	I/O	BVSEL	3
AV_{DD}	A8	—	Input	N/A	
$\overline{\text{BG}}$	M1	Low	Input	BVSEL	
$\overline{\text{BMODE0}}$	G9	Low	Input	BVSEL	4
$\overline{\text{BMODE1}}$	F8	Low	Input	BVSEL	5
$\overline{\text{BR}}$	D2	Low	Output	BVSEL	
BVSEL	B7	High	Input	BVSEL	1, 6
$\overline{\text{CI}}$	J1	Low	Output	BVSEL	
$\overline{\text{CKSTP\_IN}}$	A3	Low	Input	BVSEL	
$\overline{\text{CKSTP\_OUT}}$	B1	Low	Output	BVSEL	

Table 12. Pinout Listing for the MPC7447A, 360 HCTE Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select[1]	Notes
$\overline{\text{QACK}}$	G5	Low	Input	BVSEL	
$\overline{\text{QREQ}}$	P4	Low	Output	BVSEL	
$\overline{\text{SHD}}$[0:1]	E4, H5	Low	I/O	BVSEL	3
$\overline{\text{SMI}}$	F9	Low	Input	BVSEL	
$\overline{\text{SRESET}}$	A2	Low	Input	BVSEL	
SYSCLK	A10	—	Input	BVSEL	
$\overline{\text{TA}}$	K6	Low	Input	BVSEL	
TBEN	E1	High	Input	BVSEL	
$\overline{\text{TBST}}$	F11	Low	Output	BVSEL	
TCK	C6	High	Input	BVSEL	
TDI	B9	High	Input	BVSEL	6
TDO	A4	High	Output	BVSEL	
$\overline{\text{TEA}}$	L1	Low	Input	BVSEL	
TEMP_ANODE	N18				17
TEMP_CATHODE	N19				17
TEST[0:3]	A12, B6, B10, E10	—	Input	BVSEL	12
TEST[4]	D10	—	Input	BVSEL	9
TMS	F1	High	Input	BVSEL	6
$\overline{\text{TRST}}$	A5	Low	Input	BVSEL	6, 14
$\overline{\text{TS}}$	L4	Low	I/O	BVSEL	3
TSIZ[0:2]	G6, F7, E7	High	Output	BVSEL	
TT[0:4]	E5, E6, F6, E9, C5	High	I/O	BVSEL	
$\overline{\text{WT}}$	D3	Low	Output	BVSEL	
V_{DD}	H8, H10, H12, J7, J9, J11, J13, K8, K10, K12, K14, L7, L9, L11, L13, M8, M10, M12	—	—	N/A	
V_{DD}	A13, A16, A18, B17, B19, C13, E13, E16, F12, F17, F19, G11, G16, H14, H17, H19, M14, M16, M18, N15, N17, P16, P18	—	—	N/A	15

Table 12. Pinout Listing for the MPC7447A, 360 HCTE Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select[1]	Notes
VDD_SENSE	G13, N12	—	—	N/A	18

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals; V_{DD} supplies power to the processor core and the PLL (after filtering to become AV_{DD}). To program the I/O voltage, connect BVSEL to either GND (selects 1.8 V), or to $\overline{\text{HRESET}}$ or OV_{DD} (selects 2.5 V); see Table 3. If used, the pull-down resistor should be less than 250 Ω. Because these settings may change in future products, it is recommended BVSEL be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future if necessary. For actual recommended value of V_{in} or supply voltages see Table 4.
2. Unused address pins must be pulled down to GND and corresponding address parity pins pulled up to OV_{DD}.
3. These pins require weak pull-up resistors (for example, 4.7 KΩ) to maintain the control signals in the negated state after they have been actively negated and released by the MPC7447A and other bus masters.
4. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at $\overline{\text{HRESET}}$ going high.
5. This signal must be negated during reset, by pull-up resistor to OV_{DD} or negation by ¬$\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), to ensure proper operation.
6. Internal pull up on die.
7. Ignored in 60x bus mode.
8. These signals must be pulled down to GND if unused, or if the MPC7447A is in 60x bus mode.
9. These input signals are for factory use only and must be pulled down to GND for normal machine operation.
10. This test signal is recommended to be tied to $\overline{\text{HRESET}}$; however, other configurations will not adversely affect performance.
11. These signals are for factory use only and must be left unconnected for normal machine operation. Some pins that were NCs on the MPC7447, MPC7445, and MPC7441 have now been defined for other purposes.
12. These input signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.
13. This pin can externally cause a performance monitor event. Counting of the event is enabled through software.
14. This signal must be asserted during reset, by pull down to GND or assertion by $\overline{\text{HRESET}}$, to ensure proper operation.
15. These pins were NCs on the MPC7447, MPC7445, and MPC7441. They may be left unconnected for backward compatibility with these devices, but it is recommended they be connected in new designs to facilitate future products. See Section 9.4, “Connection Recommendations,” for more information.
16. These pins were OV_{DD} pins on the MPC7447, MPC7445, and MPC7441. These pins are internally connected to OV_{DD} and are intended to allow an external device to detect the I/O voltage level present inside the device package. If unused, they must be connected directly to OV_{DD} or left unconnected.
17. These pins provide connectivity to the on-chip temperature diode that can be used to determine the die junction temperature of the processor. These pins may be left unterminated if unused.
18. These pins are internally connected to V_{DD} and are intended to allow an external device to detect the processor core voltage level present inside the device package. If unused, they must be connected directly to V_{DD} or left unconnected.
19. These pins are internally connected to GND and are intended to allow an external device to detect the processor ground voltage level present inside the device package. If unused, they must be connected directly to GND or left unconnected.

8.2 Mechan

Figure 13 provides th
HCTE BGA package

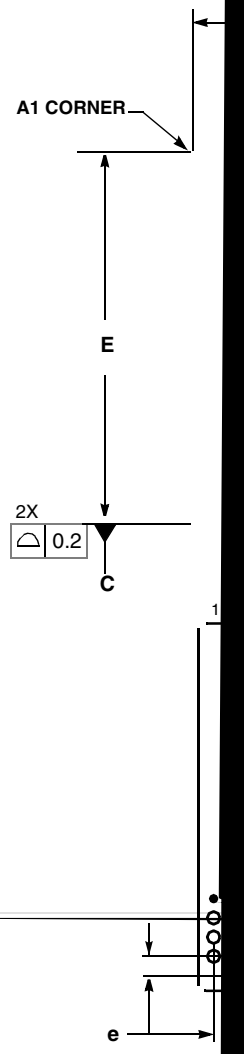
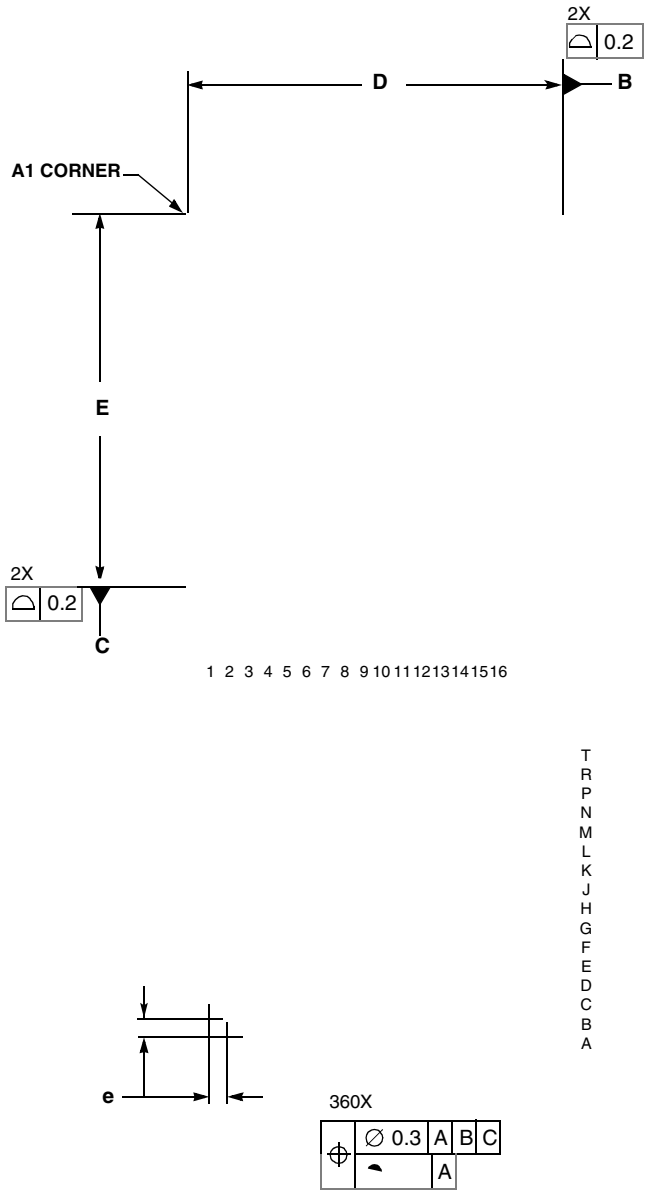


Figure 13. M

8.6 Mechanical Dimensions for the MPC7447A, 360 HCTE RoHS-Compliant BGA

Figure 15 provides the mechanical dimensions and bottom surface nomenclature for the MPC7447A, 360 HCTE BGA package.

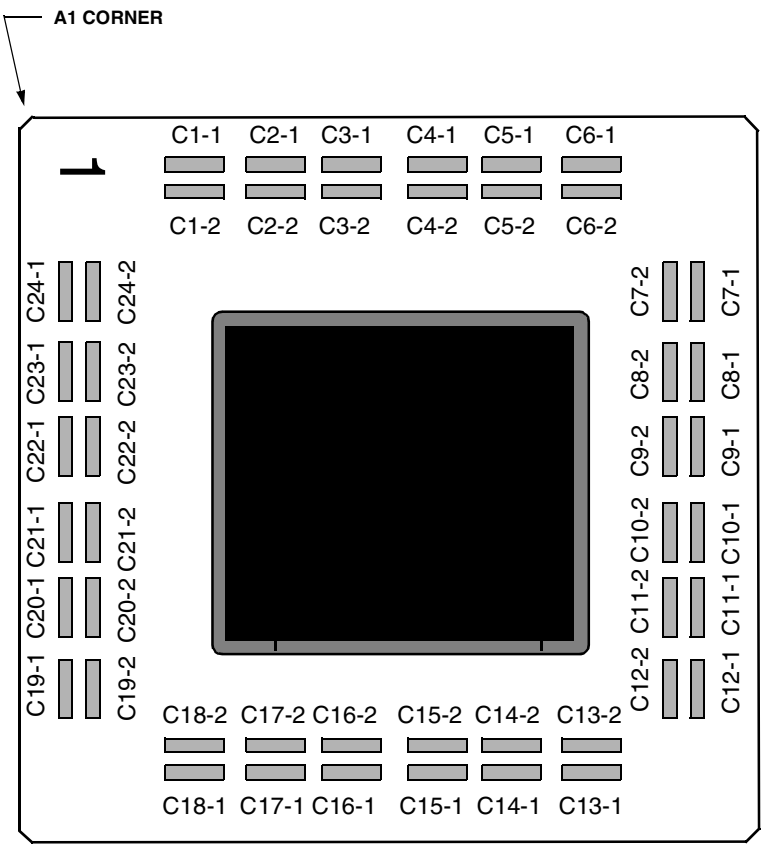


NOTES:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters.
3. Top side A1 corner index is a metalized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array.
4. Dimension A1 represents the collapsed sphere diameter.

Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC7447A, 360 HCTE RoHS-Compliant BGA Package

8.7 Substrate Capacitors for the MPC7447A, 360 HCTE

Figure 16 shows the connectivity of the substrate capacitor pads for the MPC7447A, 360 HCTE. All capacitors are 100 nF.



Capacitor	Pad Number	
	–1	–2
C1	GND	V_{DD}
C2	GND	V_{DD}
C3	GND	OV_{DD}
C4	GND	V_{DD}
C5	GND	V_{DD}
C6	GND	V_{DD}
C7	GND	V_{DD}
C8	GND	V_{DD}
C9	GND	V_{DD}
C10	GND	V_{DD}
C11	GND	V_{DD}
C12	GND	V_{DD}
C13	GND	V_{DD}
C14	GND	V_{DD}
C15	GND	V_{DD}
C16	GND	OV_{DD}
C17	GND	V_{DD}
C18	GND	OV_{DD}
C19	GND	OV_{DD}
C20	GND	V_{DD}
C21	GND	OV_{DD}
C22	GND	V_{DD}
C23	GND	OV_{DD}
C24	GND	V_{DD}

Figure 16. Substrate Bypass Capacitors for the MPC7447A, 360 HCTE

Table 14. Spread Specturm Clock Source Recommendations

At recommended operating conditions. See Table 4.

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	50	kHz	1
Frequency spread	—	1.0	%	1, 2

Notes:
1. Guaranteed by design.
2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 8.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core or bus frequency should avoid violating the stated limits by using down-spreading only.

9.2 PLL Power Supply Filtering

The AV_{DD} power signal is provided on the MPC7447A to provide power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500-KHz to 10-MHz resonant frequency range of the PLL. A circuit similar to the one shown in Figure 17 using surface-mount capacitors with minimum effective series inductance (ESL) is recommended.

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 360 HCTE footprint.

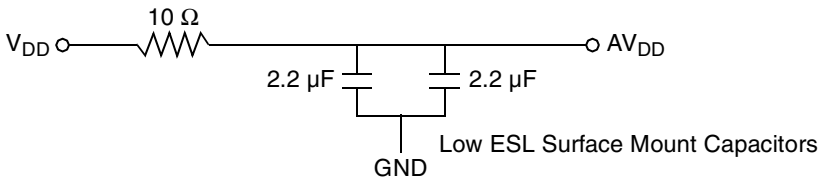


Figure 17. PLL Power Supply Filter Circuit

9.3 Decoupling Recommendations

Due to the MPC7447A dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7447A can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7447A system, and the MPC7447A itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer use sufficient decoupling capacitors, typically one capacitor for every 1–2 V_{DD} pins, and a similar or lesser number for the OV_{DD} pins, placed as close as possible to the power pins of the MPC7447A. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, OV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance.

Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
Thermagon Inc. 4707 Detroit Ave. Cleveland, OH 44102 Internet: www.thermagon.com	888-246-9050

The following section provides a heat sink selection example using one of the commercially available heat sinks.

9.8.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_i + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$$

where:

T_j is the die-junction temperature

T_i is the inlet cabinet ambient temperature

T_r is the air temperature rise within the computer cabinet

$R_{\theta JC}$ is the junction-to-case thermal resistance

$R_{\theta int}$ is the adhesive or interface material thermal resistance

$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance

P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in Table 4. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_i) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 1.5°C/W. For example, assuming a T_i of 30°C, a T_r of 5°C, an HCTE package $R_{\theta JC}$ = 0.1, and a typical power consumption (P_d) of 18.7 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 1.5°C/W + R_{\theta sa}) \times 18.7\ W$

For this example, a $R_{\theta sa}$ value of 2.1°C/W or less is required to maintain the die junction temperature below the maximum value of Table 4.

Though the die-junction-to-ambient and the heat-sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local

The ratio of I_H to I_L is usually selected to be 10:1. The above simplifies to the following:

$$V_H - V_L = 1.986 \times 10^{-4} \times nT$$

Solving for T, the equation becomes:

$$nT = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

9.8.5 Dynamic Frequency Switching (DFS)

The new DFS feature in the MPC7447A adds the ability to divide the processor-to-system bus ratio by two during normal functional operation by setting the HID1[DFS2] bit. The frequency change occurs in 1 clock cycle, and no idle waiting period is required to switch between modes. Additional information regarding DFS can be found in the *MPC7450 RISC Microprocessor Family Reference Manual.*

9.8.5.1 Power Consumption with DFS Enabled

Power consumption with DFS enabled can be approximated using the following formula:

$$P_{DFS} = \left[\frac{f_{DFS}}{f}\ (P - P_{DS})\right] + P_{DS}$$

Where:

P_{DFS} = Power consumption with DFS enabled

f_{DFS} = Core frequency with DFS enabled

f = Core frequency prior to enabling DFS

P = Power consumption prior to enabling DFS (see Table 7)

P_{DS} = Deep sleep mode power consumption (see Table 7)

The above is an approximation only. Power consumption with DFS enabled is not tested or guaranteed.

9.8.5.2 Bus-to-Core Multiplier Constraints with DFS

DFS is not available for all bus-to-core multipliers as configured by PLL_CFG[0:4] during hard reset. Specifically, because the MPC7447A does not support quarter clock ratios or the 1x multiplier, the DFS feature is limited to integer PLL multipliers of 4x and higher. The complete listing is shown in Table 16.

Table 16. Valid Divide Ratio Configurations

Bus-to-Core Multiplier Configured by PLL_CFG[0:4] (see Table 13)	Bus-to-Core Multiplier with HID1[DFS1] = 1 (÷2)
2x	N/A
3x	N/A

Table 16. Valid Divide Ratio Configurations (continued)

Bus-to-Core Multiplier Configured by PLL_CFG[0:4] (see Table 13)	Bus-to-Core Multiplier with HID1[DFS1] = 1 (÷2)
4x	2x
5x	2.5x
5.5x	N/A
6x	3x
6.5x	N/A
7x	3.5x
7.5x	N/A
8x	4x
8.5x	N/A
9x	4.5x
9.5x	N/A
10x	5x
10.5x	N/A
11x	5.5x
11.5x	N/A
12x	6x
12.5x	N/A
13x	6.5x
13.5x	N/A
14x	7x
15x	7.5x
16x	8x
17x	8.5x
18x	9x
20x	10x
21x	10.5x
24x	12x
28x	14x

9.8.5.3 Minimum Core Frequency Requirements with DFS

In many systems, enabling DFS can result in very low processor core frequencies. However, care must be taken to ensure that the resulting processor core frequency is within the limits specified in Table 8. Proper operation of the device is not guaranteed at core frequencies below the specified minimum f_{core}.

11.1 Part Numbers Fully Addressed by This Document

Table 18 provides the Freescale part numbering nomenclature for the MPC7447A.

Table 18. Part Numbering Nomenclature

MC	7447A	*xx*	*nnnn*	L	*x*
Product Code	**Part Identifier**	**Package**	**Processor Frequency**	**Application Modifier**	**Revision Level**
MC	7447A	HX = HCTE BGA VS = RoHS LGA VU = RoHS BGA	1000 1267 1333 1420	L: 1.3 V ± 50 mV 0 to 105°C	B: 1.1:PVR = 8003 0101

11.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate hardware specification addenda which supplement and supersede this document. As such parts are released, these specifications will be listed in this section.

Table 19. Part Numbers Addressed by MC7447A*xxnnnn*N*x* Series Hardware Specification Addendum (Document Order No. MPC7447AECS01AD)

MC	7447A	*xx*	*nnnn*	N	*x*
Product Code	**Part Identifier**	**Package**	**Processor Frequency**	**Application Modifier**	**Revision Level**
MC	7447A	HX = HCTE BGA VS = RoHS LGA VU = RoHS BGA	600 733 867 1000 1167	N: 1.1 V ± 50 mV 0 to 105°C	B:1.1: PVR = 8003 0101