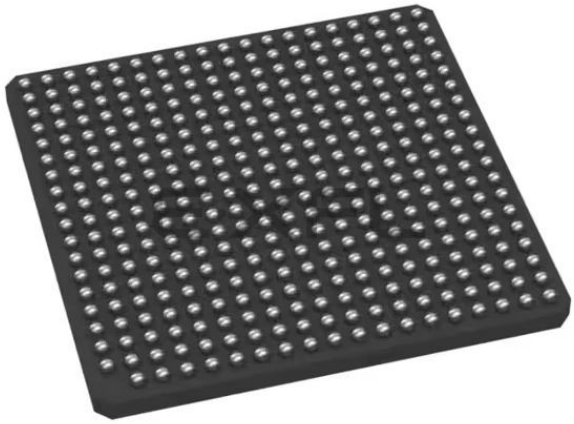

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.42GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-CLGA, FCCLGA
Supplier Device Package	360-FCCLGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc7447avs1420lb

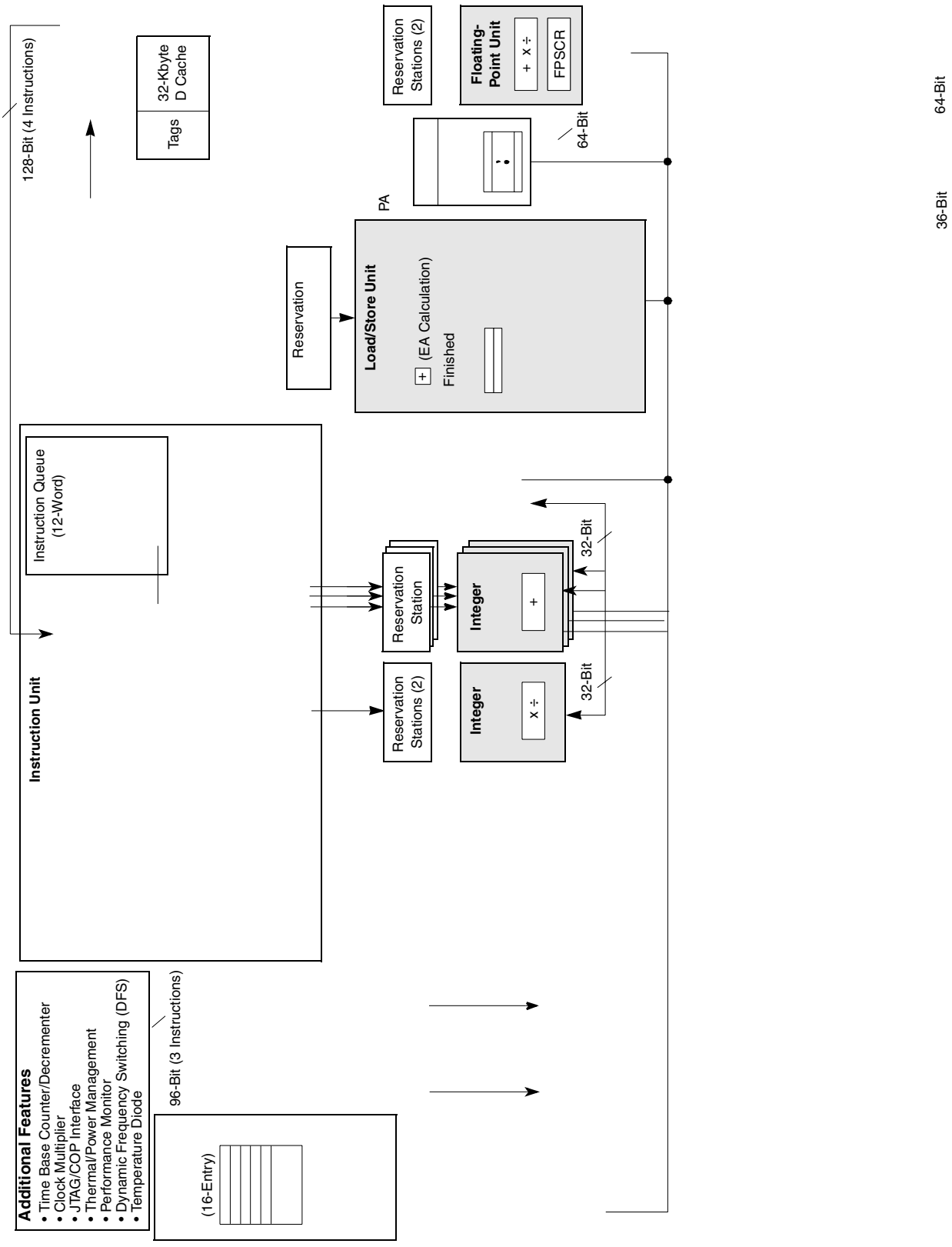


Figure 1. MPC7447A Block Diagram

Storage temperature range	T_{stg}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 4. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution**: V_{DD}/AV_{DD} must not exceed OV_{DD} by more than 1.0 V during normal operation; this limit may be exceeded for a maximum of 20 ms during the power-on reset and power-down sequences.
3. **Caution**: OV_{DD} must not exceed V_{DD}/AV_{DD} by more than 2.0 V during normal operation; this limit may be exceeded for a maximum of 20 ms during the power-on reset and power-down sequences.
4. BVSEL must be set to 0, such that the bus is in 1.8-V mode.
5. BVSEL must be set to $\overline{\text{HRESET}}$ or 1, such that the bus is in 2.5-V mode.
6. **Caution**: $V_{in1(xef(i)1er)2}$ 1eref4.8(s)-1 mo5.45 s83 .8(odcn183 .8(odcn183 .8(odcn183 .8(ocn183 .8(ocn.783824.5(1.9191 10in)Tjt0

Figure 2 shows the undershoot and overshoot voltage on the MPC7447A.

Figure 2. Overshoot/Undershoot Voltage

The MPC7447A provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC7447A core voltage must always be provided at the nominal voltage (see Table 4) or at the supported derated voltage (see Section 5.3, “Voltage and Frequency Derating”). The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal $\overline{\text{HRESET}}$. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} power pins. Table 3 provides the input threshold voltage settings. Because these settings may change in future products, it is recommended that BVSEL be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future if necessary.

Typical	4.1	4.0	3.2	4.0	W	1, 2

Notes:

1. These values specify the power consumption for the core power supply (V_{DD}) at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include I/O supply power (OV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} power is system dependent but is typically < 5% of V_{DD} power. Worst case power consumption for AV_{DD} < 3 mW.
2. Typical power is an average value measured at the nominal recommended V

5.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC7447A. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Section 5.2.1, "Clock AC Specifications," and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:4] signals, and can be dynamically modified using dynamic frequency switching (DFS). Parts are sold by maximum processor core frequency; see Section 11, "Ordering Information," for information on ordering parts. DFS is described in Section 9.8.5, "Dynamic Frequency Switching (DFS)."

5.2.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications as defined in Figure 3 and represents the tested operating frequencies of the devices. The maximum system bus frequency, f_{SYSCLK}, given in Table 8, is considered a practical maximum in a typical single-processor system. The actual maximum SYSCLK frequency for any application of the MPC7447A will be a function of the AC timings of the MPC7447A, the AC timings for the system controller, bus loading, printed-circuit board topology, trace lengths, and so forth, and may be less than the value given in Table 8.

NOTE

The core frequency information in this table applies when operating the device at the nominal core voltage indicated in Table 4. For core frequency specifications at derated core voltage conditions, see Section 5.3, "Voltage and Frequency Derating."

Table 8. Clock AC Timing Specifications

At recommended operating conditions. See Table 4.

Characteristic	Symbol	Maximum Processor Core Frequency								Unit	Notes
		1000 MHz		1267 MHz		1333 MHz		1420 MHz			
		Min	Max	Min	Max	Min	Max	Min	Max		
Processor core frequency	f_{core}	600	1000	600	1267	600	1333	600	1420	MHz	1, 8, 9
VCO frequency	f_{VCO}	1200	2000	1200	2533	1200	2667	1200	2840	MHz	1, 9
SYSCLK frequency	f_{SYSCLK}	33	167	33	167	33	167	33	167	MHz	1, 2, 8
SYSCLK cycle time	t_{SYSCLK}	6.0	30	6.0	30	6.0	30	6.0	30	ns	2
SYSCLK rise and fall time	t_{KR}, t_{KF}	—	1.0	—	1.0	—	1.0	—	1.0	ns	3
SYSCLK duty cycle measured at $OV_{DD}/2$	t_{KHKL}/t_{SYSCLK}	40	60	40	60	40	60	40	60	%	4
SYSCLK cycle-to-cycle jitter		—	150	—	150	—	150	—	150	ps	5, 6
Internal PLL relock time		—	100	—	100	—	100	—	100	µs	7

Notes:

1. **Caution**: The SYSCLK frequency and PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, processor core frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in Section 9.1.1, "PLL Configuration," for valid PLL_CFG[0:4] settings.
2. Assumes a lightly-loaded, single-processor system.
3. Rise and fall times for the SYSCLK input measured from 0.4 to 1.4 V.
4. Timing is guaranteed by design and characterization.
5. Guaranteed by design.
6. The SYSCLK driver's closed loop jitter bandwidth should be less than 1.5 MHz at –3 dB.
7. Relock timing is guaranteed by design and characterization. PLL relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time during the power-on reset sequence.
8. **Caution**: If DFS is enabled, the SYSCLK frequency and PLL_CFG[0:4] settings must be chosen such that the resulting processor frequency is greater than or equal to the minimum core frequency.
9. **Caution**: These values specify the maximum processor core and VCO frequencies when the device is operated at the nominal core voltage. If operating the device at the derated core voltage, the processor core and VCO frequencies must be reduced. See Section 5.3, "Voltage and Frequency Derating," for more information.

Figure 3 provides the SYSCLK input timing diagram.

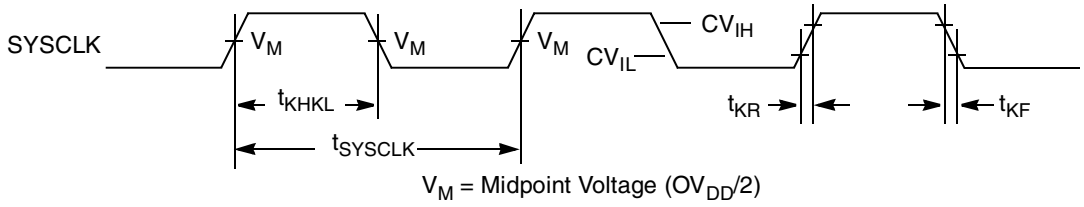


Figure 3. SYSCLK Input Timing Diagram

Table 9. Processor Bus AC Timing Specifications[1] (continued)

At recommended operating conditions. See Table 4.

Parameter	Symbol [2]	All Speed Grades		Unit	Notes
		Min	Max		
SYSCLK to $\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{SYSCLK}	3, 5, 6, 7

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 4). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) (note the position of the reference and its state for inputs) and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. t_{sysclk} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. According to the bus protocol, $\overline{\text{TS}}$ is driven only by the currently active bus master. It is asserted low and precharged high before returning to high impedance, as shown in Figure 6. The nominal precharge width for $\overline{\text{TS}}$ is 0.5 × t_{SYSCLK}, that is, less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{\text{TS}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-impedance behavior is guaranteed by design.
5. Guaranteed by design and not tested.
6. According to the bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue because any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following $\overline{\text{AACK}}$ will then go to high impedance for 1 clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{SYSCLK}; that is, it should be high impedance as shown in Figure 6 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing is tested for the signal asserted.The high-impedance behavior is guaranteed by design.
7. According to the MPX bus protocol, $\overline{\text{SHD0}}$ and $\overline{\text{SHD1}}$ can be driven by multiple bus masters beginning the cycle of $\overline{\text{TS}}$. Timing is the same as $\overline{\text{ARTRY}}$, that is, the signal is high impedance for a fraction of a cycle, then negated for up to an entire cycle (crossing a bus cycle boundary) before being three-stated again. The nominal precharge width for $\overline{\text{SHD0}}$ and $\overline{\text{SHD1}}$ is 1.0 t_{SYSCLK}. The edges of the precharge vary depending on the programmed ratio of core to bus (PLL configurations).
8. $\overline{\text{BMODE}}$[0:1] and BVSEL are mode select inputs and are sampled before and after $\overline{\text{HRESET}}$ negation. These parameters represent the input setup and hold times for each sample. These values are guaranteed by design and not tested. These inputs must remain stable after the second sample. See Figure 5 for sample timing.

Figure 4 provides the AC test load for the MPC7447A.

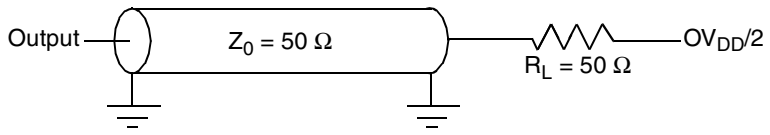


Figure 4. AC Test Load

CLK_OUT	H2	High	Output	BVSEL	
D[0:63]	R15, W15, T14, V16, W16, T15, U15, P14, V13, W13, T13, P13, U14, W14, R12, T12, W12, V12, N11, N10, R11, U11, W11, T11, R10, N9, P10, U10, R9, W10, U9, V9, W5, U6, T5, U5, W7, R6, P7, V6, P17, R19, V18, R18, V19, T19, U19, W19, U18, W17, W18, T16, T18, T17, W3, V17, U4, U8, U7, R7, P6, R8, W8, T8	High	I/O	BVSEL	
$\overline{\text{DBG}}$	M2	Low	Input	BVSEL	
DP[0:7]	T3, W4, T4, W9, M6, V3, N8, W6	High	I/O	BVSEL	
$\overline{\text{DRDY}}$	R3	Low	Output	BVSEL	7
DTI[0:3]	G1, K1, P1, N1	High	Input	BVSEL	8
EXT_QUAL	A11	High	Input	BVSEL	9
$\overline{\text{GBL}}$	E2	Low	I/O	BVSEL	
GND	B5, C3, D6, D13, E17, F3, G17, H4, H7, H9, H11, H13, J6, J8, J10, J12, K7, K3, K9, K11, K13, L6, L8, L10, L12, M4, M7, M9, M11, M13, N7, P3, P9, P12, R5, R14, R17, T7, T10, U3, U13, U17, V5, V8, V11, V15	—	—	N/A	
GND	A17, A19, B13, B16, B18, E12, E19, F13, F16, F18, G19, H18, J14, L14, M15, M17, M19, N14, N16, P15, P19	—	—	N/A	15
GND_SENSE	G12, N13	—	—	N/A	19
$\overline{\text{HIT}}$	B2	Low	Output	BVSEL	7
$\overline{\text{HRESET}}$	D8	Low	Input	BVSEL	
$\overline{\text{INT}}$	D4	Low	Input	BVSEL	
L1_TSTCLK	G8	High	Input	BVSEL	9
L2_TSTCLK	B3	High	Input	BVSEL	10
NC (no connect)	A6, A14, A15, B14, B15, C14, C15, C16, C17, C18, C19, D14, D15, D16, D17, D18, D19, E14, E15, F14, F15, G14, G15, H15, H16, J15, J16, J17, J18, J19, K15, K16, K17, K18, K19, L15, L16, L17, L18, L19	—	—	—	11
$\overline{\text{LSSD\_MODE}}$	E8	Low	Input	BVSEL	6, 12
$\overline{\text{MCP}}$	C9	Low	Input	BVSEL	
OV_{DD}	B4, C2, C12, D5, F2, H3, J5, K2, L5, M3, N6, P2, P8, P11, R4, R13, R16, T6, T9, U2, U12, U16, VF16,0(2I8)-27(VF1634.885(6)25.8(,)m-8.74H)5.9(,0(2I8)-26c(DD,0(8-277				

Table 12. Pinout Listing for the MPC7447A, 360 HCTE Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Select[1]	Notes
VDD_SENSE	G13, N12	—	—	N/A	18

Notes:

1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals; V_{DD} supplies power to the processor core and the PLL (after filtering to become AV_{DD}). To program the I/O voltage, connect BVSEL to either GND (selects 1.8 V), or to $\overline{\text{HRESET}}$ or OV_{DD} (selects 2.5 V); see Table 3. If used, the pull-down resistor should be less than 250 Ω. Because these settings may change in future products, it is recommended BVSEL be configured using resistor options, jumpers, or some other flexible means, with the capability to reconfigure the termination of this signal in the future if necessary. For actual recommended value of V_{in} or supply voltages see Table 4.
2. Unused address pins must be pulled down to GND and corresponding address parity pins pulled up to OV_{DD}.
3. These pins require weak pull-up resistors (for example, 4.7 KΩ) to maintain the control signals in the negated state after they have been actively negated and released by the MPC7447A and other bus masters.
4. This signal selects between MPX bus mode (asserted) and 60x bus mode (negated) and will be sampled at $\overline{\text{HRESET}}$ going high.
5. This signal must be negated during reset, by pull-up resistor to OV_{DD} or negation by ¬$\overline{\text{HRESET}}$ (inverse of $\overline{\text{HRESET}}$), to ensure proper operation.
6. Internal pull up on die.
7. Ignored in 60x bus mode.
8. These signals must be pulled down to GND if unused, or if the MPC7447A is in 60x bus mode.
9. These input signals are for factory use only and must be pulled down to GND for normal machine operation.
10. This test signal is recommended to be tied to $\overline{\text{HRESET}}$; however, other configurations will not adversely affect performance.
11. These signals are for factory use only and must be left unconnected for normal machine operation. Some pins that were NCs on the MPC7447, MPC7445, and MPC7441 have now been defined for other purposes.
12. These input signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.
13. This pin can externally cause a performance monitor event. Counting of the event is enabled through software.
14. This signal must be asserted during reset, by pull down to GND or assertion by $\overline{\text{HRESET}}$, to ensure proper operation.
15. These pins were NCs on the MPC7447, MPC7445, and MPC7441. They may be left unconnected for backward compatibility with these devices, but it is recommended they be connected in new designs to facilitate future products. See Section 9.4, “Connection Recommendations,” for more information.
16. These pins were OV_{DD} pins on the MPC7447, MPC7445, and MPC7441. These pins are internally connected to OV_{DD} and are intended to allow an external device to detect the I/O voltage level present inside the device package. If unused, they must be connected directly to OV_{DD} or left unconnected.
17. These pins provide connectivity to the on-chip temperature diode that can be used to determine the die junction temperature of the processor. These pins may be left unterminated if unused.
18. These pins are internally connected to V_{DD} and are intended to allow an external device to detect the processor core voltage level present inside the device package. If unused, they must be connected directly to V_{DD} or left unconnected.
19. These pins are internally connected to GND and are intended to allow an external device to detect the processor ground voltage level present inside the device package. If unused, they must be connected directly to GND or left unconnected.

8.3 Package Parameters for the MPC7447A, 360 HCTE LGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360 high coefficient of thermal expansion ceramic land grid array (HCTE).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	1.92 mm
Maximum module height	2.20 mm
Coefficient of thermal expansion	12.3 ppm/°C

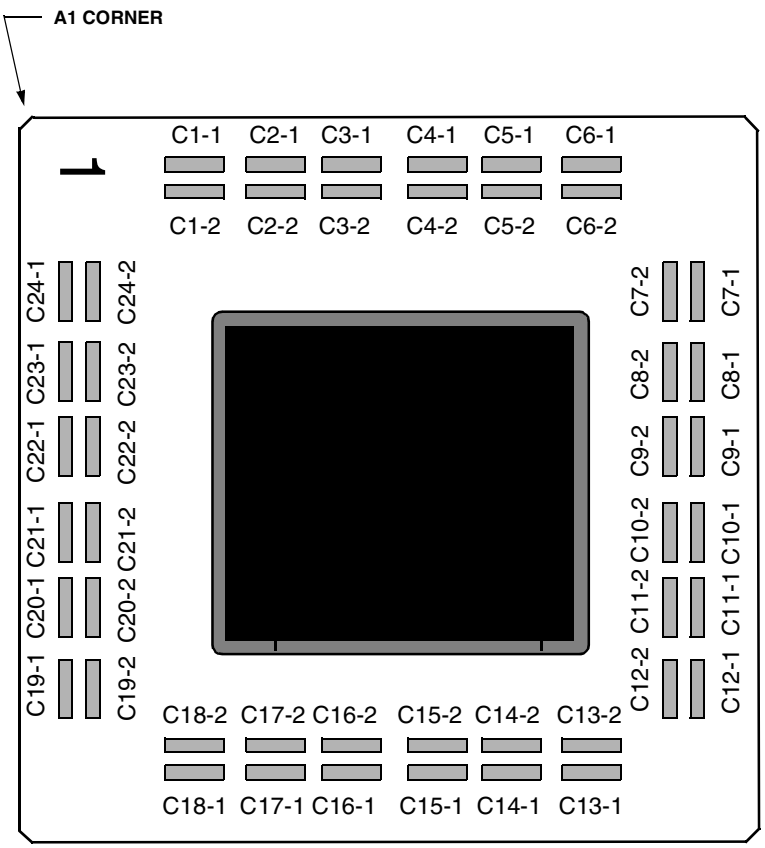
8.5 Package Parameters for the MPC7447A, 360 HCTE RoHS-Compliant BGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360 lead-free high coefficient of thermal expansion ceramic ball grid array (HCTE).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.32 mm
Maximum module height	2.80 mm
Ball diameter	0.75 mm (30 mil)
Coefficient of thermal expansion	12.3 ppm/°C

8.7 Substrate Capacitors for the MPC7447A, 360 HCTE

Figure 16 shows the connectivity of the substrate capacitor pads for the MPC7447A, 360 HCTE. All capacitors are 100 nF.



Capacitor	Pad Number	
	–1	–2
C1	GND	V_{DD}
C2	GND	V_{DD}
C3	GND	OV_{DD}
C4	GND	V_{DD}
C5	GND	V_{DD}
C6	GND	V_{DD}
C7	GND	V_{DD}
C8	GND	V_{DD}
C9	GND	V_{DD}
C10	GND	V_{DD}
C11	GND	V_{DD}
C12	GND	V_{DD}
C13	GND	V_{DD}
C14	GND	V_{DD}
C15	GND	V_{DD}
C16	GND	OV_{DD}
C17	GND	V_{DD}
C18	GND	OV_{DD}
C19	GND	OV_{DD}
C20	GND	V_{DD}
C21	GND	OV_{DD}
C22	GND	V_{DD}
C23	GND	OV_{DD}
C24	GND	V_{DD}

Figure 16. Substrate Bypass Capacitors for the MPC7447A, 360 HCTE

9 System Design Information

This section provides system and thermal design recommendations for successful application of the MPC7447A.

9.1 Clocks

9.1.1 PLL Configuration

The MPC7447A PLL is configured by the PLL_CFG[0:4] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the MPC7447A is shown in Table 13 for a set of example frequencies. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with the 1400 MHz column in Table 8. When enabled, dynamic frequency switching (DFS) also affects the core frequency by halving the bus-to-core multiplier; see Section 9.8.5, "Dynamic Frequency Switching (DFS)," for more information. Note that when DFS is enabled the resulting core frequency must meet the minimum core frequency requirements described in Table 8.

Table 13. MPC7447A Microprocessor PLL Configuration Example for 1420-MHz Parts

PLL_CFG[0:4]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)								
	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Bus (SYSCLK) Frequency						
			33 MHz	50 MHz	67 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz
01000	2x [1]	2x								
10000	3x [1]	2x								
10100	4x [1]	2x								668 (1333)
10110	5x	2x							665 (1333)	835 (1670)
10010	5.5x	2x							732 (1466)	919 (1837)
11010	6x	2x						600 (1200)	798 (1600)	1002 (2004)
01010	6.5x	2x						650 (1300)	865 (1730)	1086 (2171)
00100	7x	2x						700 (1400)	931 (1862)	1169 (2338)
00010	7.5x	2x					623 (1245)	750 (1500)	998 (2000)	1253 (2505)
11000	8x	2x				600 (1200)	664 (1328)	800 (1600)	1064 (2128)	1336 (2672)

Table 13. MPC7447A Microprocessor PLL Configuration Example for 1420-MHz Parts (continued)

PLL_CFG[0:4]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)								
	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Bus (SYSCLK) Frequency						
			33 MHz	50 MHz	67 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz
01101	24x	2x	792 (1600)	1200 (2400)						
11101	28x	2x	924 (1866)	1400 (2800)						
00110	PLL bypass		PLL off, SYSCLK clocks core circuitry directly							
11110	PLL off		PLL off, no core clocking occurs							

Notes:

1. Ratios below 5:1 require an AACK delay See *MPC7450 RISC Microprocessor Family Reference Manual*, Section 9.3.3, “MPX Bus Address Tenure Termination.”
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies that are not useful, not supported, or not tested for by the MPC7455; see Section 5.2.1, “Clock AC Specifications,” for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly and the PLL is disabled. However, the bus interface unit requires a 2x clock to function. Therefore, an additional signal, EXT_QUAL, must be driven at one-half the frequency of SYSCLK and offset in phase to meet the required input setup t_{IVKH} and hold time t_{IXKH} (see Table 9). The result will be that the processor bus frequency will be one-half SYSCLK while the internal processor is clocked at SYSCLK frequency. This mode is intended for factory use and emulator tool use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL-off mode, no clocking occurs inside the MPC7447A regardless of the SYSCLK input.

9.1.2 System Bus Clock (SYSCLK) and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 8 considers short-term (cycle-to-cycle) jitter only and the clock generator’s cycle-to-cycle output jitter should meet the MPC7457 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC7457 is compatible with spread spectrum sources if the recommendations listed in Table 14 are observed.

These capacitors should have a value of 0.01 or 0.1 μF. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance. Orientations where connections are made along the length of the part, such as 0204, are preferable but not mandatory. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993) and contrary to previous recommendations for decoupling Freescale microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

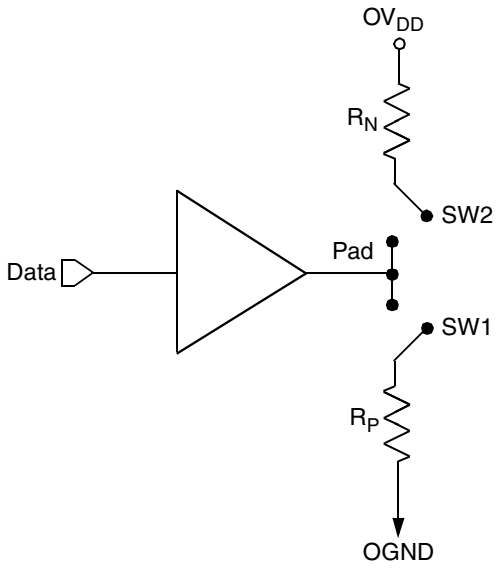


Figure 18. Driver Impedance Measurement

Table 15 summarizes the signal impedance results. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 15. Impedance Characteristics

V_{DD} = 1.5 V, OV_{DD} = 1.8 V ± 5%, T_j = 5°–85°C

Impedance		Processor Bus	Unit
Z_0	Typical	33–42	Ω
	Maximum	31–51	Ω

9.6 Pull-Up/Pull-Down Resistor Requirements

The MPC7447A requires high-resistive (weak: 4.7 KΩ) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7447A or other bus masters. These pins are: $\overline{\text{TS}}$, $\overline{\text{ARTRY}}$, $\overline{\text{SHDO}}$, and $\overline{\text{SHD1}}$.

Some pins designated as being factory test pins must be pulled up to OV_{DD} or down to GND to ensure proper device operation. The pins that must be pulled up to OV_{DD} are: $\overline{\text{LSSD\_MODE}}$ and TEST[0:3]; the pins that must be pulled down to GND are: L1_TSTCLK and TEST[4]. The $\overline{\text{CKSTP\_IN}}$ signal should likewise be pulled up through a pull-up resistor (weak or stronger: 4.7 KΩ–1 KΩ) to prevent erroneous assertions of this signal.

In addition, the MPC7447A has one open-drain style output that requires a pull-up resistor (weak or stronger: 4.7 KΩ–1 KΩ) if it is used by the system. This pin is $\overline{\text{CKSTP\_OUT}}$.

If pull-down resistors are used to configure BVSEL, the resistors should be less than 250 Ω (see Table 12). Because PLL_CFG[0:4] must remain stable during normal operation, strong pull-up and pull-down resistors (1 KΩ or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise or noise coupling.

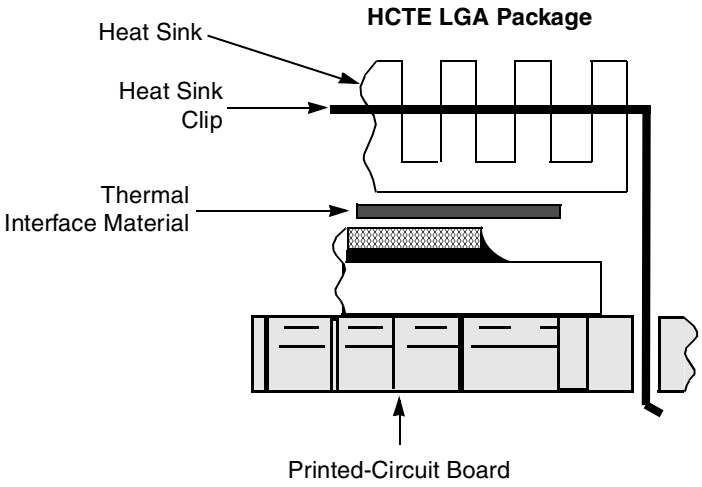


Figure 21. LGA Package Exploded Cross-Sectional View with Several Heat Sink Options

The board designer can choose between several types of heat sinks to place on the MPC7447A. There are several commercially-available heat sinks for the MPC7447A provided by the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-567-8082
Calgreg Thermal Solutions 60 Alhambra Road Warwick, RI 02886 Internet: www.calgregthermalsolutions.com	401-732-8100
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Tyco Electronics Chip Coolers™ P.O. Box 3608 Harrisburg, PA 17105-3608 Internet: www.chipcoolers.com	717-564-0100
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-2800

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.

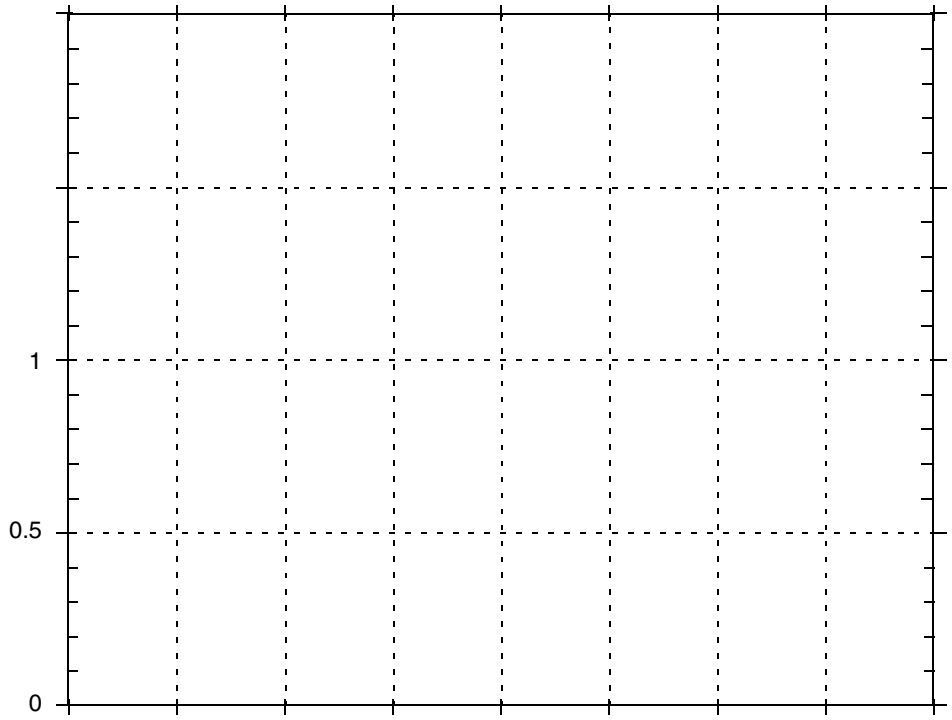


Figure 23. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity and mechanical strength to meet equipment shock/vibration requirements. There are several commercially available thermal interfaces and adhesive materials provided by the following vendors:

The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481

Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
Thermagon Inc. 4707 Detroit Ave. Cleveland, OH 44102 Internet: www.thermagon.com	888-246-9050

The following section provides a heat sink selection example using one of the commercially available heat sinks.

9.8.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_i + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$$

where:

T_j is the die-junction temperature

T_i is the inlet cabinet ambient temperature

T_r is the air temperature rise within the computer cabinet

$R_{\theta JC}$ is the junction-to-case thermal resistance

$R_{\theta int}$ is the adhesive or interface material thermal resistance

$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance

P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in Table 4. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_i) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 1.5°C/W. For example, assuming a T_i of 30°C, a T_r of 5°C, an HCTE package $R_{\theta JC}$ = 0.1, and a typical power consumption (P_d) of 18.7 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 1.5°C/W + R_{\theta sa}) \times 18.7\ W$

For this example, a $R_{\theta sa}$ value of 2.1°C/W or less is required to maintain the die junction temperature below the maximum value of Table 4.

Though the die-junction-to-ambient and the heat-sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local

9.8.4 Temperature Diode

The MPC7447A has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. For proper operation, the monitoring device used should auto-calibrate the device by canceling out the V_{BE} variation of each MPC7447A's internal diode.

The following are the specifications of the MPC7447A on-board temperature diode:

0.40 V $< V_f <$ 0.90 V

Operating range 2–300 µA

Diode leakage < 10 nA @ 125 C

Ideality factor (n) over 5–150 µA @ 60 C: 1.0275 ± 0.9 %

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_s \left[e^{\frac{qV_f}{nKT}} - 1 \right]$$

Where:

I_{fw} = Forward current
I_s = Saturation current
V_d = Voltage at diode BM: this does not show up in any equations.
V_f = Voltage forward biased
q = Charge of electron (1.6×10^{-19} C)
n = Ideality factor (normally 1.0)
K = Boltzman's constant (1.38×10^{-23} Joules/K)
T = Temperature (Kelvins)

Another useful equation is :

$$V_H - V_L = n\frac{KT}{q} \left[ln \frac{I_H}{I_L} \right]$$

Where:

V_H = Diode voltage while I_H is flowing
V_L = Diode voltage while I_L is flowing
I_H = Larger diode bias current
I_L = Smaller diode bias current

10 Document Revision History

Table 17 provides a revision history for this hardware specification.

Table 17. Document Revision History

Revision Number	Date	Substantive Changes
5	01/30/2005	Corrected RoHS BGA sphere diameter dimensions
4	09/23/2005	Added RoHS BGA case outlines and part numbers. Removed note references for $\overline{CI}$ and $\overline{WT}$ in Table 12
3	08/23/2005	Added "Section 9.1.2, "System Bus Clock (SYSCLK) and Spread Spectrum Sources"
		Section 9.8, "Thermal Management Information": Added vendor to list
		Section 9.8.3, "Heat Sink Selection Example": Correct silicon die and underfil/bump model dimensions
2	02/16/2005	Changed die size
		Table 8: Modified jitter specifications to conform to JEDEC standards, changed jitter specification to cycle-to-cycle jitter (instead of long- and short-term jitter); changed jitter bandwidth recommendations.
		Added information for LGA package.
1	—	Added t_{KHTSV}, t_{KHARV}, t_{KHTSX}, and t_{KHARX} to Table 9; these were previously grouped with t_{KHOV} and t_{KHOX}. NOTE: Documentation change only; the values for the output valid and output hold AC timing specifications remain unchanged for $\overline{TS}$, $\overline{ARTRY}$, and $\overline{SHD}$[0:1].
		Added derating section with table; added 1000 MHz speed bin
0.1	—	Retitled Table 19 to include document order information for MC7447AnnnnNx series hardware specification addendum.
0	—	Initial revision.

11 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 11.1, "Part Numbers Fully Addressed by This Document." Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact a local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier that may specify special application conditions. Each part number also contains a revision level code that refers to the die mask revision number. Section 11.2, "Part Numbers Not Fully Addressed by This Document," lists the part numbers that do not fully conform to the specifications of this document. These special part numbers require an additional document called a hardware specification addendum.

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