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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Multimedia; SIMD
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	360-BCBGA, FCCBGA
Supplier Device Package	360-FCCBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc7447avu1333lb

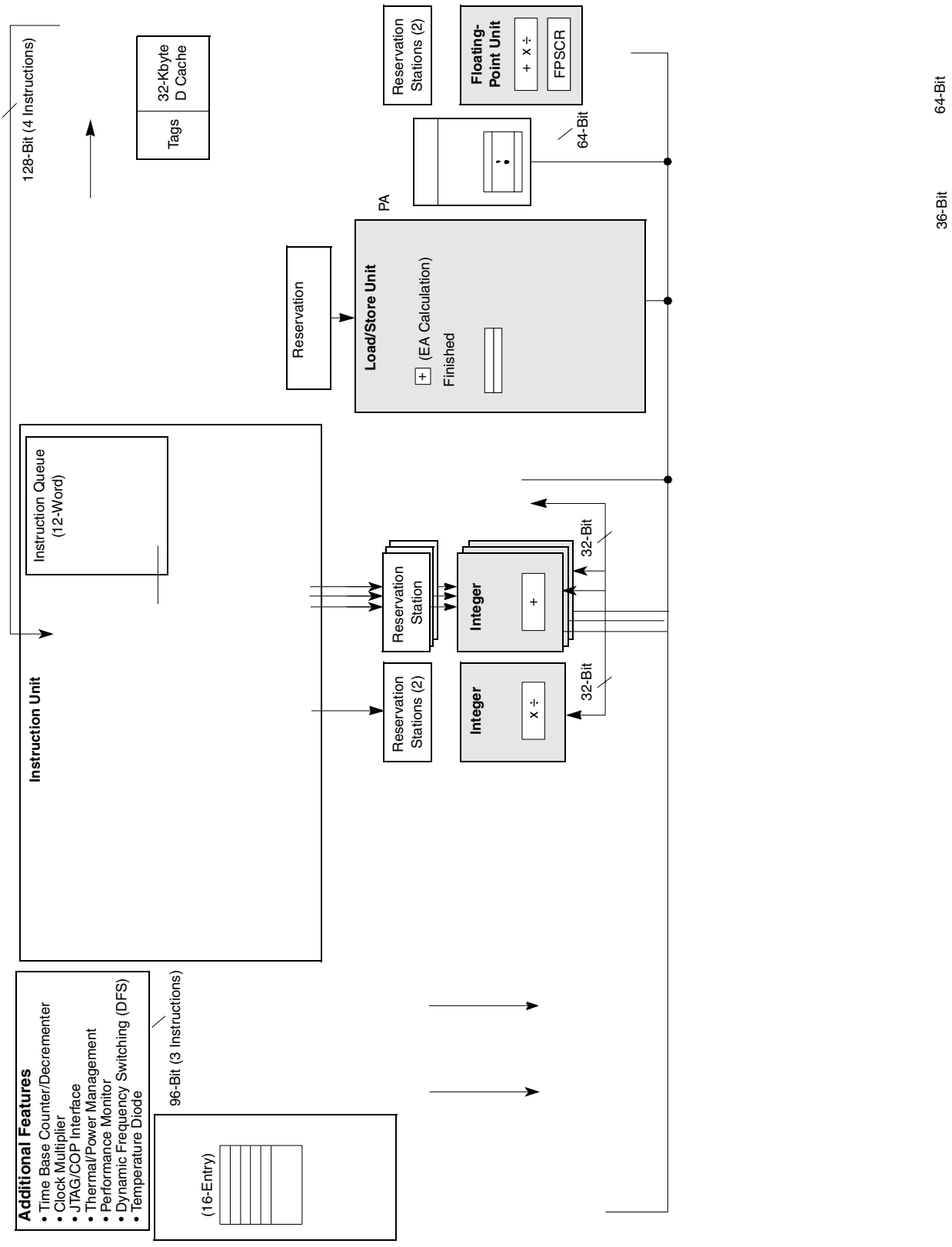

Figure 1. MPC7447A Block Diagram

Table 1. Microarchitecture Comparison (continued)

Microarchitectural Specs	MPC7447A	MPC7447	MPC7445	MPC7441
BHT size	2K-entry			
Link stack depth	8			
Unresolved branches supported	3			
Branch taken penalty (BTIC hit)	1			
Minimum misprediction penalty	6			
Execution Unit Timings (Latency-Throughput)				
Aligned load (integer, float, vector)	3-1, 4-1, 3-1			
Misaligned load (integer, float, vector)	4-2, 5-2, 4-2			
L1 miss, L2 hit latency	9 data/13 instruction			
SFX (aDd Sub, Shift, Rot, Cmp, logicals)	1-1			
Integer multiply (32×8, 32×16, 32×32)	3-1, 3-1, 4-2			
Scalar float	5-1			
VSFX (vector simple)	1-1			
VCFX (vector complex)	4-1			
VFPU (vector float)	4-1			
VPER (vector permute)	2-1			
MMUs				
TLBs (instruction and data)	128-entry, 2-way			
Tablewalk mechanism	Hardware + software			
Instruction BATs/data BATs	8/8	8/8	8/8	4/4
L1 I Cache/D Cache Features				
Size	32K/32K			
Associativity	8-way			
Locking granularity	Way			
Parity on Instruction cache	Word			
Parity on data cache	Byte			
Number of data cache misses (load/store)	5/1			
Data stream touch engines	4 streams			
On-Chip Cache Features				
Cache level	L2			
Size/associativity	512-Kbyte/8-way		256-Kbyte/8-way	
Access width	256 bits			

Table 6 provides the DC electrical

Table 6. DC Electrical Specifications (continued)

At recommended operating conditions. See Table 4.

Characteristic		Nominal Bus Voltage [1]	Symbol	Min	Max	Unit	Notes
Capacitance, V_{in} = 0 V, f = 1 MHz	All other inputs		C_{in}	—	8.0	pF	5

Notes:
1. Nominal voltages; see Table 4 for recommended operating conditions.
2. For processor bus signals, the reference is OV_{DD}
3. Excludes test signals and IEEE 1149.1 boundary scan (JTAG) signals
4. The leakage is measured for nominal OV_{DD} and V_{DD}, or both OV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or –5%).
5. Capacitance is periodically sampled rather than 100% tested.
6. Excludes signals with internal pullups: BVSEL, $\overline{\text{LSSD\_MODE}}$, TDI, TMS, and $\overline{\text{TRST}}$.

Table 7 provides the power consumption for the MPC7447A. For information regarding power consumption when dynamic frequency switching is enabled, see Section 9.8.5, “Dynamic Frequency Switching (DFS).”

NOTE

The power consumption information in this table applies when the device is operated at the nominal core voltage indicated in Table 4. For power consumption at derated core voltage conditions, see Section 5.3, “Voltage and Frequency Derating.”

Table 7. Power Consumption for MPC7447A

	Processor (CPU) Frequency				Unit	Notes
	1000	1267	1333 [5]	1420 MHz		
Full-Power Mode						
Typical	16.0	18.3	18.0	21.0	W	1, 2
Maximum	23.0	26.0	25.0	30.0	W	1, 3
Nap Mode						
Typical	4.1	4.1	3.3	4.1	W	1, 2
Sleep Mode						
Typical	4.1	4.1	3.3	4.1	W	1, 2
Deep Sleep Mode (PLL Disabled)						

Table 8. Clock AC Timing Specifications

At recommended operating conditions. See Table 4.

Characteristic	Symbol	Maximum Processor Core Frequency								Unit	Notes
		1000 MHz		1267 MHz		1333 MHz		1420 MHz			
		Min	Max	Min	Max	Min	Max	Min	Max		
Processor core frequency	f_{core}	600	1000	600	1267	600	1333	600	1420	MHz	1, 8, 9
VCO frequency	f_{VCO}	1200	2000	1200	2533	1200	2667	1200	2840	MHz	1, 9
SYSCLK frequency	f_{SYSCLK}	33	167	33	167	33	167	33	167	MHz	1, 2, 8
SYSCLK cycle time	t_{SYSCLK}	6.0	30	6.0	30	6.0	30	6.0	30	ns	2
SYSCLK rise and fall time	t_{KR}, t_{KF}	—	1.0	—	1.0	—	1.0	—	1.0	ns	3
SYSCLK duty cycle measured at $OV_{DD}/2$	t_{KHKL}/t_{SYSCLK}	40	60	40	60	40	60	40	60	%	4
SYSCLK cycle-to-cycle jitter		—	150	—	150	—	150	—	150	ps	5, 6
Internal PLL relock time		—	100	—	100	—	100	—	100	µs	7

Notes:

1. **Caution**: The SYSCLK frequency and PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, processor core frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in Section 9.1.1, "PLL Configuration," for valid PLL_CFG[0:4] settings.
2. Assumes a lightly-loaded, single-processor system.
3. Rise and fall times for the SYSCLK input measured from 0.4 to 1.4 V.
4. Timing is guaranteed by design and characterization.
5. Guaranteed by design.
6. The SYSCLK driver's closed loop jitter bandwidth should be less than 1.5 MHz at –3 dB.
7. Relock timing is guaranteed by design and characterization. PLL relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time during the power-on reset sequence.
8. **Caution**: If DFS is enabled, the SYSCLK frequency and PLL_CFG[0:4] settings must be chosen such that the resulting processor frequency is greater than or equal to the minimum core frequency.
9. **Caution**: These values specify the maximum processor core and VCO frequencies when the device is operated at the nominal core voltage. If operating the device at the derated core voltage, the processor core and VCO frequencies must be reduced. See Section 5.3, "Voltage and Frequency Derating," for more information.

Figure 3 provides the SYSCLK input timing diagram.

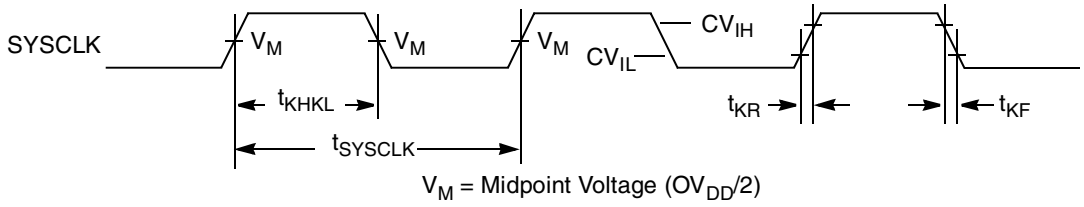

Figure 3. SYSCLK Input Timing Diagram

Figure 8 provides the JTAG clock input timing diagram.

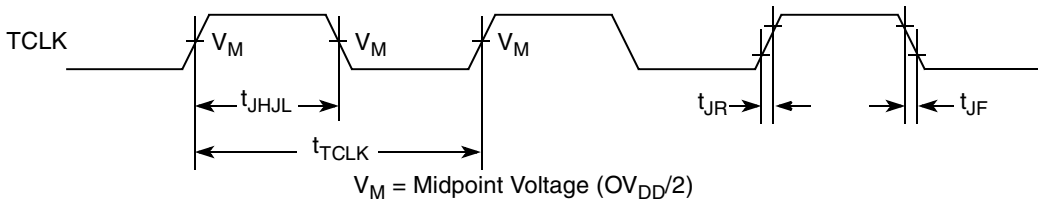

Figure 8. JTAG Clock Input Timing Diagram

Figure 9 provides the $\overline{\text{TRST}}$ timing diagram.

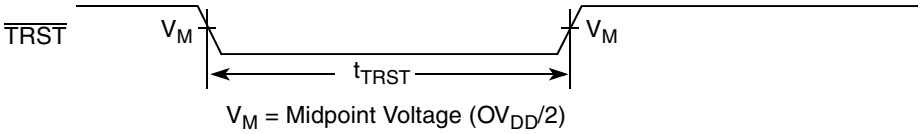

Figure 9. $\overline{\text{TRST}}$ Timing Diagram

Figure 10 provides the boundary-scan timing diagram.

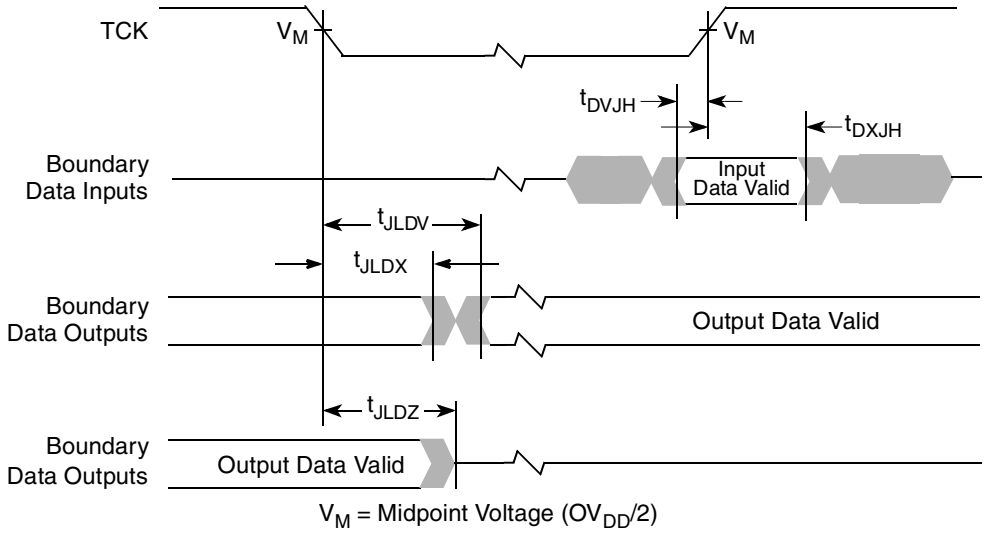

Figure 10. Boundary-Scan Timing Diagram

7 Pinout Listings

Table 12 provides the pinout listing for the MPC7447A, 360 HCTE package. The pinouts of the MPC7447A and MPC7447 are pin compatible, but there have been some changes. An MPC7447A may be populated on a board designed for a MPC7447 provided all pins defined as ‘no connect’ for the MPC7447 are unterminated as required by the *MPC7457 RISC Microprocessor Hardware Specifications*. The MPC7447A uses pins previously marked ‘no connect’ for the temperature diode pins and for additional power and ground connections. Because these ‘no connect’ pins in the MPC7447 360 pin package are not driven in functional mode, an MPC7447 can be populated in an MPC7447A board. See Section 9.4, “Connection Recommendations,” for additional information.

NOTE

Caution must be exercised when performing boundary scan test operations on a board designed for an MPC7447A but populated with an MPC7447. This is because in the MPC7447 it is possible to drive the latches associated with the former ‘no connect’ pins in the MPC7447, potentially causing contention on those pins. To prevent this, ensure that these pins are not connected on the board or, if they are connected, ensure that the states of internal MPC7447 latches do not cause these pins to be driven during board testing.

NOTE

This pinout is not compatible with the MPC750, MPC7400, or MPC7410 360 BGA and LGA package.

Table 12. Pinout Listing for the MPC7447A, 360 HCTE Package

Signal Name	Pin Number	Active	I/O	I/F Select[1]	Notes
A[0:35]	E11, H1, C11, G3, F10, L2, D11, D1, C10, G2, D12, L3, G4, T2, F4, V1, J4, R2, K5, W2, J2, K4, N4, J3, M5, P5, N3, T1, V2, U1, N5, W1, B12, C4, G10, B11	High	I/O	BVSEL	2
$\overline{\text{AACK}}$	R1	Low	Input	BVSEL	
AP[0:4]	C1, E3, H6, F5, G7	High	I/O	BVSEL	2
$\overline{\text{ARTRY}}$	N2	Low	I/O	BVSEL	3
AV_{DD}	A8	—	Input	N/A	
$\overline{\text{BG}}$	M1	Low	Input	BVSEL	
$\overline{\text{BMODE0}}$	G9	Low	Input	BVSEL	4
$\overline{\text{BMODE1}}$	F8	Low	Input	BVSEL	5
$\overline{\text{BR}}$	D2	Low	Output	BVSEL	
BVSEL	B7	High	Input	BVSEL	1, 6
$\overline{\text{CI}}$	J1	Low	Output	BVSEL	
$\overline{\text{CKSTP\_IN}}$	A3	Low	Input	BVSEL	
$\overline{\text{CKSTP\_OUT}}$	B1	Low	Output	BVSEL	

8.5 Package Parameters for the MPC7447A, 360 HCTE RoHS-Compliant BGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360 lead-free high coefficient of thermal expansion ceramic ball grid array (HCTE).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.32 mm
Maximum module height	2.80 mm
Ball diameter	0.75 mm (30 mil)
Coefficient of thermal expansion	12.3 ppm/°C

9 System Design Information

This section provides system and thermal design recommendations for successful application of the MPC7447A.

9.1 Clocks

9.1.1 PLL Configuration

The MPC7447A PLL is configured by the PLL_CFG[0:4] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the MPC7447A is shown in Table 13 for a set of example frequencies. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with the 1400 MHz column in Table 8. When enabled, dynamic frequency switching (DFS) also affects the core frequency by halving the bus-to-core multiplier; see Section 9.8.5, "Dynamic Frequency Switching (DFS)," for more information. Note that when DFS is enabled the resulting core frequency must meet the minimum core frequency requirements described in Table 8.

Table 13. MPC7447A Microprocessor PLL Configuration Example for 1420-MHz Parts

PLL_CFG[0:4]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)								
	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Bus (SYSCLK) Frequency						
			33 MHz	50 MHz	67 MHz	75 MHz	83 MHz	100 MHz	133 MHz	167 MHz
01000	2x [1]	2x								
10000	3x [1]	2x								
10100	4x [1]	2x								668 (1333)
10110	5x	2x							665 (1333)	835 (1670)
10010	5.5x	2x							732 (1466)	919 (1837)
11010	6x	2x						600 (1200)	798 (1600)	1002 (2004)
01010	6.5x	2x						650 (1300)	865 (1730)	1086 (2171)
00100	7x	2x						700 (1400)	931 (1862)	1169 (2338)
00010	7.5x	2x					623 (1245)	750 (1500)	998 (2000)	1253 (2505)
11000	8x	2x				600 (1200)	664 (1328)	800 (1600)	1064 (2128)	1336 (2672)

01100	8.5x	2x				638 (1276)	706 (1412)	850 (1700)	1131 (2261)	1420 (2833)
01111	9x	2x			603 (1200)	675 (1350)	747 (1494)	900 (1800)	1197 (2394)	
01110	9.5x	2x			637 (1266)	713 (1524)	789 (1578)	950 (1900)	1264 (2528)	
10101	10x	2x			670 (1333)	750 (1500)	830 (1660)	1000 (2000)	1330 (2667)	
10001	10.5x	2x			704 (1400)	788 (1876)	872 (1744)	1050 (2100)	1397 (2793)	
10011	11x	2x			737 (1466)	825 (1650)	913 (1826)	1100 (2200)		
00000	11.5x	2x			771 (532)	863 (1726)	955 (1910)	1150 (2300)		
10111	12x	2x		600 (1200)	804 (1600)	900 (1800)	996 (1992)	1200 (2400)		
11111	12.5x	2x		625 (1200)	838 (1666)	938 (1876)	1038 (2076)	1250 (2500)		
01011	13x	2x		650 (1300)	871 (1730)	975 (1950)	1079 (2158)	1300 (2600)		
11100	13.5x	2x		675 (1350)	905 (1800)	1013 (2026)	1121 (2242)	1350 (2700)		
11001	14x	2x		700 (1400)	938 (1866)	1050 (2100)	1162 (2324)	1400 (2800)		
00011	15x	2x		750 (1500)	1005 (2000)	1125 (2250)	1245 (2490)			
11011	16x	2x		800 (1600)	1072 (2132)	1200 (2400)	1328 (2656)			
00001	17x	2x		850 (1900)	1139 (2264)	1275 (2550)	1411 (2822)			
00101	18x	2x								

Table 14. Spread Specturm Clock Source Recommendations

At recommended operating conditions. See Table 4.

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	50	kHz	1
Frequency spread	—	1.0	%	1, 2

Notes:
1. Guaranteed by design.
2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 8.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core or bus frequency should avoid violating the stated limits by using down-spreading only.

9.2 PLL Power Supply Filtering

The AV_{DD} power signal is provided on the MPC7447A to provide power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500-KHz to 10-MHz resonant frequency range of the PLL. A circuit similar to the one shown in Figure 17 using surface-mount capacitors with minimum effective series inductance (ESL) is recommended.

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 360 HCTE footprint.

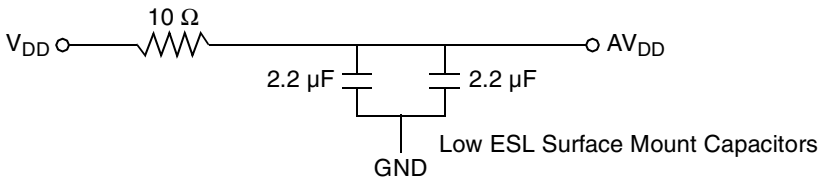

Figure 17. PLL Power Supply Filter Circuit

9.3 Decoupling Recommendations

Due to the MPC7447A dynamic power management feature, large address and data buses, and high operating frequencies, the MPC7447A can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC7447A system, and the MPC7447A itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer use sufficient decoupling capacitors, typically one capacitor for every 1–2 V_{DD} pins, and a similar or lesser number for the OV_{DD} pins, placed as close as possible to the power pins of the MPC7447A. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, OV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance.

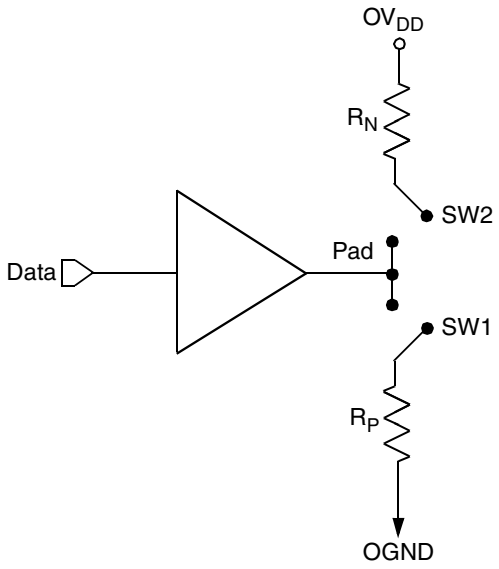

Figure 18. Driver Impedance Measurement

Table 15 summarizes the signal impedance results. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 15. Impedance Characteristics

V_{DD} = 1.5 V, OV_{DD} = 1.8 V ± 5%, T_j = 5°–85°C

Impedance		Processor Bus	Unit
Z_0	Typical	33–42	Ω
	Maximum	31–51	Ω

9.6 Pull-Up/Pull-Down Resistor Requirements

The MPC7447A requires high-resistive (weak: 4.7 KΩ) pull-up resistors on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC7447A or other bus masters. These pins are: $\overline{\text{TS}}$, $\overline{\text{ARTRY}}$, $\overline{\text{SHDO}}$, and $\overline{\text{SHD1}}$.

Some pins designated as being factory test pins must be pulled up to OV_{DD} or down to GND to ensure proper device operation. The pins that must be pulled up to OV_{DD} are: $\overline{\text{LSSD\_MODE}}$ and TEST[0:3]; the pins that must be pulled down to GND are: L1_TSTCLK and TEST[4]. The $\overline{\text{CKSTP\_IN}}$ signal should likewise be pulled up through a pull-up resistor (weak or stronger: 4.7 KΩ–1 KΩ) to prevent erroneous assertions of this signal.

In addition, the MPC7447A has one open-drain style output that requires a pull-up resistor (weak or stronger: 4.7 KΩ–1 KΩ) if it is used by the system. This pin is $\overline{\text{CKSTP\_OUT}}$.

If pull-down resistors are used to configure BVSEL, the resistors should be less than 250 Ω (see Table 12). Because PLL_CFG[0:4] must remain stable during normal operation, strong pull-up and pull-down resistors (1 KΩ or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise or noise coupling.

The COP header shown in Figure 19 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 19; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 19 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Figure 19 is usually connected to the PCI bridge chip in a system and is an input to the MPC7447A informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the MPC7447A must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is negated when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged through logic so that it also can be driven by the PCI bridge.

9.8 Thermal Management Information

This section provides thermal management information for the high coefficient of thermal expansion (HCTE) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The MPC7447A implements several features designed to assist with thermal management, including DFS and the temperature diode. DFS reduces the power consumption of the device by reducing the core frequency; see Section 9.8.5.1, "Power Consumption with DFS Enabled," for specific information regarding power reduction and DFS. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see Section 9.8.4, "Temperature Diode," for more information.

To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly (see Figure 20 and Figure 21); however, due to the potential large mass of the heat sink, attachment through the printed-circuit board is suggested. In any implementation of a heat sink solution, the force on the die should not exceed ten pounds.

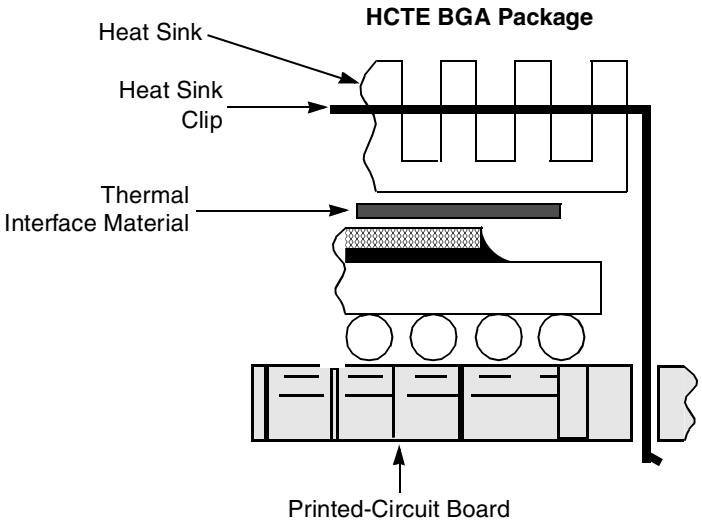

Figure 20. BGA Package Exploded Cross-Sectional View with Several Heat Sink Options

NOTE

A clip on heat sink is not recommended for LGA because there may not be adequate clearance between the device and the circuit board. A through-hole solution is recommended, as shown in Figure 21 below.

9.8.1 Internal Package Conduction Resistance

For the exposed-die packaging technology described in Table 5, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance (the case is actually the top of the exposed silicon die)

9.8.4 Temperature Diode

The MPC7447A has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. For proper operation, the monitoring device used should auto-calibrate the device by canceling out the V_{BE} variation of each MPC7447A's internal diode.

The following are the specifications of the MPC7447A on-board temperature diode:

0.40 V $< V_f <$ 0.90 V

Operating range 2–300 µA

Diode leakage < 10 nA @ 125 C

Ideality factor (n) over 5–150 µA @ 60 C: 1.0275 ± 0.9 %

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_s \left[e^{\frac{qV_f}{nKT}} - 1 \right]$$

Where:

I_{fw} = Forward current
I_s = Saturation current
V_d = Voltage at diode BM: this does not show up in any equations.
V_f = Voltage forward biased
q = Charge of electron (1.6×10^{-19} C)
n = Ideality factor (normally 1.0)
K = Boltzman's constant (1.38×10^{-23} Joules/K)
T = Temperature (Kelvins)

Another useful equation is :

$$V_H - V_L = n\frac{KT}{q} \left[ln \frac{I_H}{I_L} \right]$$

Where:

V_H = Diode voltage while I_H is flowing
V_L = Diode voltage while I_L is flowing
I_H = Larger diode bias current
I_L = Smaller diode bias current

The ratio of I_H to I_L is usually selected to be 10:1. The above simplifies to the following:

$$V_H - V_L = 1.986 \times 10^{-4} \times nT$$

Solving for T, the equation becomes:

$$nT = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

9.8.5 Dynamic Frequency Switching (DFS)

The new DFS feature in the MPC7447A adds the ability to divide the processor-to-system bus ratio by two during normal functional operation by setting the HID1[DFS2] bit. The frequency change occurs in 1 clock cycle, and no idle waiting period is required to switch between modes. Additional information regarding DFS can be found in the *MPC7450 RISC Microprocessor Family Reference Manual.*

9.8.5.1 Power Consumption with DFS Enabled

Power consumption with DFS enabled can be approximated using the following formula:

$$P_{DFS} = \left[\frac{f_{DFS}}{f}\ (P - P_{DS})\right] + P_{DS}$$

Where:

P_{DFS} = Power consumption with DFS enabled

f_{DFS} = Core frequency with DFS enabled

f = Core frequency prior to enabling DFS

P = Power consumption prior to enabling DFS (see Table 7)

P_{DS} = Deep sleep mode power consumption (see Table 7)

The above is an approximation only. Power consumption with DFS enabled is not tested or guaranteed.

9.8.5.2 Bus-to-Core Multiplier Constraints with DFS

DFS is not available for all bus-to-core multipliers as configured by PLL_CFG[0:4] during hard reset. Specifically, because the MPC7447A does not support quarter clock ratios or the 1x multiplier, the DFS feature is limited to integer PLL multipliers of 4x and higher. The complete listing is shown in Table 16.

Table 16. Valid Divide Ratio Configurations

Bus-to-Core Multiplier Configured by PLL_CFG[0:4] (see Table 13)	Bus-to-Core Multiplier with HID1[DFS1] = 1 (÷2)
2x	N/A
3x	N/A

Table 16. Valid Divide Ratio Configurations (continued)

Bus-to-Core Multiplier Configured by PLL_CFG[0:4] (see Table 13)	Bus-to-Core Multiplier with HID1[DFS1] = 1 (÷2)
4x	2x
5x	2.5x
5.5x	N/A
6x	3x
6.5x	N/A
7x	3.5x
7.5x	N/A
8x	4x
8.5x	N/A
9x	4.5x
9.5x	N/A
10x	5x
10.5x	N/A
11x	5.5x
11.5x	N/A
12x	6x
12.5x	N/A
13x	6.5x
13.5x	N/A
14x	7x
15x	7.5x
16x	8x
17x	8.5x
18x	9x
20x	10x
21x	10.5x
24x	12x
28x	14x

9.8.5.3 Minimum Core Frequency Requirements with DFS

In many systems, enabling DFS can result in very low processor core frequencies. However, care must be taken to ensure that the resulting processor core frequency is within the limits specified in Table 8. Proper operation of the device is not guaranteed at core frequencies below the specified minimum f_{core}.

10 Document Revision History

Table 17 provides a revision history for this hardware specification.

Table 17. Document Revision History

Revision Number	Date	Substantive Changes
5	01/30/2005	Corrected RoHS BGA sphere diameter dimensions
4	09/23/2005	Added RoHS BGA case outlines and part numbers. Removed note references for $\overline{CI}$ and $\overline{WT}$ in Table 12
3	08/23/2005	Added "Section 9.1.2, "System Bus Clock (SYSCLK) and Spread Spectrum Sources"
		Section 9.8, "Thermal Management Information": Added vendor to list
		Section 9.8.3, "Heat Sink Selection Example": Correct silicon die and underfil/bump model dimensions
2	02/16/2005	Changed die size
		Table 8: Modified jitter specifications to conform to JEDEC standards, changed jitter specification to cycle-to-cycle jitter (instead of long- and short-term jitter); changed jitter bandwidth recommendations.
		Added information for LGA package.
1	—	Added t_{KHTSV}, t_{KHARV}, t_{KHTSX}, and t_{KHARX} to Table 9; these were previously grouped with t_{KHOV} and t_{KHOX}. NOTE: Documentation change only; the values for the output valid and output hold AC timing specifications remain unchanged for $\overline{TS}$, $\overline{ARTRY}$, and $\overline{SHD}$[0:1].
		Added derating section with table; added 1000 MHz speed bin
0.1	—	Retitled Table 19 to include document order information for MC7447AnnnnNx series hardware specification addendum.
0	—	Initial revision.

11 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 11.1, "Part Numbers Fully Addressed by This Document." Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact a local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier that may specify special application conditions. Each part number also contains a revision level code that refers to the die mask revision number. Section 11.2, "Part Numbers Not Fully Addressed by This Document," lists the part numbers that do not fully conform to the specifications of this document. These special part numbers require an additional document called a hardware specification addendum.