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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	LINbus, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.75K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	PG-TQFP-48
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc886lm8ffa5vaclxuma1

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2 General Device Information

Chapter 2 contains the block diagram, pin configurations, definitions and functions of the SAL-XC886.

2.1 Block Diagram

The block diagram of the SAL-XC886 is shown in **Figure 2**.

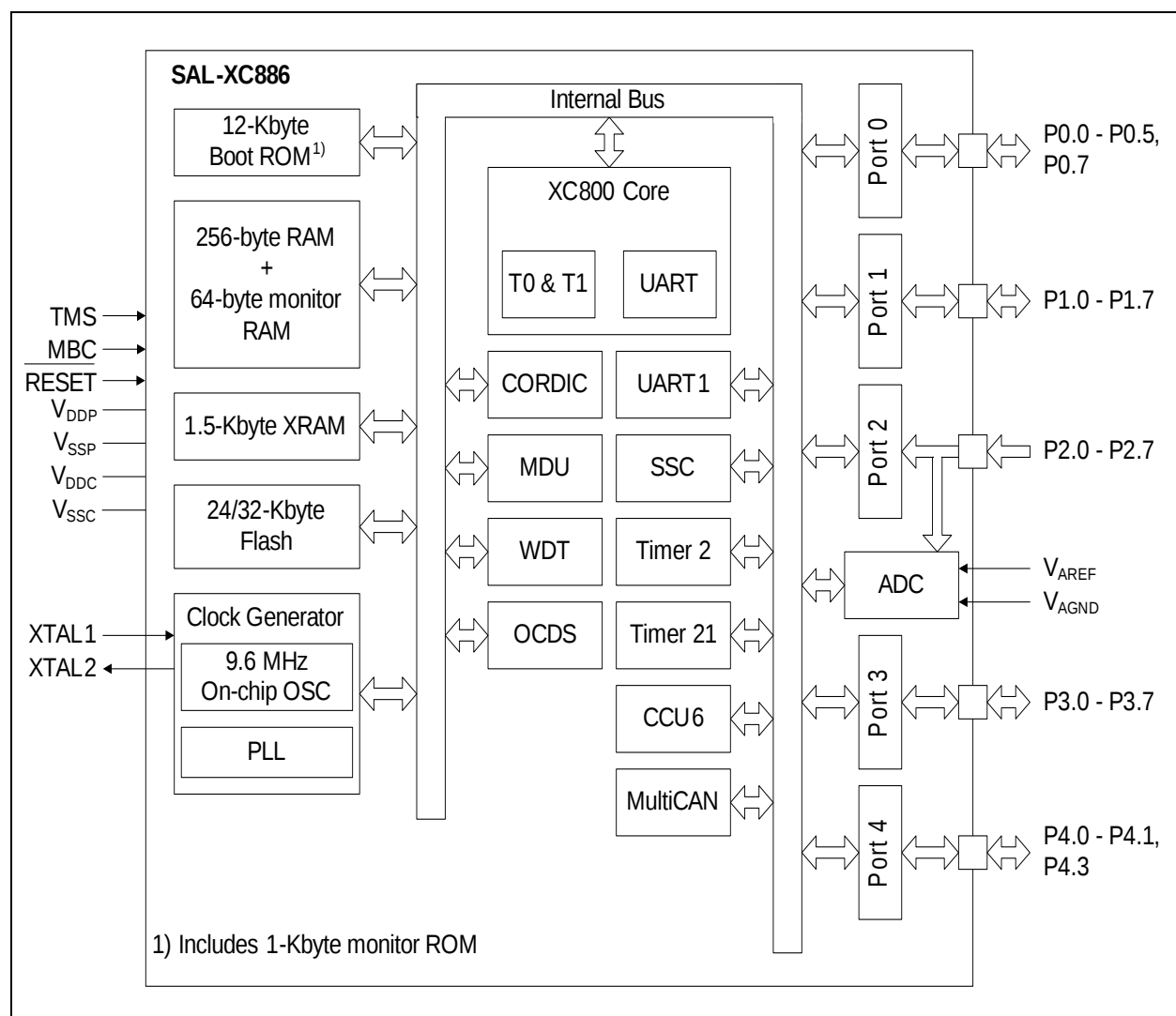


Figure 2 SAL-XC886 Block Diagram

General Device Information

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function	
P0.4	1		Hi-Z	MTSR_1	SSC Master Transmit Output/ Slave Receive Input
				CC62_1	Input/Output of Capture/Compare channel 2
				TXD1_0	UART1 Transmit Data Output/Clock Output
P0.5	2		Hi-Z	MRST_1	SSC Master Receive Input/Slave Transmit Output
				EXINT0_0	External Interrupt Input 0
				T2EX1_1	Timer 21 External Trigger Input
				RXD1_0	UART1 Receive Data Input
				COUT62_1	Output of Capture/Compare channel 2
P0.7	47		PU	CLKOUT_1	Clock Output

General Device Information

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function
P1		I/O		Port 1 Port 1 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, Timer 0, Timer 1, Timer 2, Timer 21, MultiCAN and SSC.
P1.0	26		PU	RXD_0 UART Receive Data Input T2EX Timer 2 External Trigger Input RXDC0_0 MultiCAN Node 0 Receiver Input
P1.1	27		PU	EXINT3 External Interrupt Input 3 T0_1 Timer 0 Input TDO_1 JTAG Serial Data Output TXD_0 UART Transmit Data Output/Clock Output TXDC0_0 MultiCAN Node 0 Transmitter Output
P1.2	28		PU	SCK_0 SSC Clock Input/Output
P1.3	29		PU	MTSR_0 SSC Master Transmit Output/Slave Receive Input TXDC1_3 MultiCAN Node 1 Transmitter Output
P1.4	30		PU	MRST_0 SSC Master Receive Input/ Slave Transmit Output EXINT0_1 External Interrupt Input 0 RXDC1_3 MultiCAN Node 1 Receiver Input
P1.5	31		PU	CCPOS0_1 CCU6 Hall Input 0 EXINT5 External Interrupt Input 5 T1_1 Timer 1 Input EXF2_0 Timer 2 External Flag Output RXDO_0 UART Transmit Data Output

General Device Information

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function
P1.6	8		PU	CCPOS1_1 CCU6 Hall Input 1 T12HR_0 CCU6 Timer 12 Hardware Run Input EXINT6_0 External Interrupt Input 6 RXDC0_2 MultiCAN Node 0 Receiver Input T21_1 Timer 21 Input
P1.7	9		PU	CCPOS2_1 CCU6 Hall Input 2 T13HR_0 CCU6 Timer 13 Hardware Run Input T2_1 Timer 2 Input TXDC0_2 MultiCAN Node 0 Transmitter Output P1.5 and P1.6 can be used as a software chip select output for the SSC.

General Device Information

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function
V_{DDP}	7, 17, 43	–	–	I/O Port Supply (5.0 V) Also used by EVR and analog modules. All pins must be connected.
V_{SSP}	18, 42	–	–	I/O Port Ground All pins must be connected.
V_{DDC}	6	–	–	Core Supply Monitor (2.5 V)
V_{SSC}	5	–	–	Core Supply Ground
V_{AREF}	24	–	–	ADC Reference Voltage
V_{AGND}	23	–	–	ADC Reference Ground
XTAL1	4	I	Hi-Z	External Oscillator Input (backup for on-chip OSC, normally NC)
XTAL2	3	O	Hi-Z	External Oscillator Output (backup for on-chip OSC, normally NC)
TMS	10	I	PD	Test Mode Select
RESET	41	I	PU	Reset Input
MBC¹⁾	44	I	PU	Monitor & BootStrap Loader Control

1) An external pull-up device in the range of 4.7 k Ω to 100 k Ω . is required to enter user mode. Alternatively MBC can be tied to high if alternate functions (for debugging) of the pin are not utilized.

Functional Description

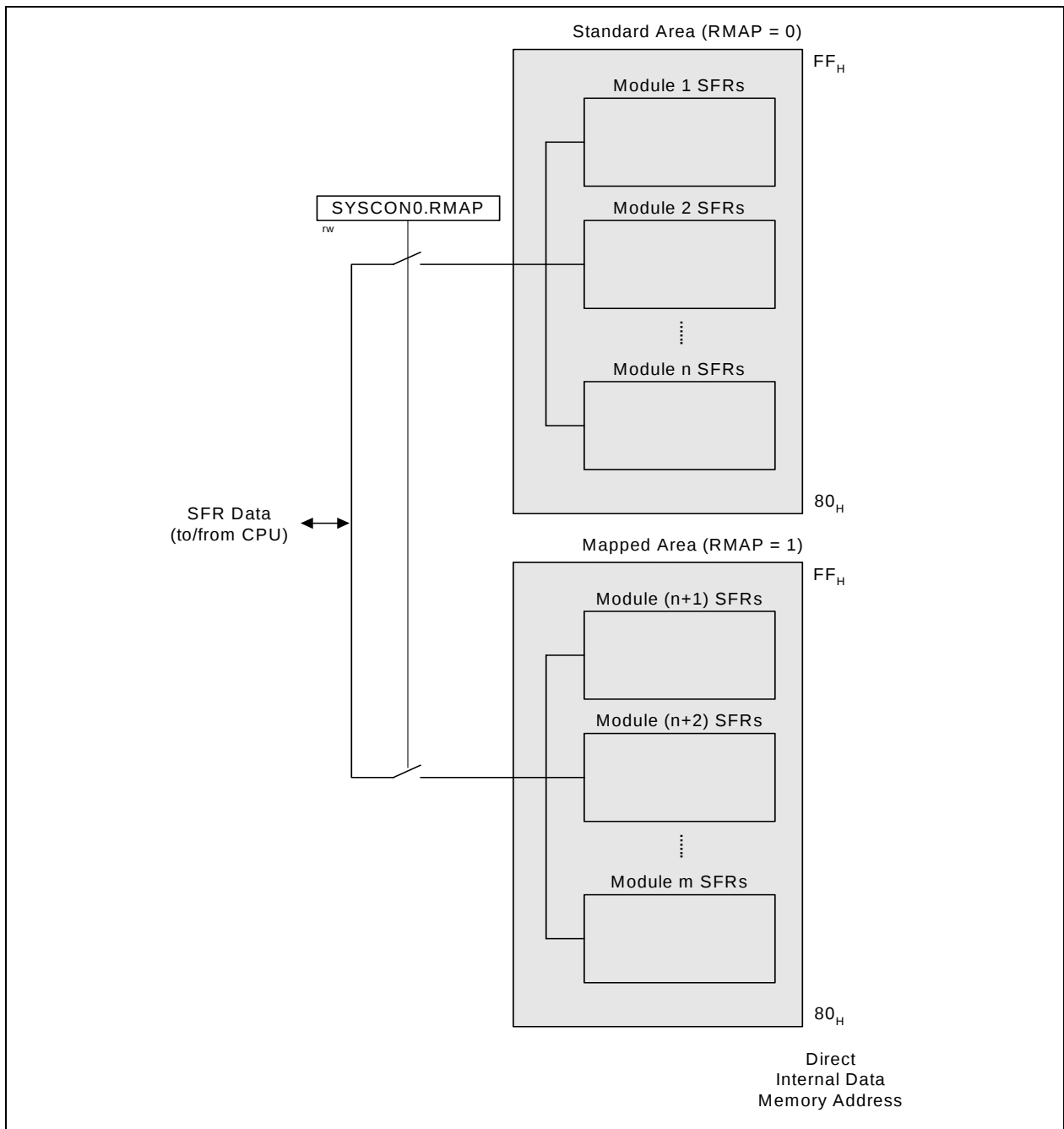


Figure 7 Address Extension by Mapping

Functional Description

The page register has the following definition:

MOD_PAGE

Page Register for module MOD

Reset Value: 00_H

7	6	5	4	3	2	1	0
OP		STNR		0	PAGE		
w		w		r	rw		

Field	Bits	Type	Description
PAGE	[2:0]	rw	Page Bits When written, the value indicates the new page. When read, the value indicates the currently active page.
STNR	[5:4]	w	Storage Number This number indicates which storage bit field is the target of the operation defined by bit field OP. If OP = 10 _B , the contents of PAGE are saved in STx before being overwritten with the new value. If OP = 11 _B , the contents of PAGE are overwritten by the contents of STx. The value written to the bit positions of PAGE is ignored. 00 ST0 is selected. 01 ST1 is selected. 10 ST2 is selected. 11 ST3 is selected.

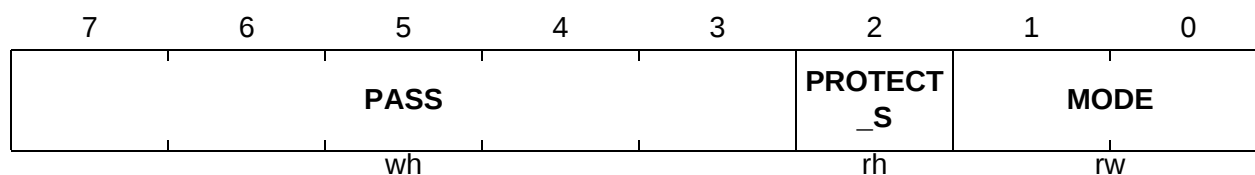
Functional Description

3.2.3.1 Password Register

PASSWD

Password Register

Reset Value: 07_H



Field	Bits	Type	Description
MODE	[1:0]	rw	Bit Protection Scheme Control Bits 00 Scheme disabled - direct access to the protected bits is allowed. 11 Scheme enabled - the bit field PASS has to be written with the passwords to open and close the access to protected bits. (default) Others: Scheme Enabled. These two bits cannot be written directly. To change the value between 11 _B and 00 _B , the bit field PASS must be written with 11000 _B ; only then, will the MODE[1:0] be registered.
PROTECT_S	2	rh	Bit Protection Signal Status Bit This bit shows the status of the protection. 0 Software is able to write to all protected bits. 1 Software is unable to write to any protected bits.
PASS	[7:3]	wh	Password Bits The Bit Protection Scheme only recognizes three patterns. 11000 _B Enables writing of the bit field MODE. 10011 _B Opens access to writing of all protected bits. 10101 _B Closes access to writing of all protected bits

Functional Description

Table 6 CORDIC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
9F _H	CD_CORDZH Reset: 00 _H CORDIC Z Data High Byte	Bit Field	DATAH							
		Type	rw							
A0 _H	CD_STATC Reset: 00 _H CORDIC Status and Data Control Register	Bit Field	KEEP Z	KEEP Y	KEEP X	DMAP	INT_E N	EOC	ERRO R	BSY
		Type	rw	rw	rw	rw	rw	rwh	rh	rh
A1 _H	CD_CON Reset: 00 _H CORDIC Control Register	Bit Field	MPS		X_USI GN	ST_M ODE	ROTV EC	MODE		ST
		Type	rw		rw	rw	rw	rw		rwh

3.2.4.4 System Control Registers

The system control SFRs can be accessed in the mapped memory area (RMAP = 0).

Table 7 SCU Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0 or 1										
8F _H	SYSCON0 Reset: 04_H System Control Register 0	Bit Field	0			IMOD E	0	1	0	RMAP
		Type	r			rw	r	r	r	rw
RMAP = 0										
BF _H	SCU_PAGE Reset: 00_H Page Register	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rw		
RMAP = 0, PAGE 0										
B3 _H	MODPISEL Reset: 00_H Peripheral Input Select Register	Bit Field	0	URRIS H	JTAGT DIS	JTAGT CKS	EXINT 2IS	EXINT 1IS	EXINT 0IS	URRIS
		Type	r	rw	rw	rw	rw	rw	rw	rw
B4 _H	IRCON0 Reset: 00_H Interrupt Request Register 0	Bit Field	0	EXINT 6	EXINT 5	EXINT 4	EXINT 3	EXINT 2	EXINT 1	EXINT 0
		Type	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh
B5 _H	IRCON1 Reset: 00_H Interrupt Request Register 1	Bit Field	0	CANS RC2	CANS RC1	ADCS R1	ADCS R0	RIR	TIR	EIR
		Type	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh
B6 _H	IRCON2 Reset: 00_H Interrupt Request Register 2	Bit Field	0			CANS RC3	0			CANS RC0
		Type	r			rwh	r			rwh
B7 _H	EXICON0 Reset: F0_H External Interrupt Control Register 0	Bit Field	EXINT3		EXINT2		EXINT1		EXINT0	
		Type	rw		rw		rw		rw	
BA _H	EXICON1 Reset: 3F_H External Interrupt Control Register 1	Bit Field	0		EXINT6		EXINT5		EXINT4	
		Type	r		rw		rw		rw	
BB _H	NMICON Reset: 00_H NMI Control Register	Bit Field	0	NMI ECC	NMI VDDP	NMI VDD	NMI OCDS	NMI FLASH	NMI PLL	NMI WDT
		Type	r	rw	rw	rw	rw	rw	rw	rw

3.3 Flash Memory

The Flash memory provides an embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data. It is operated from a single 2.5 V supply from the Embedded Voltage Regulator (EVR) and does not require additional programming or erasing voltage. The sectorization of the Flash memory allows each sector to be erased independently.

Features

- In-System Programming (ISP) via UART
- In-Application Programming (IAP)
- Error Correction Code (ECC) for dynamic correction of single-bit errors
- Background program and erase operations for CPU load minimization
- Support for aborting erase operation
- Minimum program width¹⁾ of 32-byte for D-Flash and 64-byte for P-Flash
- 1-sector minimum erase width
- 1-byte read access
- Flash is delivered in erased state (read all zeros)
- Operating supply voltage: $2.5\text{ V} \pm 7.5\%$
- Read access time: $3 \times t_{\text{CCLK}} = 150\text{ ns}^{2)}$
- Program time: $248256 / f_{\text{SYS}} = 3.1\text{ ms}^{3)}$
- Erase time: $9807360 / f_{\text{SYS}} = 123\text{ ms}^{3)}$

1) P-Flash: 64-byte wordline can only be programmed once, i.e., one gate disturb allowed.
D-Flash: 32-byte wordline can be programmed twice, i.e., two gate disturbs allowed.

2) Values shown here are typical values. $f_{\text{SYS}} = 80\text{ MHz} \pm 7.5\%$ ($f_{\text{CCLK}} = 20\text{ MHz} \pm 7.5\%$) is the maximum frequency range for Flash read access.

3) Values shown here are typical values. $f_{\text{SYS}} = 80\text{ MHz} \pm 7.5\%$ is the only frequency range for Flash programming and erasing. f_{SYSmin} is used for obtaining the worst case timing.

Functional Description

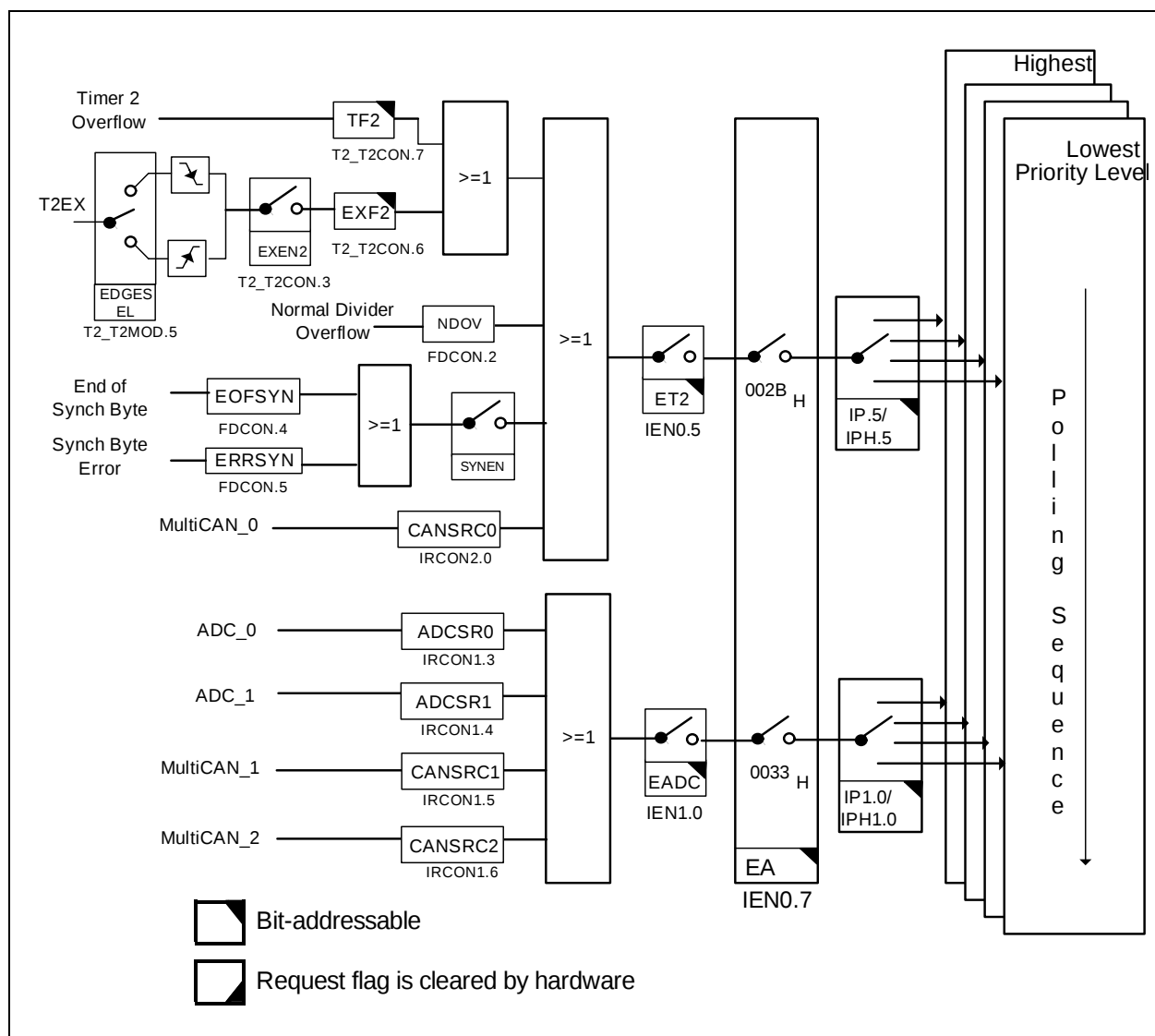


Figure 14 Interrupt Request Sources (Part 2)

Functional Description

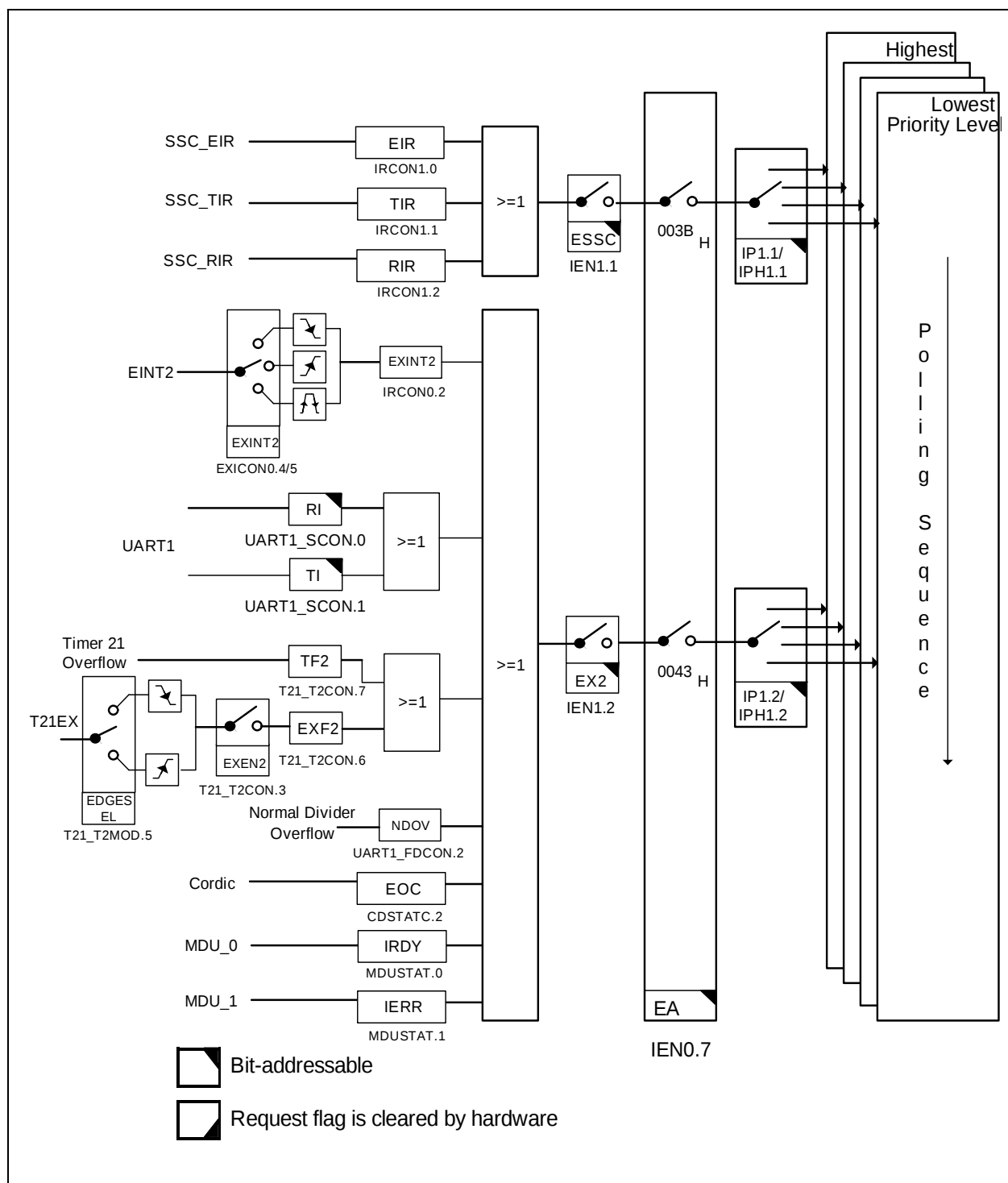


Figure 15 Interrupt Request Sources (Part 3)

Functional Description

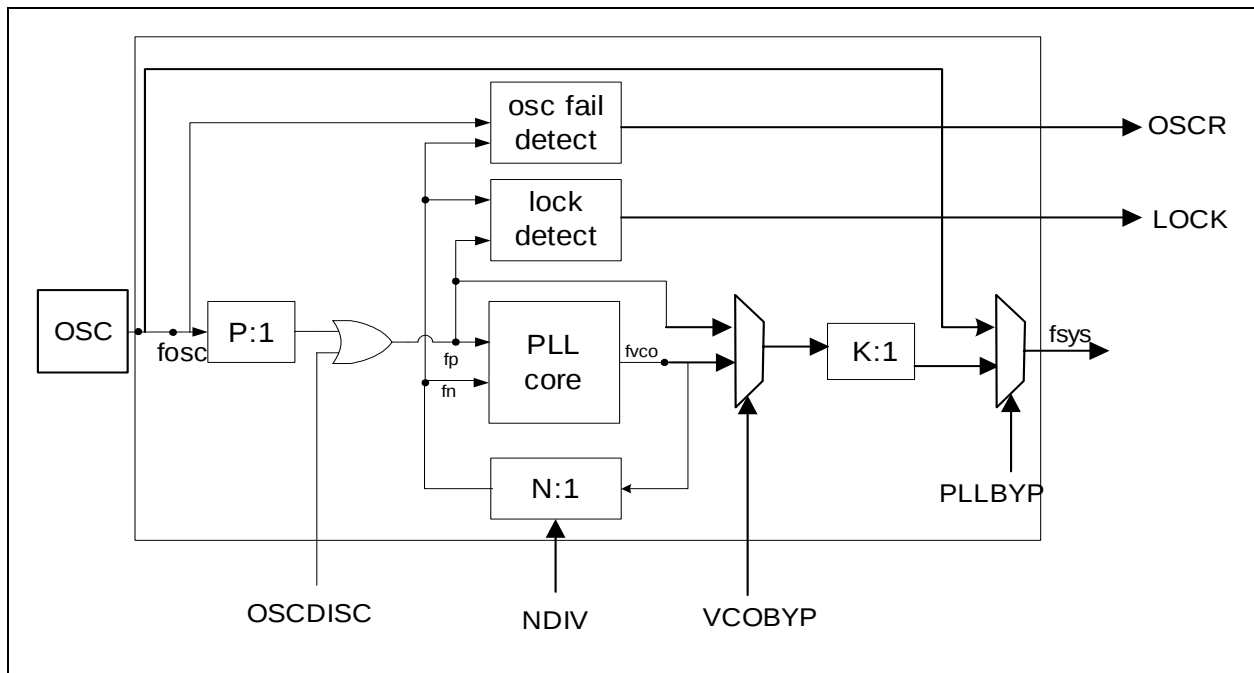


Figure 23 CGU Block Diagram

PLL Base Mode

When the oscillator is disconnected from the PLL, the system clock is derived from the VCO base (free running) frequency clock ([Table 24](#)) divided by the K factor.

$$f_{SYS} = f_{VCObase} \times \frac{1}{K}$$

(3.1)

Prescaler Mode (VCO Bypass Operation)

In VCO bypass operation, the system clock is derived from the oscillator clock, divided by the P and K factors.

$$f_{SYS} = f_{OSC} \times \frac{1}{P \times K}$$

(3.2)

Functional Description

GLOBCTR. A prescaling ratio of 32 can be selected when the maximum performance of the ADC is not required.

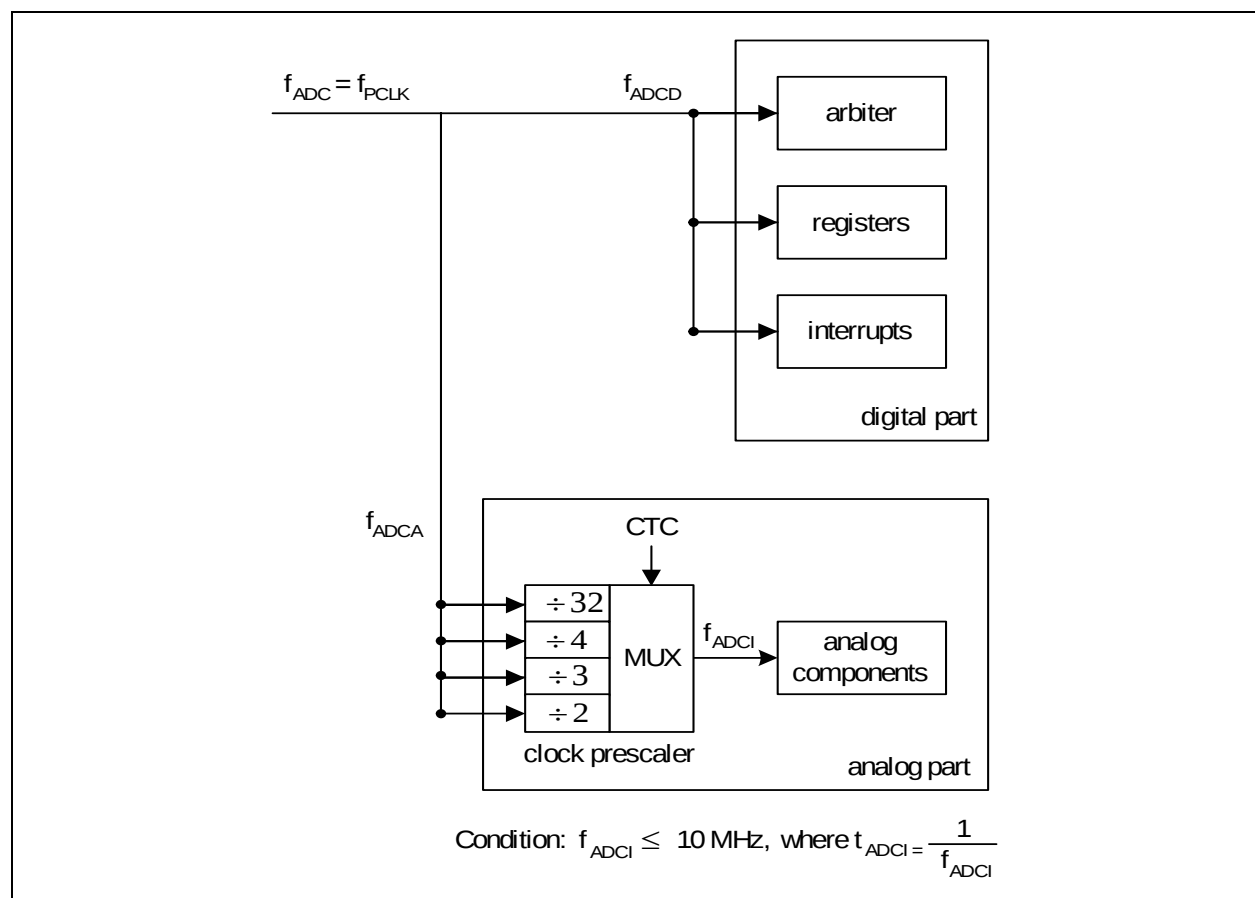


Figure 34 ADC Clocking Scheme

For module clock $f_{ADC} = 20 \text{ MHz}$, the analog clock f_{ADCI} frequency can be selected as shown in [Table 33](#).

Table 33 f_{ADCI} Frequency Selection

Module Clock f_{ADC}	CTC	Prescaling Ratio	Analog Clock f_{ADCI}
20 MHz	00 _B	$\div 2$	10 MHz
	01 _B	$\div 3$	6.67 MHz
	10 _B	$\div 4$	5 MHz
	11 _B (default)	$\div 32$	625 kHz

As f_{ADCI} cannot exceed 10 MHz, bit field CTC should not be set to 00_B when f_{ADC} is more than 20 MHz. During slow-down mode where f_{ADC} may be reduced to 10 MHz, 5 MHz etc., CTC can be set to 00_B as long as the divided analog clock f_{ADCI} does not exceed

Functional Description

10 MHz. However, it is important to note that the conversion error could increase due to loss of charges on the capacitors, if f_{ADC} becomes too low during slow-down mode.

3.21.2 ADC Conversion Sequence

The analog-to-digital conversion procedure consists of the following phases:

- Synchronization phase (t_{SYN})
- Sample phase (t_{S})
- Conversion phase
- Write result phase (t_{WR})

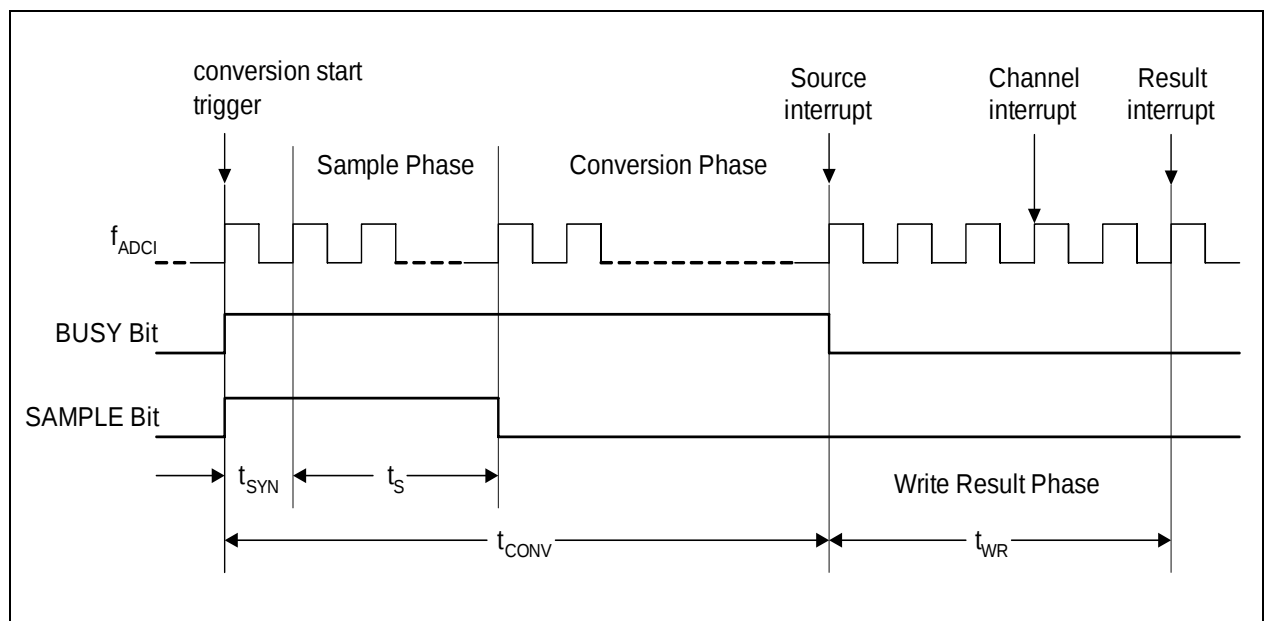


Figure 35 ADC Conversion Timing

Electrical Parameters

Table 42 Power Down Current (Operating Conditions apply; $V_{DDP} = 5V$ range)

Parameter	Symbol	Limit Values		Unit	Test Condition
		typ. ¹⁾	max. ²⁾		
V _{DDP} = 5V Range					
Power-Down Mode	I _{PDP}	1	10	μA	T _A = + 25 °C ³⁾⁴⁾
		-	30	μA	T _A = + 85 °C ⁴⁾⁵⁾

1) The typical I_{PDP} values are measured at $V_{DDP} = 5.0\text{ V}$.

2) The maximum I_{PDP} values are measured at $V_{DDP} = 5.5\text{ V}$.

3) I_{PDP} has a maximum value of $500\text{ }\mu A$ at $T_A = + 150\text{ }^{\circ}C$.

4) I_{PDP} is measured with: $\overline{RESET} = V_{DDP}$, $V_{AGND} = V_{SS}$, $RXD/INT0 = V_{DDP}$; rest of the ports are programmed to be input with either internal pull devices enabled or driven externally to ensure no floating inputs.

5) Not subjected to production test, verified by design/characterization.

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