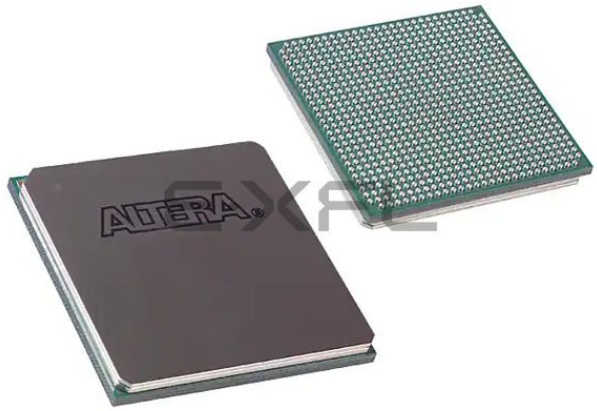

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4300
Number of Logic Elements/Cells	107500
Total RAM Bits	8936448
Number of I/O	488
Number of Gates	-
Voltage - Supply	0.86V ~ 1.15V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep3se110f780c3n

The design security feature is available when configuring Stratix III FPGAs using the fast passive parallel (FPP) configuration mode with an external host (such as a MAX II device or microprocessor), or when using fast active serial (AS) or passive serial (PS) configuration schemes.

For more information about the design security feature, refer to the *Design Security in Stratix III Devices* chapter.

SEU Mitigation

Stratix III devices have built-in error detection circuitry to detect data corruption due to soft errors in the configuration random-access memory (CRAM) cells. This feature allows all CRAM contents to be read and verified continuously during user mode operation to match a configuration-computed CRC value. The enhanced CRC circuit and frame-based configuration architecture allows detection and location of multiple, single, and adjacent bit errors which, in conjunction with a soft circuit supplied as a reference design, allows don't-care soft errors in the CRAM to be ignored during device operation. This provides a steep decrease in the effective soft error rate, increasing system reliability.

On-chip memory block SEU mitigation is also offered using the ninth bit and a configurable megafunction in the Quartus II software for MLAB and M9K blocks while the M144K memory blocks have built-in error correction code (ECC) circuitry.

For more information about the dedicated error detection circuitry, refer to the *SEU Mitigation in Stratix III Devices* chapter.

Programmable Power

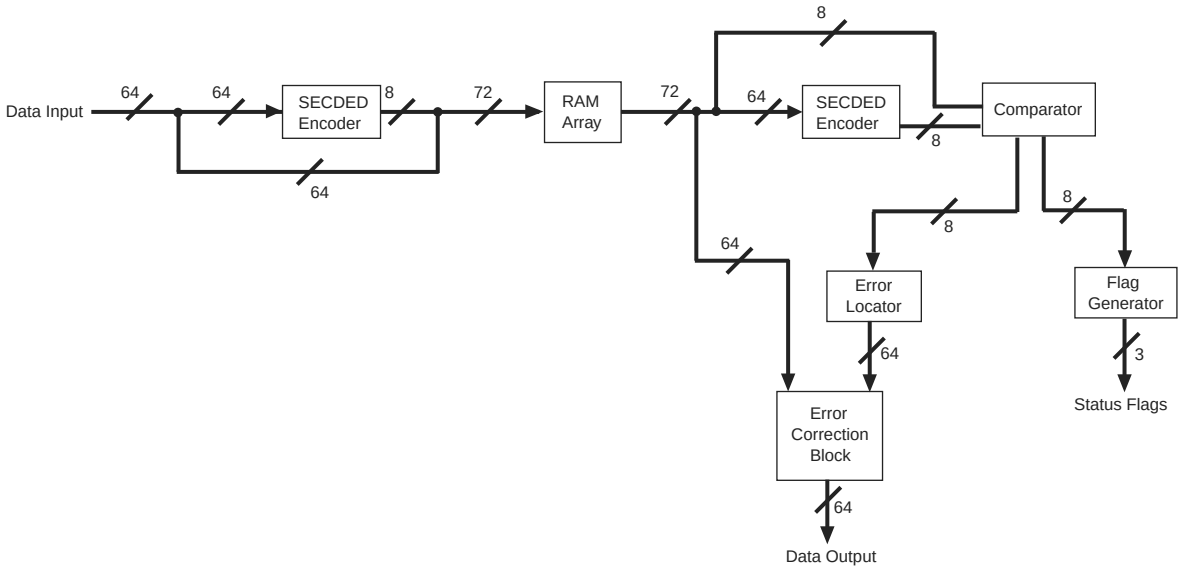
Stratix III delivers Programmable Power, the only FPGA with user programmable power options balancing today's power and performance requirements. Stratix III devices utilize the most advanced power-saving techniques, including a variety of process, circuit, and architecture optimizations and innovations. In addition, user controllable power reduction techniques provide an optimal balance of performance and power reduction specific for each design configured into the Stratix III FPGA. The Quartus II software (starting from version 6.1) automatically optimizes designs to meet the performance goals while simultaneously leveraging the programmable power-saving options available in the Stratix III FPGA without the need for any changes to the design flow.

For more information about Programmable Power in Stratix III devices, refer to the following documents:

- *Programmable Power and Temperature Sensing Diode in Stratix III Devices* chapter
- *AN 437: Power Optimization in Stratix III FPGAs*
- *Stratix III Programmable Power White Paper*

Figure 4–8 shows a block diagram of the ECC block of the M144K.

Figure 4–8. ECC Block Diagram of the M144K



Memory Modes

Stratix III TriMatrix memory blocks allow you to implement fully synchronous SRAM memory in multiple modes of operation. M9K and M144K blocks do not support asynchronous memory (unregistered inputs). MLABs support asynchronous (flow-through) read operations.

Depending on which TriMatrix memory block you target, the following modes may be used:

- Single-port
- Simple dual-port
- True dual-port
- Shift-register
- ROM
- FIFO

When using the memory blocks in ROM, single-port, simple dual-port, or true dual-port mode, you can corrupt the memory contents if you violate the setup or hold-time on any of the memory block input registers. This applies to both read and write operations.

Single Port RAM

All TriMatrix memory blocks support single-port mode. Single-port mode allows you to do either one read or one write operation at a time. Simultaneous reads and writes are not supported in single-port mode. Figure 4–9 shows the single-port RAM configuration.

Chapter Revision History

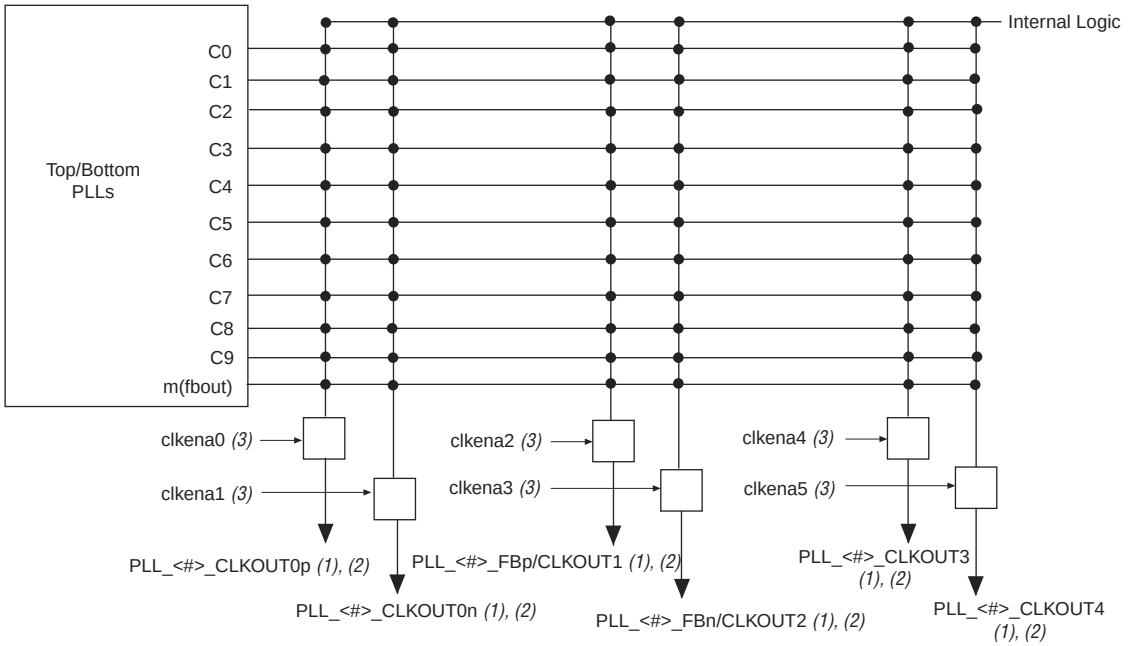
Table 4–10 shows the revision history for this chapter.

Table 4–10. Chapter Revision History

Date and Revision	Changes Made	Summary of Changes
May 2009, version 1.8	■ Updated Table 4–1. ■ Updated "Read/Write Clock Mode" and "Simple Dual-Port Mode" sections.	—
February 2009, version 1.7	■ Updated Figure 4–2, Figure 4–4, and Figure 4–5. ■ Removed "Referenced Documents" section.	—
November 2008, Version 1.6	■ Updated "Byte-Enable Support", "Address Clock Enable Support", "Asynchronous Clear", "Single Port RAM", and "Simple Dual-Port Mode" sections. ■ Updated Figure 4–1, Figure 4–5, Figure 4–8, Figure 4–10, and Figure 4–15. ■ Added Figure 4–2, Figure 4–6, Figure 4–11, Figure 4–14, and Figure 4–16.	—
October 2008, version 1.5	■ Updated Table 4–1. ■ Updated "Asynchronous Clear" and "Clocking Modes" section. ■ Added "Programming File Compatibility" section. ■ Updated New Document Format.	—
May 2008, version 1.4	■ Updated "Introduction" section. ■ Updated "TriMatrix Memory Block Types" section. ■ Updated "Byte-Enable Support" section. ■ Updated "Mixed Width Support" section. ■ Updated "Same-Port Read-During-Write Mode" section. ■ Updated Figure 4–16, Figure 4–17, and Figure 4–18. ■ Updated "Mixed-Port Read-During-Write Mode" section. ■ Updated Table 4–1, Table 4–2, and Table 4–4.	—
November 2007, version 1.3	Updated Table 4–2.	—
October 2007, version 1.2	■ Updated Table 4–1. ■ Added section "Referenced Documents". ■ Added live links for references.	—
May 2007, version 1.1	Updated Table 4–2, Table 4–9.	—
November 2006, version 1.0	Initial Release.	—

Figure 6–20 shows the clock I/O pins associated with Top/Bottom PLLs.

Figure 6–20. External Clock Outputs for Top/Bottom PLLs



Notes to Figure 6–20:

(1) These clock output pins can be fed by any one of the C[9..0], m counters.

(2) The CLKOUT0p and CLKOUT0n pins can be either single-ended or differential clock outputs. CLKOUT1 and CLKOUT2 pins are dual-purpose I/O pins that can be used as two single-ended outputs, one differential external feedback input pin pair or one single-ended external feedback input pin (CLKOUT1 only). CLKOUT3 and CLKOUT4 pins are two single-ended output pins.

(3) These external clock enable signals are available only when using the ALTCLKCTRL megafunction.

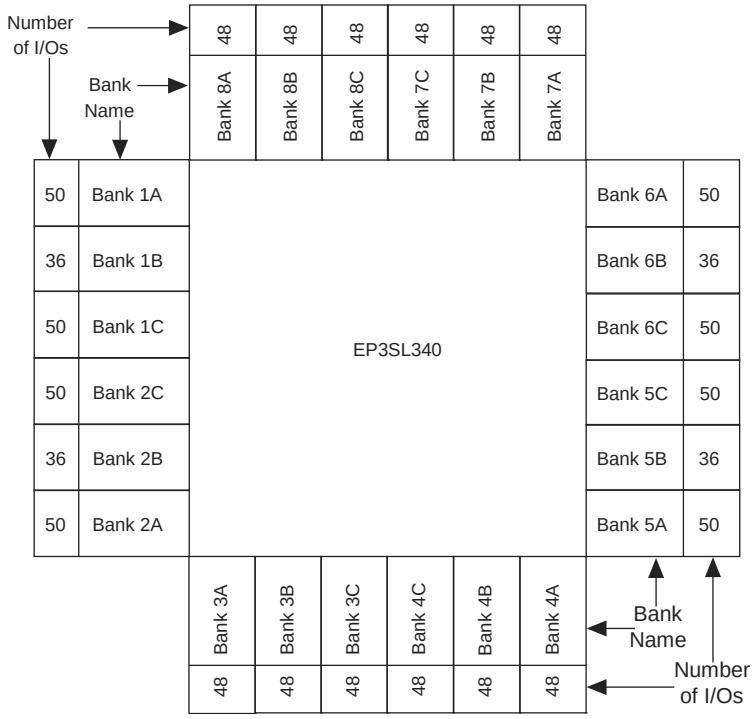
Any of the output counters (C[9..0] on Top/Bottom PLLs and C[6..0] on Left/Right PLLs) or the M counter can feed the dedicated external clock outputs, as shown in Figure 6–20 and Figure 6–21. Therefore, one counter or frequency can drive all output pins available from a given PLL.

Each Left/Right PLL supports two clock I/O pins, configured as either two single-ended I/Os or one differential I/O pair. When using both pins as single-ended I/Os, one of them can be the clock output while the other pin is the external feedback input (FB) pin. Hence, Left/Right PLLs only support external feedback mode for single-ended I/O standards.

Table 6–23. Chapter Revision History (Part 2 of 2)

Date	Version	Changes Made
October 2007	1.2	■ Updated Table 6–13 to remove a reference to gated locks. Updated Table 6–16 and added new rows to it. ■ Modified Figure 6–3 and Figure 6–40. ■ Edited notes for Figure 6–9, Figure 6–10, and Figure 6–17. ■ Replaced Figure 6–41. ■ Added section “Referenced Documents”. ■ Added live links for references.
May 2007	1.1	Changed frequency difference between inclk0 and inclk1 to more than 20% instead of 100% on page 42. Updated Table 6–16, note to Figure 6–17, and Figure 6–19.
November 2006	1.0	Initial Release.

Figure 7–6. Number of I/Os in Each Bank in EP3SL340 Devices in the 1760-pin FineLine BGA Package *(Note 1), (2)*



Notes to Figure 7–6:

(1) All I/O pin counts include dedicated clock inputs pins. The pin count includes all general purpose I/O, dedicated clock pins, and dual-purpose configuration pins. Dedicated configuration pins are not included in the pin count.

(2) Figure 7–6 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

Stratix III I/O Structure

The I/O element (IOE) in Stratix III devices contains a bi-directional I/O buffer and I/O registers to support a complete embedded bi-directional single data rate or DDR transfer. The IOEs are located in I/O blocks around the periphery of the Stratix III device. There are up to four IOEs per row I/O block and four IOEs per column I/O block. The row IOEs drive row, column, or direct link interconnects. The column IOEs drive column interconnects.

The Stratix III bi-directional IOE also supports the following features:

- Programmable input delay
- Programmable output-current strength
- Programmable slew rate
- Programmable output delay
- Programmable bus-hold
- Programmable pull-up resistor
- Open-drain output
- On-chip series termination with calibration

Table 7–5. Programmable Current Strength *(Note 1)*

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA) for Column I/O Pins	I_{OH} / I_{OL} Current Strength Setting (mA) for Row I/O Pins
3.3-V LVTTL	16, 12, 8, 4	12, 8, 4
3.3-V LVCMOS	16, 12, 8, 4	8, 4
3.0-V LVTTL	16, 12, 8, 4	12, 8, 4
3.0-V LVCMOS	16, 12, 8, 4	8, 4
2.5-V LVTTL/LVCMOS	16, 12, 8, 4	12, 8, 4
1.8-V LVTTL/LVCMOS	12, 10, 8, 6, 4, 2	8, 6, 4, 2
1.5-V LVTTL/LVCMOS	12, 10, 8, 6, 4, 2	8, 6, 4, 2
1.2-V LVTTL/LVCMOS	8, 6, 4, 2	4, 2
SSTL-2 Class I	12, 10, 8	12, 8
SSTL-2 Class II	16	16
SSTL-18 Class I	12, 10, 8, 6, 4	12, 10, 8, 6, 4
SSTL-18 Class II	16, 8	16, 8
SSTL-15 Class I	12, 10, 8, 6, 4	8, 6, 4
SSTL-15 Class II	16, 8	—
HSTL-18 Class I	12, 10, 8, 6, 4	12, 10, 8, 6, 4
HSTL-18 Class II	16	16
HSTL-15 Class I	12, 10, 8, 6, 4	8, 6, 4
HSTL-15 Class II	16	—
HSTL-12 Class I	12, 10, 8, 6, 4	8, 6, 4
HSTL-12 Class II	16	—

Note to Table 7–5:

(1) The default setting in the Quartus II software is 50-Ω OCT R_S without calibration for all non-voltage reference and HSTL/SSTL class I I/O standards. The default setting is 25-Ω OCT R_S without calibration for HSTL/SSTL class II I/O standards.

Altera recommends performing IBIS or SPICE simulations to determine the right current strength setting for your specific application.

Programmable Slew Rate Control

The output buffer for each Stratix III device regular- and dual-function I/O pin has a programmable output slew-rate control that you can configure for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. A slow slew rate can help reduce system noise, but adds a nominal delay to rising and falling edges. Each I/O pin has an individual slew-rate control, allowing you to specify the slew rate on a pin-by-pin basis.

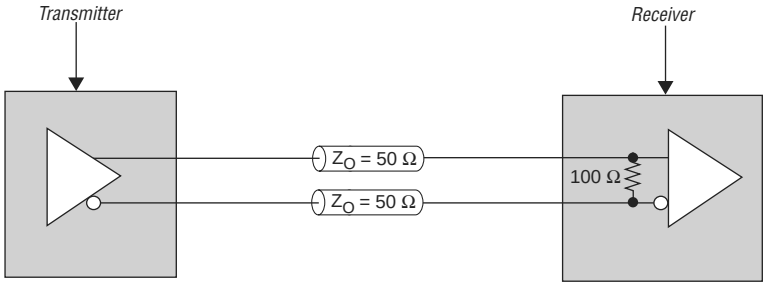
You cannot use the programmable slew rate feature when using OCT R_S.

The Quartus II software allows four settings for programmable slew rate control—0, 1, 2, and 3—where 0 is slow slew rate and 3 is fast slew rate. Table 7–6 lists the default setting for the I/O standards supported in the Quartus II software.

LVDS Input On-Chip Termination (R_D)

Stratix III devices support OCT for differential LVDS input buffers with a nominal resistance value of 10 Ω, as shown in Figure 7–12. You can enable OCT R_D in row I/O banks when V_{CCIO} and V_{CCPD} are set to 2.5 V. The column I/O banks do not support OCT R_D. The dedicated clock input pairs `CLK[1,3,8,10][p,n]`, `PLL_L[1,4]_CLK[p,n]`, and `PLL_R[1,4]_CLK[p,n]` on the row I/O banks of the Stratix III devices do not support OCT R_D. Dedicated clock input pairs `CLK[0,2,9,11][p,n]` on row I/O banks support OCT R_D. Dedicated clock input pairs `CLK[4,5,6,7][p,n]` and `CLK[12,13,14,15][p,n]` on column I/O banks do not support OCT R_D.

Figure 7–12. Differential Input On-Chip Termination



For more information about OCT R_D, refer to the *High Speed Differential I/O Interfaces with DPA in Stratix III Devices* chapter.

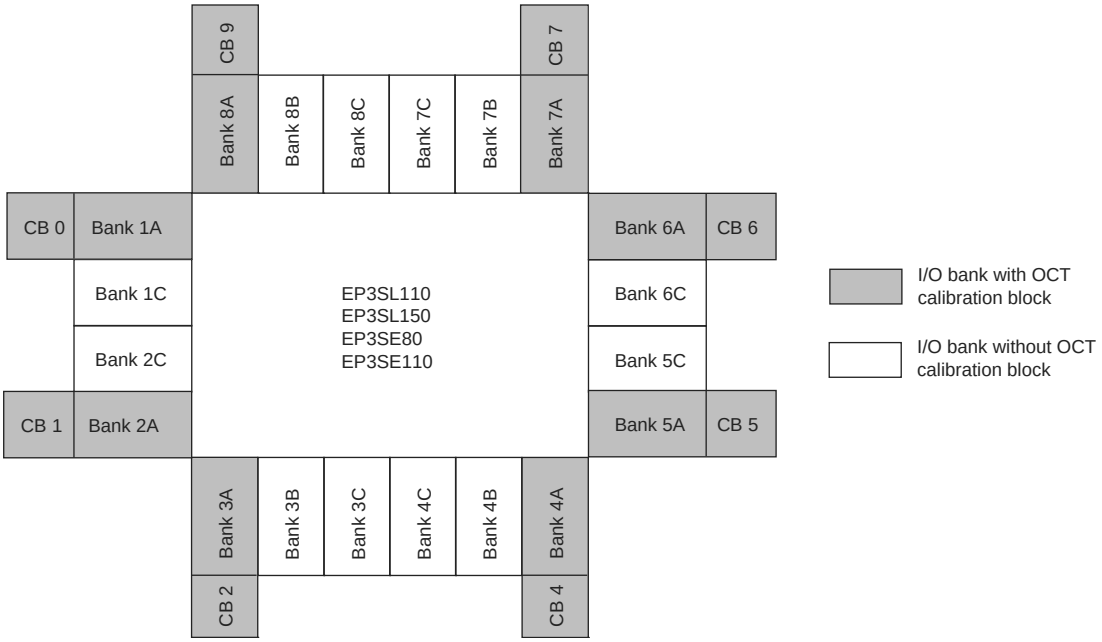
Table 7–11 lists the assignment name and its value for OCT R_D in the Quartus II software Assignment Editor.

You must set the V_{CCIO} to 2.5 V when OCT R_D is used for the LVDS input buffer, even if the LVDS input buffer is powered by V_{CCPD}.

Table 7–11. On-Chip Differential Termination in Quartus II Software Assignment Editor

Assignment Name	Allowed Values	Applies To
Input Termination (Accepts wildcards/groups)	Parallel 50 Ω with calibration	Input buffers for single-ended and differential-HSTL/SSTL standards
	Differential	Input buffers for LVDS receivers on row I/O banks.
Output Termination	Series 25 Ω without calibration	Output buffers for single-ended LVTTL/LVCMOS and HSTL/SSTL standards as well as differential HSTL/SSTL standards.
	Series 50 Ω without calibration	
	Series 25 Ω with calibration	
	Series 40 Ω with calibration	
	Series 50 Ω with calibration	
	Series 60 Ω with calibration	

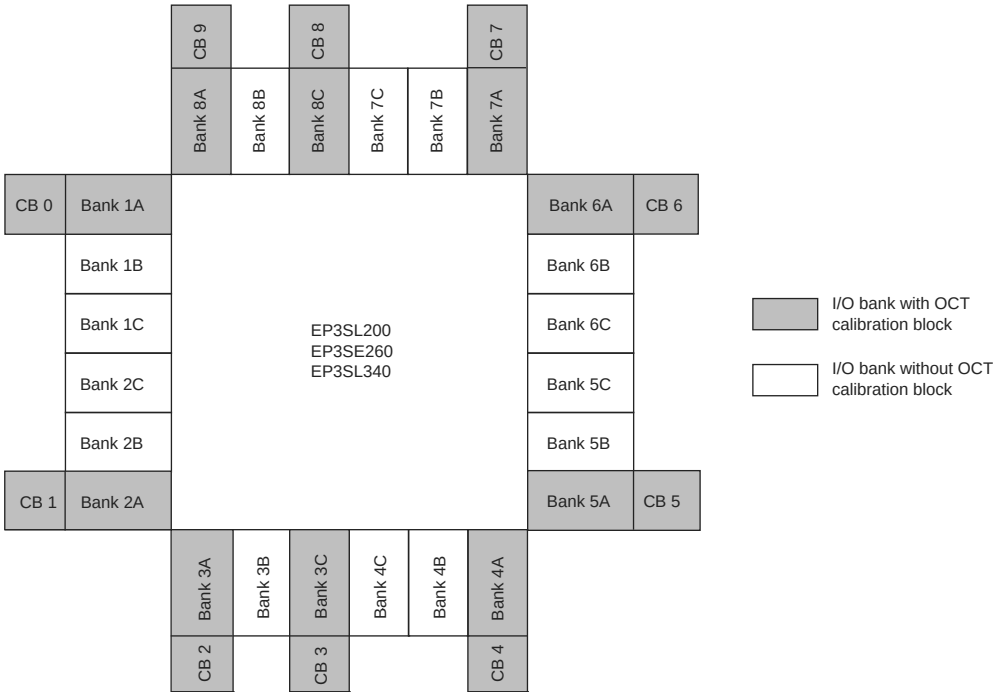
Figure 7–14. OCT Calibration Block (CB) Location in EP3SL110, EP3SL150, EP3SE80, and EP3SE110 Devices *(Note 1)*



Note to Figure 7–14:

(1) Figure 7–14 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

Figure 7–15. OCT Calibration Block (CB) Location in EP3SL200, EP3SE260 and EP3SL340 *(Note 1)*



Note to Figure 7–15:

(1) Figure 7–15 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

8. External Memory Interfaces in Stratix III Devices

SIII51008-1.9

The Stratix® III I/O structure has been completely redesigned to provide flexible, high-performance support for existing and emerging external memory standards. These include high-performance double data rate (DDR) memory standards such as DDR3, DDR2, DDR SDRAM, QDR II+, QDR II SRAM, and RLDRAM II.

Packed with features such as dynamic on-chip termination (OCT), trace mismatch compensation, read and write leveling, half data rate (HDR) blocks, and 4- to 36- bit programmable DQ group widths, Stratix III I/O elements provide easy-to-use built-in functionality required for a rapid and robust implementation.

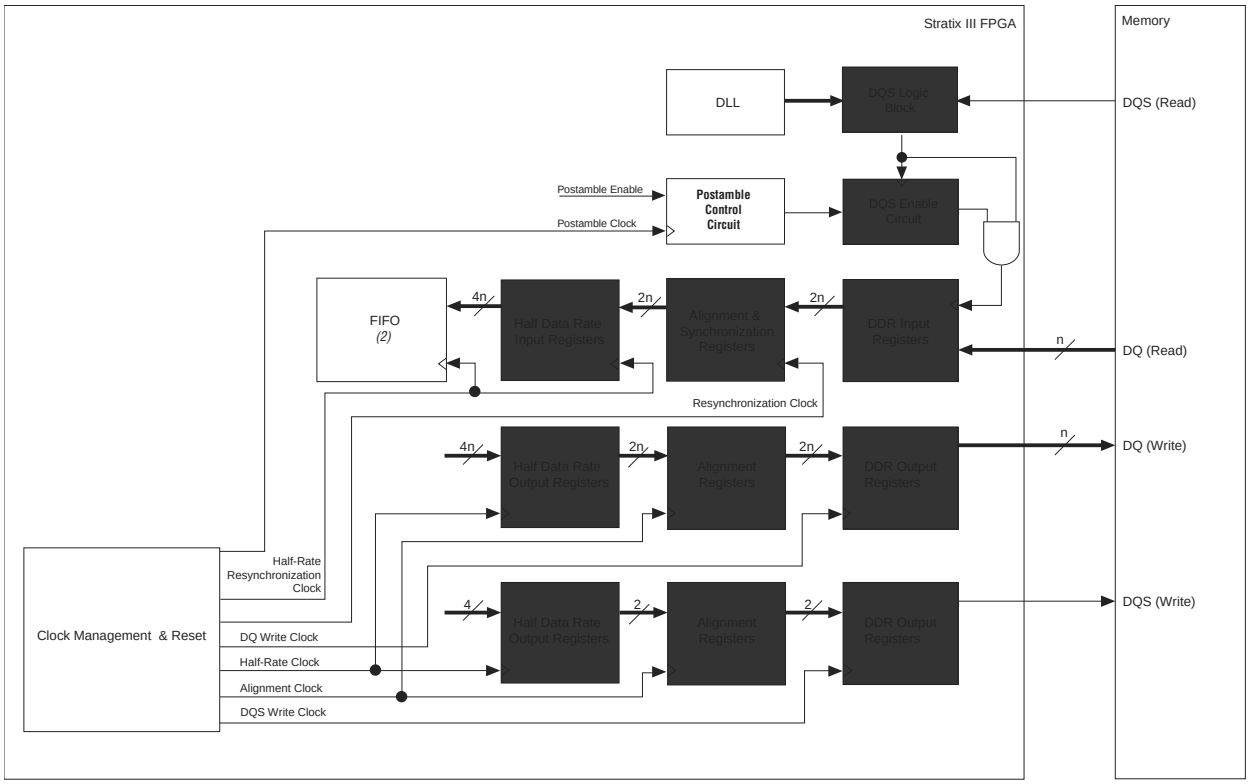
DDR external memory support is found on all sides of the Stratix III FPGA. Stratix III devices provide an efficient architecture to quickly and easily fit wide external–memory interfaces with the new small modular I/O bank structure.

A self-calibrating megafunction (ALTMEMPHY) is optimized to take advantage of the Stratix III I/O structure, along with the Quartus® II software's TimeQuest Timing Analyzer, which provides the total solution for the highest reliable frequency of operation across process, voltage, and temperature (PVT) variations.

While this chapter describe the silicon capability of Stratix III devices, for more information about the external memory system specifications, implementation, board guidelines, timing analysis, simulation, and design debugging, refer to the Literature: External Memory Interfaces section of the Altera website.

Figure 8–2 shows an overview of the memory interface data path that uses all the Stratix III I/O Element (IOE) features.

Figure 8–2. External Memory Interface Data Path Overview *(Note 1)*, *(2)*, *(3)*



Notes to Figure 8–2:

(1) Each register block can be bypassed.

(2) The blocks for each memory interface may differ slightly.

(3) These signals may be bi-directional or uni-directional, depending on the memory standard. When bi-directional, the signal is active during both read and write operations.

This chapter describes the hardware features in Stratix III devices that facilitate high-speed memory interfacing for each DDR memory standard. Stratix III devices feature DLLs, PLLs, dynamic OCT, read and write leveling, and deskew ciruitry.

Memory Interfaces Pin Support

A typical memory interface requires data (D, Q, or DQ), data strobe (DQS/CQ and DQSn/CQn), address, command, and clock pins. Some memory interfaces use data mask (DM) pins to enable write masking and QVLD pins to indicate that the read data is ready to be captured. This section describes how Stratix III devices support all these different pins.

For more information on memory interfaces, refer to the *Stratix III Pin Connection Guidelines*.

Figure 8–6. Number of DQS/DQ Groups per Bank in EP3SL200, EP3SE260 and EP3SL340 Devices in the 1517-pin FineLine BGA Package

Notes to Figure 8–6:

(1) You can also use DQS/DQSn pins in some of the ×4 groups as RUP/RDN pins. You cannot use a ×4 group for memory interfaces if two pins of the group are being used as RUP and RDN pins for OCT calibration. You can still use the ×16/×18 or ×32/×36 groups that includes these ×4 groups. However, there are restrictions on using ×8/×9 groups that include these ×4 groups as described on page 8–5.

(2) Some of the DQS/DQ pins in this bank can also be used as configuration pins. Choose the DQS/DQ pins that are not going to be used by your configuration scheme.

(3) All I/O pin counts include eight dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n, CLK8p, CLK8n, CLK10p, and CLK10n) and eight dedicated corner PLL clock inputs (PLL_L1_CLKp, PLL_L1_CLKn, PLL_L4_CLKp, PLL_L4_CLKn, PLL_R4_CLKp, PLL_R4_CLKn, PLL_R1_CLKp, and PLL_R1_CLKn) that can be used for data inputs.

Table 8–13. Chapter Revision History (Part 2 of 2)

Date and Revision	Changes Made	Summary of Changes
November 2007, version 1.3	■ Updated Table 8–5. ■ Updated Figure 8–6.	Minor updates to content.
October 2007, version 1.2	■ Updated Table 8–1, Table 8–3, Table 8–4, Table 8–5. ■ Added Table 8–2. ■ Minor text edits. ■ Updated Figure 8–3, note 3 to Figure 8–4, note 3 to Figure 8–5, note 2 to Figure 8–6, added a note to Figure 8–7, added a note and updated Figure 8–10, notes to Figure 8–11, and updated Figure 8–12. ■ Added new material to “Memory Clock Pins” on page 8–21. ■ Added section “Referenced Documents”. ■ Added live links for references.	Minor updates to content.
May 2007, version 1.1	■ Updated Figure 8–5, Figure 8–8, Figure 8–14, Figure 8–18, Figure 8–19, Figure 8–20, and Figure 8–21. ■ Added new figure, Figure 8–17. ■ Added memory support information for -4L in Table 8–1, Table 8–8, Table 8–10, and Table 8–11. ■ Added new material to section “Phase Offset Control” on page 8–32.	Minor updates to content.
November 2006, version 1.0	Initial Release.	—

Remote System Upgrade

Stratix III devices contain the remote update feature. For more information about this feature, refer to the *Remote System Upgrades with Stratix III Devices* in volume 1 of the *Stratix III Device Handbook*.

Power-On Reset Circuit

The POR circuit keeps the entire system in reset until the power supply voltage levels have stabilized on power-up. On power-up, the device does not release nSTATUS until V_{CCPT}, V_{CCL}, V_{CC}, V_{CCPD}, and V_{CCPGM} are above the device's POR trip point. On power down, brown-out occurs if V_{CC} or V_{CCL} ramps down below the POR trip point and V_{CC}, V_{CCPD}, or V_{CCPGM} drops below the threshold voltage.

In Stratix III devices, a pin-selectable option (PORSEL) is provided that allows you to select a typical POR time setting of 12 ms or 100 ms. In both cases, you can extend the POR time by using an external component to assert the nSTATUS pin low.

V_{CCPGM} Pins

Stratix III devices offer a new power supply, V_{CCPGM}, for all the dedicated configuration pins and dual function pins. The configuration voltages supported are 1.8 V, 2.5 V, 3.0 V, and 3.3 V. Stratix III devices do not support the 1.5 V configuration.

Use this pin to power all dedicated configuration inputs, dedicated configuration outputs, dedicated configuration bi-directional pins, and some of the dual functional pins that you use for configuration. With V_{CCPGM}, configuration input buffers do not have to share power lines with the regular I/O buffer in Stratix III devices.

The operating voltage for the configuration input pin is independent of the I/O bank's power supply V_{CCIO} during the configuration. Therefore, no configuration voltage constraints on V_{CCIO} are needed in Stratix III devices.

V_{CCPD} Pins

Stratix III devices have a dedicated programming power supply, V_{CCPD}, which must be connected to 3.3 V/3.0 V/2.5 V to power the I/O pre-drivers, the JTAG input and output pins (TCK, TMS, TDI, TDO, and TRST), and the design security circuitry.

V_{CCPGM} and V_{CCPD} must ramp up from 0 V to the desired voltage level within 100 ms. If these supplies are not ramped up within this specified time, your Stratix III device will not configure successfully. If your system does not allow ramp-up time of 100 ms or less, you must hold nCONFIG low until all power supplies are stable.

For more information about the configuration pins power supply, refer to "Device Configuration Pins" on page 11–43.

By stopping DCLK, the configuration circuit allows enough clock cycles to process the last byte of latched configuration data. When the clock restarts, the MAX II device must provide data on the DATA[7..0] pins prior to sending the first DCLK rising edge.

If an error occurs during configuration, the device drives its nSTATUS pin low, resetting itself internally. The low signal on the nSTATUS pin also alerts the MAX II device that there is an error. If the **Auto-restart configuration after error** option (available in the Quartus II software on the **General** tab of the **Device and Pin Options** dialog box) is turned on, the device releases nSTATUS after a reset time-out period (maximum of 100 µs). After nSTATUS is released and pulled high by a pull-up resistor, the MAX II device can try to reconfigure the target device without needing to pulse nCONFIG low. If this option is turned off, the MAX II device must generate a low-to-high transition (with a low pulse of at least 2 µs) on nCONFIG to restart the configuration process.

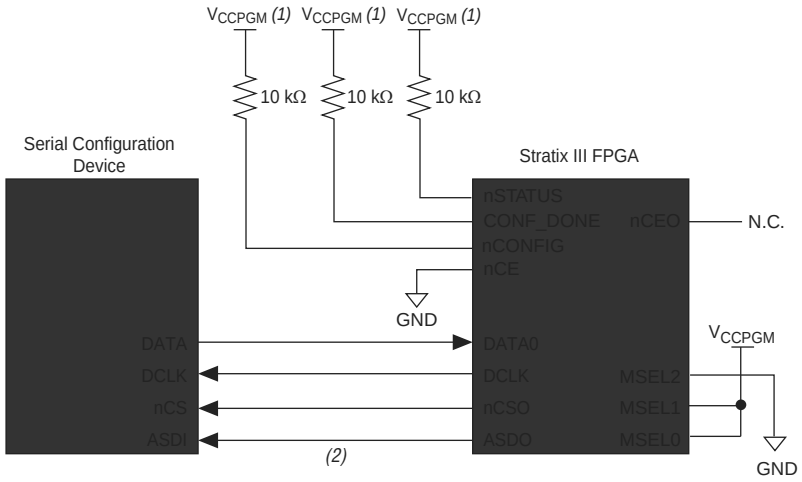
If you have enabled the **Auto-restart configuration after error** option, the nSTATUS pin transitions from high to low and back again to high when a configuration error is detected. This appears as a low pulse at the nSTATUS pin with a minimum pulse width of 10 µs to a maximum pulse width of 500 µs, as defined in the t_{STATUS} specification.

The MAX II device can also monitor the CONF_DONE and INIT_DONE pins to ensure successful configuration. The MAX II device must monitor the CONF_DONE pin to detect errors and determine when programming completes. If all configuration data is sent, but the CONF_DONE or INIT_DONE signals have not gone high, the MAX II device will reconfigure the target device.

If you use the optional CLKUSR pin and the nCONFIG is pulled low to restart configuration during device initialization, you must ensure CLKUSR continues toggling during the time nSTATUS is low (maximum of 100 µs).

When the device is in user mode, transitioning the nCONFIG pin low to high initiates a reconfiguration. The nCONFIG pin should be low for at least 2 µs. When nCONFIG is pulled low, the device also pulls nSTATUS and CONF_DONE low and all I/O pins are tri-stated. After nCONFIG returns to a logic high level and nSTATUS is released by the device, reconfiguration begins.

Figure 11–8. Single Device Fast AS Configuration



Notes to Figure 11–8:

(1) Connect the pull-up resistors to V_{CCPGM} at 3.3-V supply.

(2) Stratix III devices use the ASDO-to-ASDI path to control the configuration device.

Upon power-up, the Stratix III devices go through a POR. The POR delay is dependent on the PORSEL pin setting. When PORSEL is driven low, the POR time is approximately 100 ms. If PORSEL is driven high, the POR time is approximately 12 ms. During POR, the device will reset, hold nSTATUS and CONF_DONE low, and tri-state all user I/O pins. After the device successfully exits POR, all user I/O pins continue to be tri-stated. If nIO_pullup is driven low during power-up and configuration, the user I/O pins and dual-purpose I/O pins will have weak pull-up resistors which are on (after POR) before and during configuration. If nIO_pullup is driven high, the weak pull-up resistors are disabled.

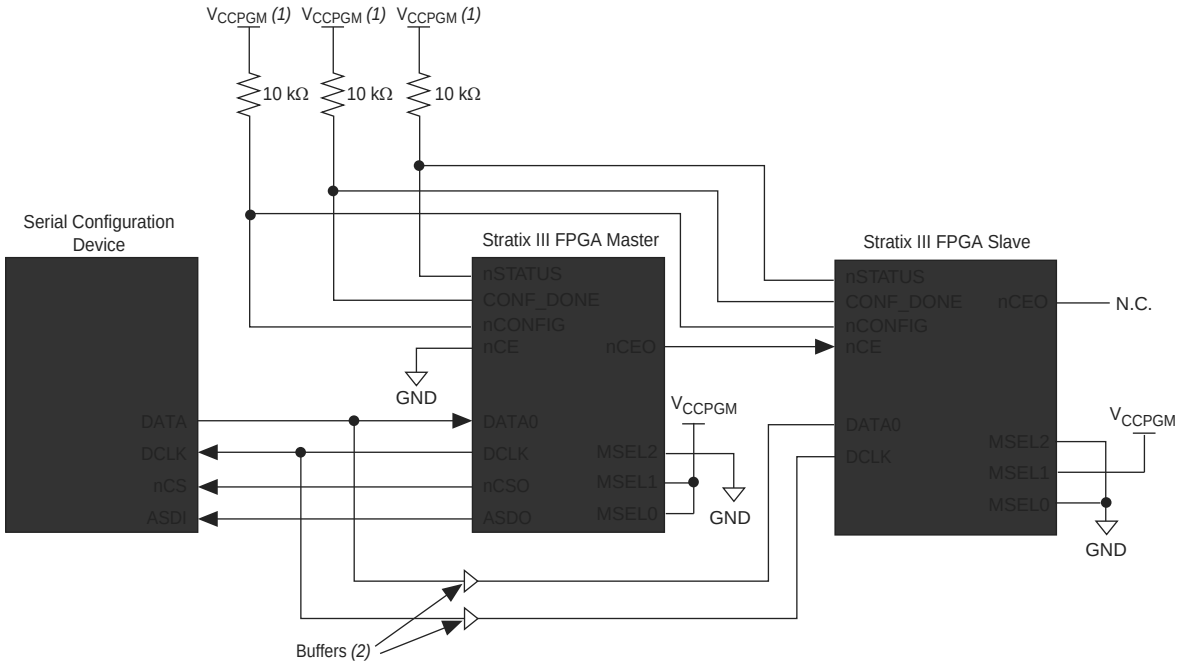
The configuration cycle consists of three stages: reset, configuration, and initialization. While nCONFIG or nSTATUS are low, the device is in reset. After POR, the Stratix III device releases nSTATUS, which is pulled high by an external 10-kΩ pull-up resistor and enters configuration mode.

To begin configuration, power the V_{CC}, V_{CCIO}, V_{CCPGM}, and V_{CCPD} voltages (for the banks where the configuration and JTAG pins reside) to the appropriate voltage levels.

The serial clock (DCLK) generated by the Stratix III device controls the entire configuration cycle and provides the timing for the serial interface. Stratix III devices use an internal oscillator to generate DCLK. Using the MSEL[] pins, you can select to use a 40 MHz oscillator.

In fast AS configuration schemes, Stratix III devices drive out control signals on the falling edge of DCLK. The serial configuration device responds to the instructions by driving out configuration data on the falling edge of DCLK. Then the data is latched into the Stratix III device on the following falling edge of DCLK.

Figure 11–9. Multi-Device Fast AS Configuration



Notes to Figure 11–9:

(1) Connect the pull-up resistors to V_{CCPGM} at 3.3-V supply.

(2) Connect the repeater buffers between the Stratix III master and slave device(s) for DATA[0] and DCLK. This prevents any potential signal integrity and clock skew problems.

As shown in Figure 11–9, the nSTATUS and CONF_DONE pins on all target devices are connected with external pull-up resistors. These pins are open-drain bi-directional pins on the devices. When the first device asserts nCEO (after receiving all of its configuration data), it releases its CONF_DONE pin. The subsequent devices in the chain keep this shared CONF_DONE line low until they have received their configuration data. When all target devices in the chain have received their configuration data and released CONF_DONE, the pull-up resistor drives a high level on this line and all devices simultaneously enter initialization mode.

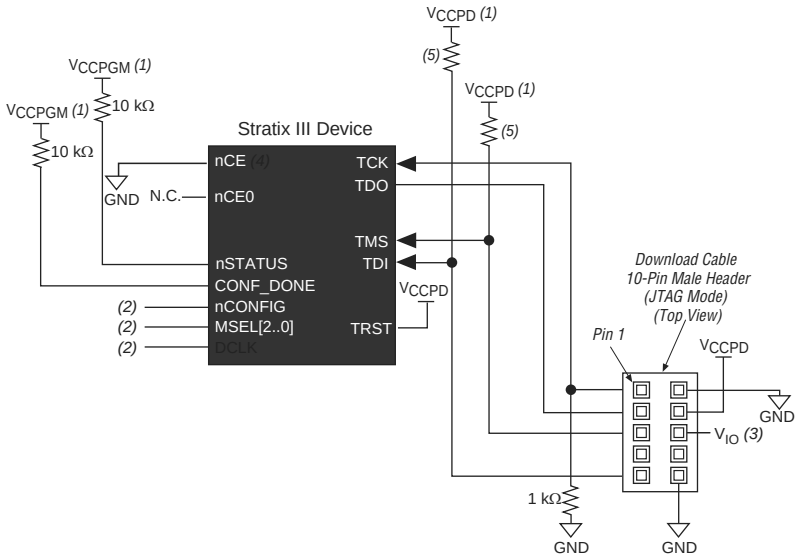
If an error occurs at any point during configuration, the nSTATUS line is driven low by the failing device. If you enable the **Auto-restart configuration after error** option, reconfiguration of the entire chain begins after a reset time-out period (maximum of 100 µs). If the **Auto-restart configuration after error** option is turned off, the external system must monitor nSTATUS for errors and then pulse nCONFIG low to restart configuration. The external system can pulse nCONFIG if it is under system control rather than tied to V_{CCPGM}.

☞ If you have enabled the **Auto-restart configuration after error** option, the nSTATUS pin transitions from high to low and back again to high when a configuration error is detected. This appears as a low pulse at the nSTATUS pin with a minimum pulse width of 10 µs to a maximum pulse width of 500 µs, as defined in the t_{STATUS} specification.

☞ While you can cascade Stratix III devices, you cannot cascade or chain together serial configuration devices.

Figure 11–19 shows JTAG configuration of a single Stratix III device.

Figure 11–19. JTAG Configuration of a Single Device Using a Download Cable



Notes to Figure 11–19:

(1) You should connect the pull-up resistor to the same supply voltage as the USB-Blaster, MasterBlaster (VIO pin), ByteBlaster II, ByteBlasterMV, or EthernetBlaster cables. The voltage supply can be connected to the V_{CCPD} of the device.

(2) You should connect the nCONFIG and MSEL[2..0] pins to support a non-JTAG configuration scheme. If you only use the JTAG configuration, connect nCONFIG to V_{CCPGM}, and MSEL[2..0] to ground. Pull DCLK either high or low, whichever is convenient on your board.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} should match the device's V_{CCPD}. Refer to the *MasterBlaster Serial/USB Communications Cable Data Sheet* for this value. In the USB-Blaster, ByteBlaster II, ByteBlasterMV, and EthernetBlaster, this pin is a no connect.

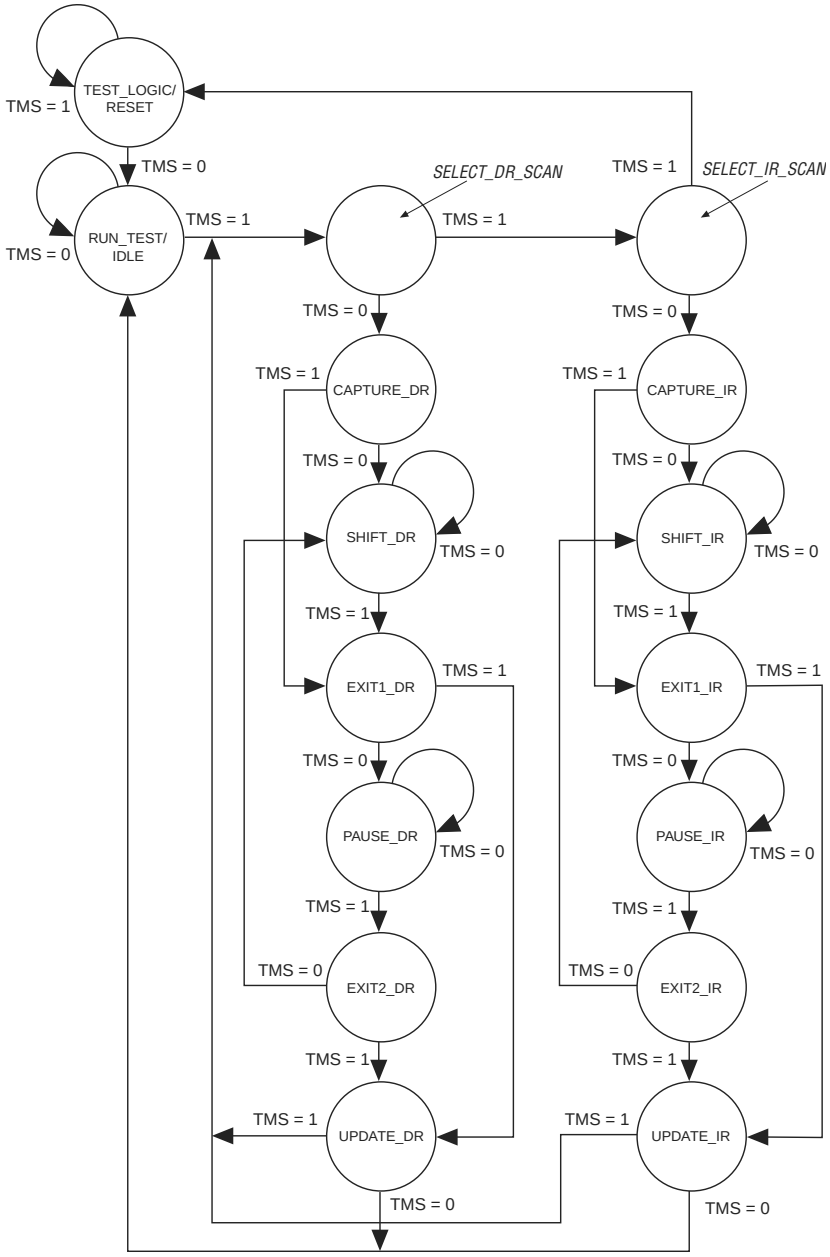
(4) You must connect nCE to GND or drive it low for successful JTAG configuration.

(5) Pull-up resistor values can vary from 1 kΩ to 10 kΩ

To configure a single device in a JTAG chain, the programming software places all other devices in bypass mode. In bypass mode, devices pass programming data from the TDI pin to the TDO pin through a single bypass register without being affected internally. This scheme enables the programming software to program or verify the target device. Configuration data driven into the device appears on the TDO pin one clock cycle later.

The Quartus II software verifies successful JTAG configuration upon completion. At the end of configuration, the software checks the state of CONF_DONE through the JTAG port. When Quartus II generates a JAM file (**.jam)** for a multi-device chain, it contains instructions so that all the devices in the chain will be initialized at the same time. If CONF_DONE is not high, the Quartus II software indicates that configuration has failed. If CONF_DONE is high, the software indicates that configuration was successful. After the configuration bitstream is transmitted serially through the JTAG TDI port, the TCK port is clocked an additional 1,094 cycles to perform device initialization.

Figure 13–5. IEEE Std. 1149.1 TAP Controller State Machine



When the TAP controller is in the TEST_LOGIC/RESET state, the BST circuitry is disabled, the device is in normal operation, and the instruction register is initialized with IDCODE as the initial instruction. At device power-up, the TAP controller starts in this TEST_LOGIC/RESET state. In addition, forcing the TAP controller to the TEST_LOGIC/RESET state is achieved by holding TMS high for five TCK clock cycles, or by holding the TRST pin low. In the TEST_LOGIC/RESET state, the TAP controller remains in this state as long as TMS is held high (while TCK is clocked) or TRST is held low. Figure 13–6 shows the timing requirements for the IEEE Std. 1149.1 signals.