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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	10200
Number of Logic Elements/Cells	255000
Total RAM Bits	16672768
Number of I/O	744
Number of Gates	-
Voltage - Supply	0.86V ~ 1.15V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep3se260f1152c3n

Stratix III devices have up to 112 DSP blocks. The architectural highlights of the Stratix III DSP block are the following:

- High-performance, power optimized, fully pipelined multiplication operations
- Native support for 9-bit, 12-bit, 18-bit, and 36-bit word lengths
- Native support for 18-bit complex multiplications
- Efficient support for floating point arithmetic formats (24-bit for Single Precision and 53-bit for Double Precision)
- Signed and unsigned input support
- Built-in addition, subtraction, and accumulation units to efficiently combine multiplication results
- Cascading 18-bit input bus to form tap-delay lines
- Cascading 44-bit output bus to propagate output results from one block to the next block
- Rich and flexible arithmetic rounding and saturation units
- Efficient barrel shifter support
- Loopback capability to support adaptive filtering

DSP block multipliers can optionally feed an adder/subtractor or accumulator in the block depending on user configuration. This option saves ALM routing resources and increases performance, because all connections and blocks are inside the DSP block. Additionally, the DSP Block input registers can efficiently implement shift registers for FIR filter applications, and the Stratix III DSP blocks support rounding and saturation. The Quartus II software includes megafunctions that control the mode of operation of the DSP blocks based on user parameter settings.

For more information, refer to the *DSP Blocks in Stratix III Devices* chapter.

Clock Networks and PLLs

Stratix III devices provide dedicated Global Clock Networks (GCLKs), Regional Clock Networks (RCLKs), and Periphery Clock Networks (PCLKs). These clocks are organized into a hierarchical clock structure that provides up to 104 unique clock domains (16 GCLK + 88 RCLK) within the Stratix III device and allows for up to 38 (16 GCLK + 22 RCLK) unique GCLK/RCLK clock sources per device quadrant.

Stratix III devices deliver abundant PLL resources with up to 12 PLLs per device and up to 10 outputs per PLL. Every output can be independently programmed, creating a unique, customizable clock frequency. Inherent jitter filtration and fine granularity control over multiply, divide ratios, and dynamic phase-shift reconfiguration provide the high-performance precision required in today's high-speed applications. Stratix III PLLs are feature rich, supporting advanced capabilities such as clock switchover, reconfigurable phase shift, PLL reconfiguration, and reconfigurable bandwidth. PLLs can be used for general-purpose clock management supporting multiplication, phase shifting, and programmable duty cycle. Stratix III PLLs also support external feedback mode, spread-spectrum input clock tracking, and post-scale counter cascading.

4×, 6×, 7×, 8×, and 10× SERDES modes when using the dedicated DPA circuitry. DPA minimizes bit errors, simplifies PCB layout and timing management for high-speed data transfer, and eliminates channel-to-channel and channel-to-clock skew in high-speed data transmission systems. Soft CDR can also be implemented, enabling low-cost 1.6-Gbps clock embedded serial links.

Stratix III devices have the following dedicated circuitry for high-speed differential I/O support:

- Differential I/O buffer
- Transmitter serializer
- Receiver deserializer
- Data realignment
- Dynamic phase aligner (DPA)
- Soft CDR functionality
- Synchronizer (FIFO buffer)
- PLLs

For more information, refer to the *High Speed Differential I/O Interfaces with DPA in Stratix III Devices* chapter.

Hot Socketing and Power-On Reset

Stratix III devices are hot-socketing compliant. Hot socketing is also known as hot plug-in or hot swap, and power sequencing support without the use of any external devices. Robust on-chip hot-socketing and power-sequencing support ensures proper device operation independent of the power-up sequence. You can insert or remove a Stratix III board in a system during system operation without causing undesirable effects to the running system bus or the board that was inserted into the system.

The hot-socketing feature makes it easier to use Stratix III devices on PCBs that also contain a mixture of 3.3-V, 3.0-V, 2.5-V, 1.8-V, 1.5-V, and 1.2-V devices. With the Stratix III hot socketing feature, you do not need to ensure a specific power-up sequence for each device on the board.

For more information, refer to the *Hot Socketing and Power-On Reset in Stratix III Devices* chapter.

Configuration

Stratix III devices are configured using one of the following four configuration schemes:

- Fast passive parallel (FPP)
- Fast active serial (AS)
- Passive serial (PS)
- Joint Test Action Group (JTAG)

All configuration schemes use either an external controller (for example, a MAX® II device or microprocessor), a configuration device, or a download cable.

Signal Integrity

Stratix III devices simplify the challenge of signal integrity through a number of chip, package, and board level enhancements to enable efficient high-speed data transfer into and out of the device. These enhancements include:

- 8:1:1 user I/O/Gnd/V_{CC} ratio to reduce the loop inductance in the package
- Dedicated power supply for each I/O bank, limit of I/Os is 24 to 48 I/Os per bank, to help limit simultaneous switching noise
- Programmable slew-rate support with up to four settings to match desired I/O standard, control noise, and overshoot
- Programmable output-current drive strength support with up to six settings to match desired I/O standard performance
- Programmable output-delay support to control rise/fall times and adjust duty cycle, compensate for skew, and reduce simultaneous switching outputs (SSO) noise
- Dynamic OCT with auto calibration support for series and parallel OCT and differential OCT support for LVDS I/O standard on the left/right banks

For more information about SI support in the Quartus II software, refer to the *Quartus II Handbook*.

For more information about how to use the various configuration, PLL, external memory interfaces, I/O, high-speed differential I/O, power, and JTAG pins, refer to the *Stratix III Device Family Pin Connection Guidelines*.

Reference and Ordering Information

The following section describes Stratix III device software support and ordering information.

Software Support

Stratix III devices are supported by the Altera Quartus II design software, version 6.1 and later, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analyzer, and device configuration.

For more information about the Quartus II software features, refer to the *Quartus II Handbook*.

The Quartus II software supports a variety of operating systems. The specific operating system for the Quartus II software can be obtained from the Quartus II **Readme.txt** file or the *Operating System Support* section of the Altera website. It also supports seamless integration with industry-leading EDA tools through the NativeLink® interface.

☞ Refer to "ALM Interconnects" on page 2–20 for more information on shared arithmetic chain interconnect.

LUT-Register Mode

LUT-Register mode allows third register capability within an ALM. Two internal feedback loops allow combinational `ALUT1` to implement the master latch and combinational `ALUT0` to implement the slave latch needed for the third register. The LUT register shares its clock, clock enable, and asynchronous clear sources with the top dedicated register. Figure 2–15 shows the register constructed using two combinational blocks within the ALM. Figure 2–16 shows the ALM in LUT-Register mode.

Figure 2–15. LUT Register from Two Combinational Blocks

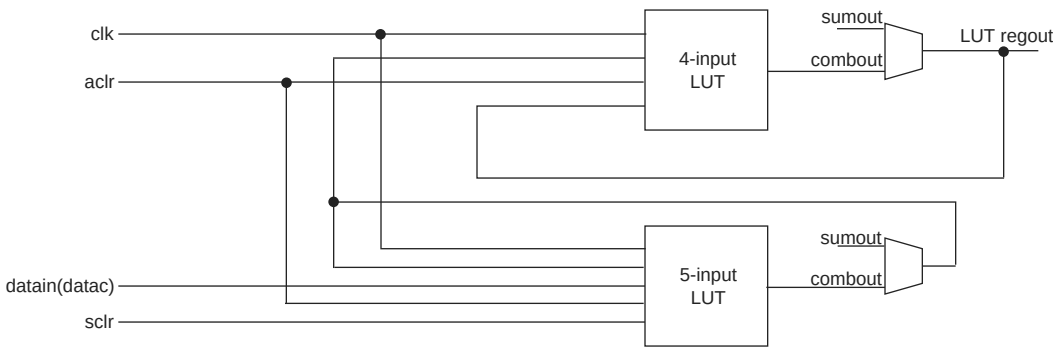
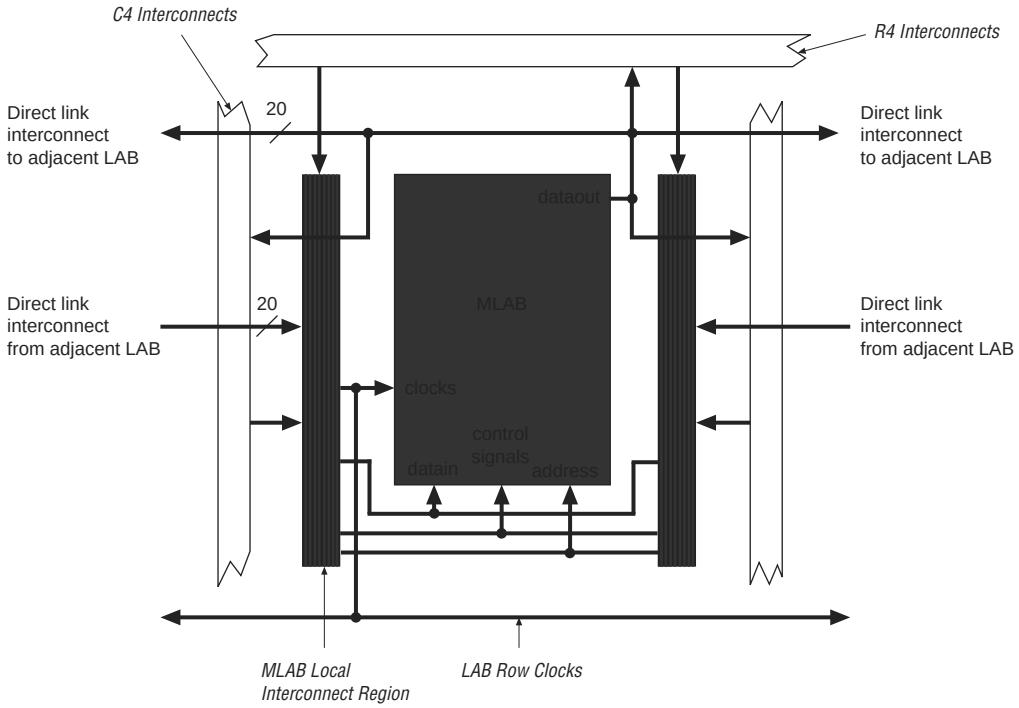
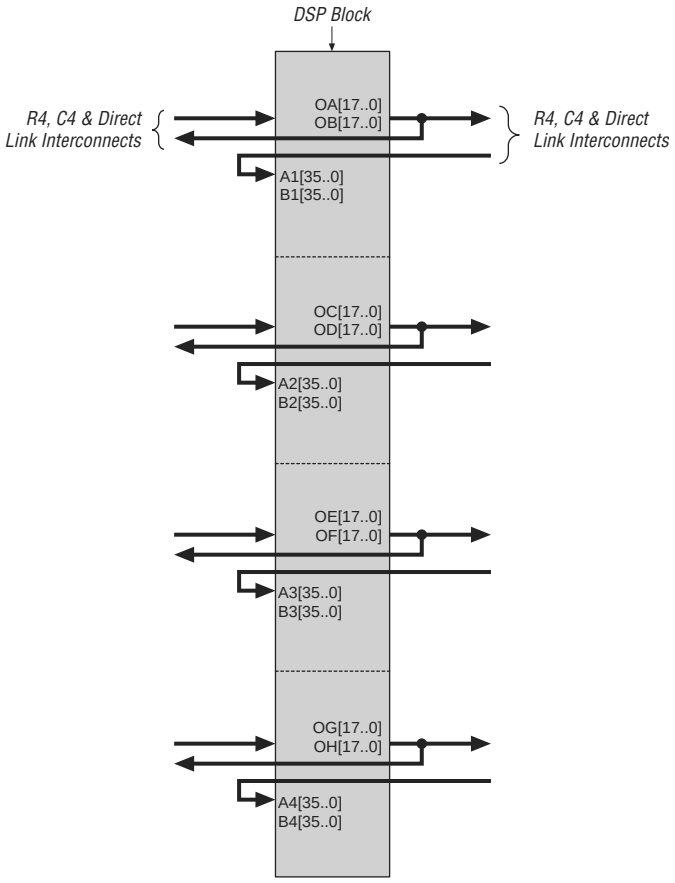


Figure 3–4. MLAB RAM Block LAB Row Interface



The M9K RAM block local interconnect is driven by the R4, C4, and direct link interconnects from adjacent LABs. The M9K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 20 direct link input connections to the M9K RAM Block are possible from the left adjacent LABs and another 20 possible from the right adjacent LAB. M9K RAM block outputs can also connect to left and right LABs through direct link interconnect. Figure 3–5 shows the M9K RAM block to logic array interface.

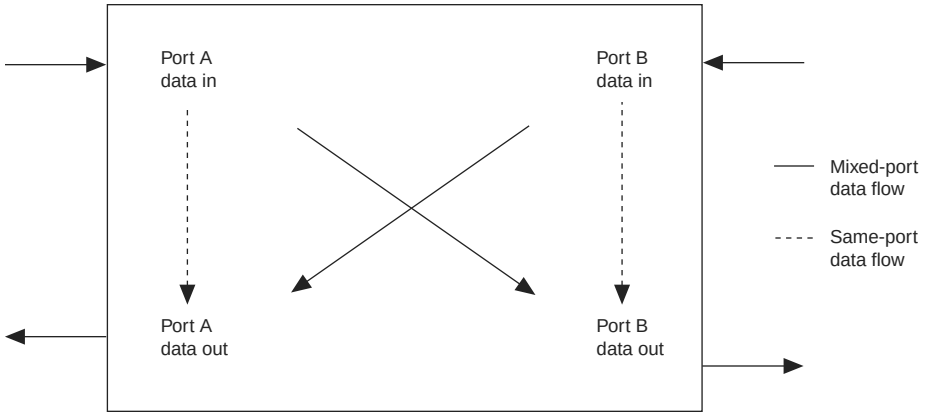
Figure 3–7. High-Level View, DSP Block Interface to Interconnect



Read During Write

You can customize the read-during-write behavior of the Stratix III TriMatrix memory blocks to suit your design needs. Two types of read-during-write operations are available: same port and mixed port. Figure 4–18 shows the difference between the two types.

Figure 4–18. Stratix III Read-During-Write Data Flow



Same-Port Read-During-Write Mode

This mode applies to either a single-port RAM or the same port of a true dual-port RAM. In same-port read-during-write mode, three output choices are available: new data mode (or flow-through), old data mode, or don't care mode. In new data mode, the new data is available on the rising edge of the same clock cycle on which it was written. In old data mode, the RAM outputs reflect the old data at that address before the write operation proceeds. In don't care mode, the RAM outputs don't care values for a read-during-write operation.

If you are not using the new data mode or old data mode, you should select the don't care mode. Using the don't care mode increases the flexibility in the type of memory block used, provided you do not assign block type when instantiating a memory block. You may also get potential performance gain by selecting the don't care mode.

A single DSP block can implement up to two independent 44-bit accumulators.

The dynamic `accum_sload` control signal is used to clear the accumulation. A `logic 1` value on the `accum_sload` signal synchronously loads the accumulator with the multiplier result only, while a `logic 0` enables accumulation by adding or subtracting the output of the DSP block (accumulator feedback) to the output of the multiplier and first-stage adder.

☞ The control signal for the accumulator and subtractor is static and therefore has to be configured at compile time.

This mode supports the round and saturation logic unit as it is configured as an 18-bit multiplier accumulator. You can use the pipeline registers and output registers within the DSP block to increase the performance of the DSP block.

Shift Modes

Stratix III devices support the following shift modes for 32-bit input only:

- Arithmetic shift left, `ASL[N]`
- Arithmetic shift right, `ASR[32-N]`
- Logical shift left, `LSL[N]`
- Logical shift right, `LSR[32-N]`
- 32-bit rotator or Barrel shifter, `ROT[N]`

☞ You can switch the shift mode between these modes using the dynamic rotate and shift control signals.

The shift mode in a Stratix III device can be easily used by the soft embedded processor such as Nios® II to perform the dynamic shift and rotate operation. Figure 5–20 shows the shift mode configuration.

The shift mode makes use of the available multipliers to logically or arithmetically shift left, right, or rotate the desired 32-bit data. The DSP block is configured like the independent 36-bit multiplier mode to perform the shift mode operations.

The arithmetic shift right requires signed input vector. During arithmetic shift right, the sign is extended to fill the MSB of the 32-bit vector. The logical shift right uses unsigned input vector. During logical shift right, zeros are padded in the most significant bits shifting the 32-bit vector to the right. The barrel shifter uses unsigned input vector and implements a rotation function on a 32-bit word length.

Two control signals `rotate` and `shift_right` together with the `signa` and `signb` signals, determining the shifting operation. Examples of shift operations are listed in Table 5–5 on page 5–31.

When you use **both** the input cascade and chainout features, the DSP block uses an 18-bit delay register in the boundary of each half-DSP block or from block-to-block to synchronize the input scan chain data with the chainout data. The top half computes the sum of product and chains the output to the next block after the output register. The output register uses the delay register to delay the cascade input by one clock cycle to compensate the latency for the bottom half.

For applications in which the system clock is slower than the speed of the DSP block, the multipliers can be time-multiplexed to improve efficiency. This makes multi-channel and semi-parallel FIR structures possible. The structure to achieve this is similar to Figure 5–22 and Figure 5–23. The main difference is that the input cascade chain is no longer used and each half-DSP block is used in Four-Multiplier Mode with independent inputs. Figure 5–24 shows an example for chained cascaded summation.

In most cases, only the final stage FIR tap with the rounding and saturation unit is deployed.

Regional Clock Networks

The regional clock (RCLK) networks only pertain to the quadrant they drive into. The RCLK networks provide the lowest clock delay and skew for logic contained within a single device quadrant. Stratix III device I/O elements and internal logic within a given quadrant can also drive RCLKs to create internally generated regional clocks and other high fan-out control signals; for example, synchronous or asynchronous clears and clock enables. Figure 6–2 to Figure 6–4 show CLK pins and PLLs that can drive RCLK networks in Stratix III devices. The EP3SL50, EP3SL70, EP3SL110, EP3SL150, EP3SE50, EP3SE80, and EP3SE110 devices contain 64 RCLKs; the EP3SL200, EP3SE260, and EP3SL340 devices contain 88 RCLKs.

Figure 6–2. Regional Clock Networks (EP3SL50, EP3SL70, and EP3SE50 Devices)

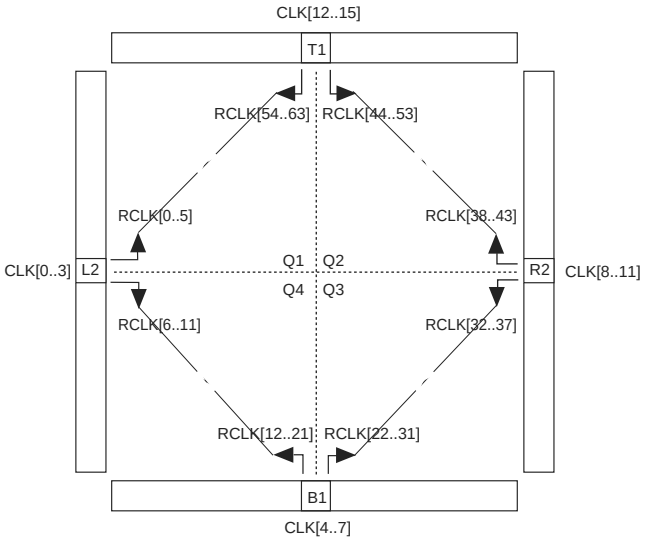


Figure 6–3. Regional Clock Networks (EP3SL110, EP3SL150, EP3SE80, and EP3SE110 Devices)

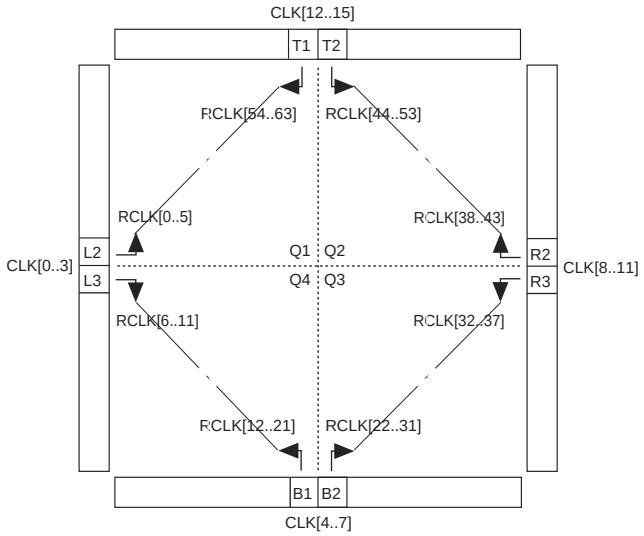


Table 6–16. Top/Bottom PLL Reprogramming Bits (Part 2 of 2)

Block Name	Number of Bits		Total
	Counter	Other *(1)*	
Total number of bits	—	—	234

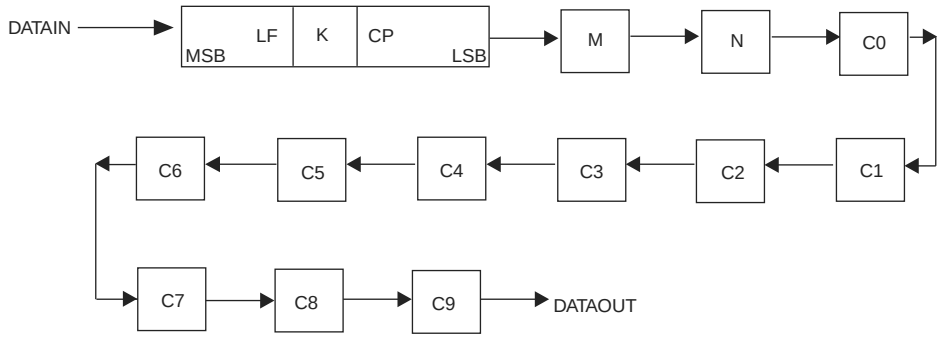
Notes to Table 6–16:

(1) Includes two control bits, `rbypass`, for bypassing the counter, and `rselodd`, to select the output clock duty cycle.
(2) LSB bit for `C9` low-count value is the first bit shifted into the scan chain for Top/Bottom PLLs.
(3) LSB bit for `C6` low-count value is the first bit shifted into the scan chain for Left/Right PLLs.
(4) MSB bit for loop filter is the last bit shifted into the scan chain.

Table 6–16 lists the scan chain order of PLL components for Top/Bottom PLLs which have 10 post-scale counters. The order of bits is the same for the Left/Right PLLs, but the reconfiguration bits start with the `C6` post-scale counter.

Figure 6–42 shows the scan-chain order of PLL components for the Top/Bottom PLLs.

Figure 6–42. Scan-Chain Order of PLL Components for Top/Bottom PLLs *(Note 1)*

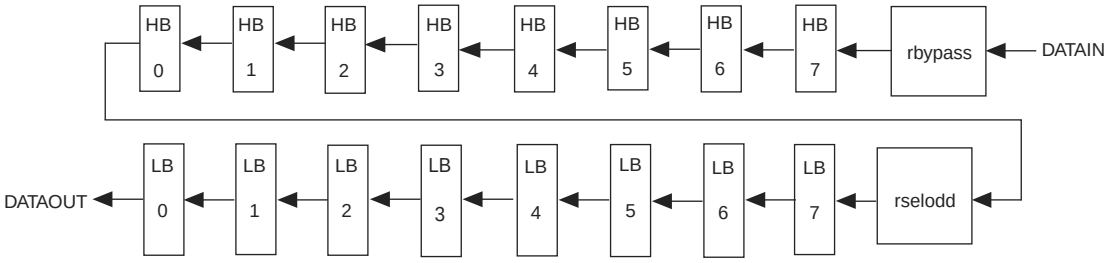


Note to Figure 6–42:

(1) Left/Right PLLs have the same scan-chain order. The post-scale counters end at `C6`.

Figure 6–43 shows the scan-chain bit-order sequence for post-scale counters in all Stratix III PLLs.

Figure 6–43. Scan-Chain Bit-Order Sequence for Post-Scale Counters in Stratix III PLLs



Stratix III I/O Standards Support

Stratix III devices support a wide range of industry I/O standards. Table 7–1 lists the I/O standards supported by Stratix III devices as well as typical applications. Stratix III devices support V_{CCIO} voltage levels of 3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V.

Table 7–1. I/O Standard Applications for Stratix III Devices (Part 1 of 2)

I/O Standard	Typical Application
3.3-V LVTTL/LVCMOS	General purpose
3.0-V LVTTL/LVCMOS	General purpose
2.5-V LVTTL/LVCMOS	General purpose
1.8-V LVTTL/LVCMOS	General purpose
1.5-V LVTTL/LVCMOS	General purpose
1.2-V LVTTL/LVCMOS	General purpose
3.0-V PCI	PC and embedded system
3.0-V PCI-X	PC and embedded system
SSTL-2 Class I	DDR SDRAM
SSTL-2 Class II	DDR SDRAM
SSTL-18 Class I	DDR2 SDRAM
SSTL-18 Class II	DDR2 SDRAM
SSTL-15 Class I	DDR3 SDRAM
SSTL-15 Class II	DDR3 SDRAM
HSTL-18 Class I	QDR II/RLDRAM II
HSTL-18 Class II	QDR II/RLDRAM II
HSTL-15 Class I	QDR II/QDR II+/RLDRAM II
HSTL-15 Class II	QDR II/QDR II+/RLDRAM II
HSTL-12 Class I	General purpose
HSTL-12 Class II	General purpose
Differential SSTL-2 Class I	DDR SDRAM
Differential SSTL-2 Class II	DDR SDRAM
Differential SSTL-18 Class I	DDR2 SDRAM
Differential SSTL-18 Class II	DDR2 SDRAM
Differential SSTL-15 Class I	DDR3 SDRAM
Differential SSTL-15 Class II	DDR3 SDRAM
Differential HSTL-18 Class I	Clock interfaces
Differential HSTL-18 Class II	Clock interfaces
Differential HSTL-15 Class I	Clock interfaces
Differential HSTL-15 Class II	Clock interfaces
Differential HSTL-12 Class I	Clock interfaces
Differential HSTL-12 Class II	Clock interfaces
LVDS	High-speed communications
RSDS	Flat panel display

Table 7–4. Memory Interface Standards Supported (Part 2 of 2)

Memory Interface Standard	I/O Standard
DDR3 SDRAM	SSTL-15
RLDRAM II	HSTL-18
QDR II SRAM	HSTL-18
QDR II+ SRAM	HSTL-15

For more information about external memory interfaces, refer to the *External Memory Interfaces in Stratix III Devices* chapter.

High-Speed Differential I/O with DPA Support

Stratix III devices contain dedicated circuitry for supporting differential standards at speeds up to 1.6 Gbps. The high-speed differential I/O circuitry supports the following high speed I/O interconnect standards and applications: Utopia IV, SPI-4.2, SFI-4, 10 Gigabit Ethernet XSBI, RapidIOTM, and NPSI. Stratix III devices support ×2, ×4, ×6, ×7, ×8, and ×10 SERDES modes for high-speed differential I/O interfaces and ×4, ×6, ×7, ×8, and ×10 SERDES modes with dedicated DPA circuitry. DPA minimizes bit errors, simplifies PCB layout and timing management for high-speed data transfer, and eliminates channel-to-channel and channel-to-clock skew in high-speed data transmission systems.

×2 mode is supported by the DDR registers and is not included in SERDES. For Stratix III devices, SERDES can be bypassed in the Quartus II MegaWizard™ Plug-In Manager for the ALTLVDS megafunction to support DDR (×2) operation.

Stratix III devices have the following dedicated circuitry for high-speed differential I/O support:

- Differential I/O buffer
- Transmitter serializer
- Receiver deserializer
- Data realignment
- DPA
- Synchronizer (FIFO buffer)
- Phase-locked loops (PLLs)

For more information about DPA support, refer to the *High-Speed Differential I/O Interfaces with DPA in Stratix III Devices* chapter.

Programmable Current Strength

The output buffer for each Stratix III device I/O pin has a programmable current-strength control for certain I/O standards. You can use programmable current strength to mitigate the effects of high signal attenuation due to a long transmission line or a legacy backplane. The LVTTL, LVCMOS, SSTL, and HSTL standards have several levels of current strength that you can control. Table 7–5 lists information about programmable current strength.

I/O Termination

I/O termination requirements for single-ended and differential I/O standards are discussed in this section.

Single-Ended I/O Standards

Although single-ended, non-voltage-referenced I/O standards do not require termination, impedance matching may be necessary to reduce reflections and improve signal integrity.

Voltage-referenced I/O standards require both an input reference voltage, $V_{REF,}$ and a termination voltage, V_{TT}. The reference voltage of the receiving device tracks the termination voltage of the transmitting device. Each voltage-referenced I/O standard requires a unique termination setup. For example, a proper resistive signal termination scheme is critical in SSTL2 standards to produce a reliable DDR memory system with superior noise margin.

Stratix III OCT R_S and OCT R_T provide the convenience of no external components. Alternatively, you can use external pull-up resistors to terminate the voltage-referenced I/O standards, such as SSTL and HSTL.

Differential I/O Standards

Differential I/O standards typically require a termination resistor between the two signals at the receiver. The termination resistor must match the differential load impedance of the signal line. Stratix III devices provide an optional differential on-chip resistor when using LVDS.

For PCB layout guidelines, refer to *AN 224: High-Speed Board Layout Guidelines* and *AN 315: Guidelines for Designing High-Speed FPGA PCBs*.

I/O Banks Restrictions

Each I/O bank can simultaneously support multiple I/O standards. The following sections provide guidelines for mixing non-voltage-referenced and voltage-referenced I/O standards in Stratix III devices.

Non-Voltage-Referenced Standards

Each Stratix III device I/O bank has its own V_{CCIO} pins and supports only one V_{CCIO}, either 1.2, 1.5, 1.8, 2.5, 3.0, or 3.3 V. An I/O bank can simultaneously support any number of input signals with different I/O standard assignments, as listed in Table 7–2.

For output signals, a single I/O bank supports non-voltage-referenced output signals that are driving at the same voltage as V_{CCIO}. Since an I/O bank can only have one V_{CCIO} value, it can only drive out that one value for non-voltage-referenced signals. For example, an I/O bank with a 2.5-V V_{CCIO} setting can support 2.5-V standard inputs and outputs and 3-V LVCMOS inputs (not output or bi-directional pins).

The user watchdog timer is a counter that counts down from the initial value loaded into the remote system upgrade control register by the factory configuration. The counter is 29-bits wide and has a maximum count value of 2^{29}. When specifying the user watchdog timer value, specify only the most significant 12 bits. The granularity of the timer setting is 2^{15} cycles. The cycle time is based on the frequency of the 10-MHz internal oscillator. Table 12–6 specifies the operating range of the 10-MHz internal oscillator.

Table 12–6. 10-MHz Internal Oscillator Specifications

Minimum	Typical	Maximum	Unit
5	6.5	10	MHz

The user watchdog timer begins counting once the application configuration enters device user mode. This timer must be periodically reloaded or reset by the application configuration before the timer expires by asserting `RU_nRSTIMER`. If the application configuration does not reload the user watchdog timer before the count expires, a time-out signal is generated by the remote system upgrade dedicated circuitry. The time-out signal tells the remote system upgrade circuitry to set the user watchdog timer status bit (`Wd`) in the remote system upgrade status register and reconfigures the device by loading the factory configuration.

To allow remote system upgrade dedicated circuitry to reset the watchdog timer, you must assert the `RU_nRSTIMER` signal active for a minimum of 250 ns. This is equivalent to strobing the `reset_timer` input of the ALTREMOTE_UPDATE megafunction high for a minimum of 250 ns.

The user watchdog timer is disabled during the configuration cycle of the device. Errors during configuration are detected by the CRC engine. Also, the timer is disabled for factory configurations. Functional errors should not exist in the factory configuration since it is stored and validated during production and is never updated remotely.

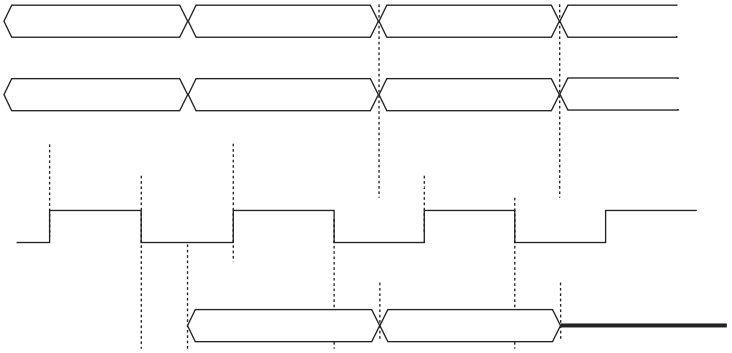
The user watchdog timer is disabled in factory configurations and during the configuration cycle of the application configuration. It is enabled after the application configuration enters user mode. If you do not wish to use the user watchdog timer feature during application configuration user mode operation, turn this feature off by setting `Wd_en` bit to `1'b0` in the update register during factory configuration user mode operation.

Quartus II Software Support

The Quartus II software provides the flexibility to include the remote system upgrade interface between the Stratix III device logic array and the dedicated circuitry, generate configuration files for productions, and remote programming of the system configuration memory.

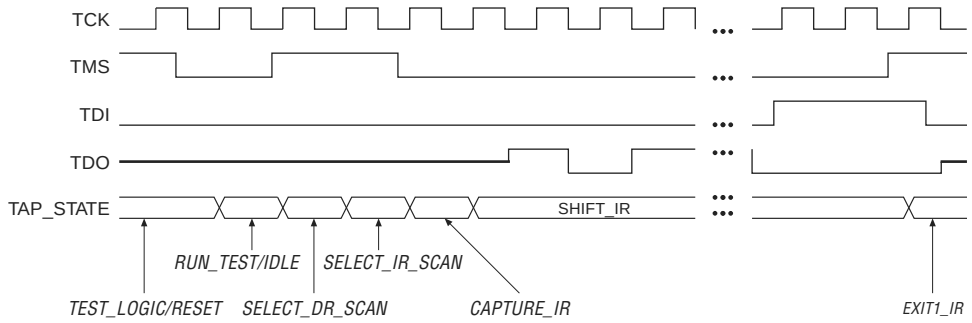
The implementation of the **ALTREMOTE_UPDATE megafunction** option in the Quartus II software is for the interface between the remote system upgrade circuitry and the device logic array interface. Using the megafunction block instead of creating your own logic saves design time and offers more efficient logic synthesis and device implementation.

Figure 13–6. IEEE Std. 1149.1 Timing Waveforms



To start IEEE Std. 1149.1 operation, select an instruction mode by advancing the TAP controller to the shift instruction register (SHIFT_IR) state and shift in the appropriate instruction code on the TDI pin. The waveform diagram in Figure 13–7 shows the entry of the instruction code into the instruction register. It also shows the values of TCK, TMS, TDI, TDO, and the states of the TAP controller. From the RESET state, TMS is clocked with the pattern 01100 to advance the TAP controller to SHIFT_IR.

Figure 13–7. Selecting the Instruction Mode



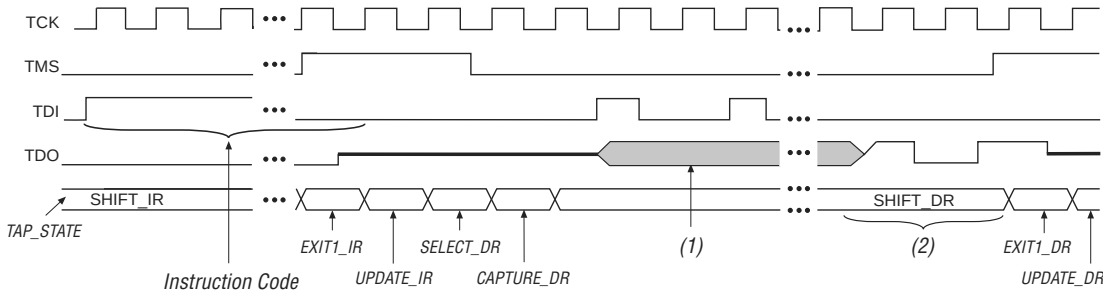
The TDO pin is tri-stated in all states except in the SHIFT_IR and SHIFT_DR states. The TDO pin is activated at the first falling edge of TCK after entering either of the shift states and is tri-stated at the first falling edge of TCK after leaving either of the shift states.

When the SHIFT_IR state is activated, TDO is no longer tri-stated, and the initial state of the instruction register is shifted out on the falling edge of TCK. TDO continues to shift out the contents of the instruction register as long as the SHIFT_IR state is active. The TAP controller remains in the SHIFT_IR state as long as TMS remains low.

EXTEST mode selects data differently than SAMPLE/PRELOAD mode. EXTEST chooses data from the update registers as the source of the output and output-enable signals. After the EXTEST instruction code is entered, the multiplexers select the update register data. Therefore, data stored in these registers from a previous EXTEST or SAMPLE/PRELOAD test cycle can be forced onto the pin signals. In the capture phase, the results of this test data are stored in the capture registers and then shifted out of TDO during the shift phase. You can then store new test data in the update registers during the update phase.

The EXTEST waveform diagram in Figure 13–11 resembles the SAMPLE/PRELOAD waveform diagram, except for the instruction code. The data shifted out of TDO consists of the data that was present in the capture registers after the capture phase. New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register.

Figure 13–11. EXTEST Shift Data Register Waveforms



Note to Figure 13–11:

(1) Data stored in the boundary-scan register is shifted out of TDO.

(2) After boundary-scan register data has been shifted out, data entered into TDI will shift out of TDO.

16. Programmable Power and Temperature-Sensing Diodes in Stratix III Devices

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Introduction

The total power of an FPGA includes static power and dynamic power. Static power is the power consumed by the FPGA when it is programmed but no clocks are operating. Dynamic power is comprised of switching power when the device is configured and running. Dynamic power is calculated with the Equation 16–1:

Equation 16–1. Dynamic Power Equation

$$P = \frac{1}{2} CV^2 \times \text{frequency} \times \text{toggle rate}$$

Equation 16–1 shows that the frequency and toggle rate are design-dependent. However, voltage can be varied to lower dynamic power consumption by the square value of the voltage difference. Stratix® III devices minimize static and dynamic power with advanced process optimizations, selectable core voltage, and programmable power technology. These technologies enable Stratix III designs to optimally meet design-specific performance requirements with the lowest possible power.

The Quartus® II software optimizes all designs with Stratix III power technology to ensure performance is met at the lowest power consumption. This automatic process allows you to concentrate on the functionality of your design, instead of the power consumption of the design.

Power consumption also affects thermal management. Stratix III offers a temperature sensing diode (TSD), which you can use with external circuitry to monitor the device junction temperature for activities such as controlling air flow to the FPGA.

Stratix III Power Technology

The following section provides details about Stratix III selectable core voltage and programmable power technology.

Selectable Core Voltage

Altera offers a series of low-voltage Stratix products that have the ability to power the core logic of the device with either a 0.9-V or 1.1-V power supply. This power supply, called V_{CCL}, powers the logic array block (LAB), memory logic array block (MLAB), digital signal processing (DSP) blocks, TriMatrix™ memory blocks, clock networks, and routing lines. The periphery, consisting of the I/O registers and their routing connections are powered by V_{CC} with a 1.1-V power supply. You can use the same 1.1-V power supply if you want both V_{CC} and V_{CCL} to be 1.1 V.