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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	10200
Number of Logic Elements/Cells	255000
Total RAM Bits	16672768
Number of I/O	976
Number of Gates	-
Voltage - Supply	0.86V ~ 1.15V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep3se260f1517c3n

Table 1–1 lists the Stratix III FPGA family features.

Table 1–1. FPGA Family Features for Stratix III Devices

	Device/ Feature	ALMs	LEs	M9K Blocks	M144K Blocks	MLAB Blocks	Total Embedded RAM Kbits	MLAB RAM Kbits *(1)*	Total RAM Kbits*(2)*	18×18-bit Multipliers (FIR Mode)	PLLs *(3)*
Stratix III Logic Family	EP3SL50	19K	47.5K	108	6	950	1,836	297	2,133	216	4
	EP3SL70	27K	67.5K	150	6	1,350	2,214	422	2,636	288	4
	EP3SL110	43K	107.5K	275	12	2,150	4,203	672	4,875	288	8
	EP3SL150	57K	142.5K	355	16	2,850	5,499	891	6,390	384	8
	EP3SL200	80K	200K	468	36	4,000	9,396	1,250	10,646	576	12
	EP3SL340	135K	337.5K	1,040	48	6,750	16,272	2,109	18,381	576	12
Stratix III Enhanced Family	EP3SE50	19K	47.5K	400	12	950	5,328	297	5,625	384	4
	EP3SE80	32K	80K	495	12	1,600	6,183	500	6,683	672	8
	EP3SE110	43K	107.5K	639	16	2,150	8,055	672	8,727	896	8
	EP3SE260	102K	255K	864	48	5,100	14,688	1,594	16,282	768	12

Notes to Table 1–1:

(1) MLAB ROM mode supports twice the number of MLAB RAM Kbits.

(2) For total ROM Kbits, use this equation to calculate:
Total ROM Kbits = Total Embedded RAM Kbits + [(# of MLAB blocks × 640)/1024]

(3) The availability of the PLLs shown in this column is based on the device with the largest package. Refer to the *Clock Networks and PLLs in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook* for the availability of the PLLs for each device.

The Stratix III logic family (*L*) offers balanced logic, memory, and multipliers to address a wide range of applications, while the enhanced family (*E*) offers more memory and multipliers per logic and is ideal for wireless, medical imaging, and military applications.

Stratix III devices are available in space-saving FineLine BGA (FBGA) packages (refer to Table 1–2 and Table 1–3).

Figure 2–5. High-Level Block Diagram of the Stratix III ALM

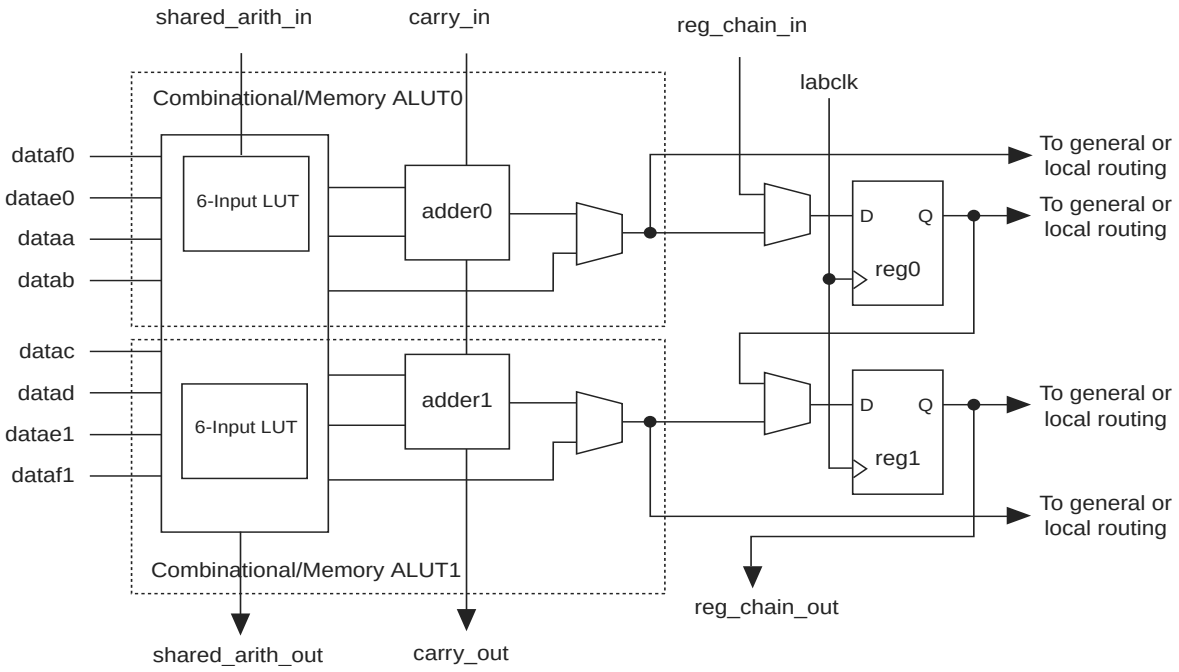
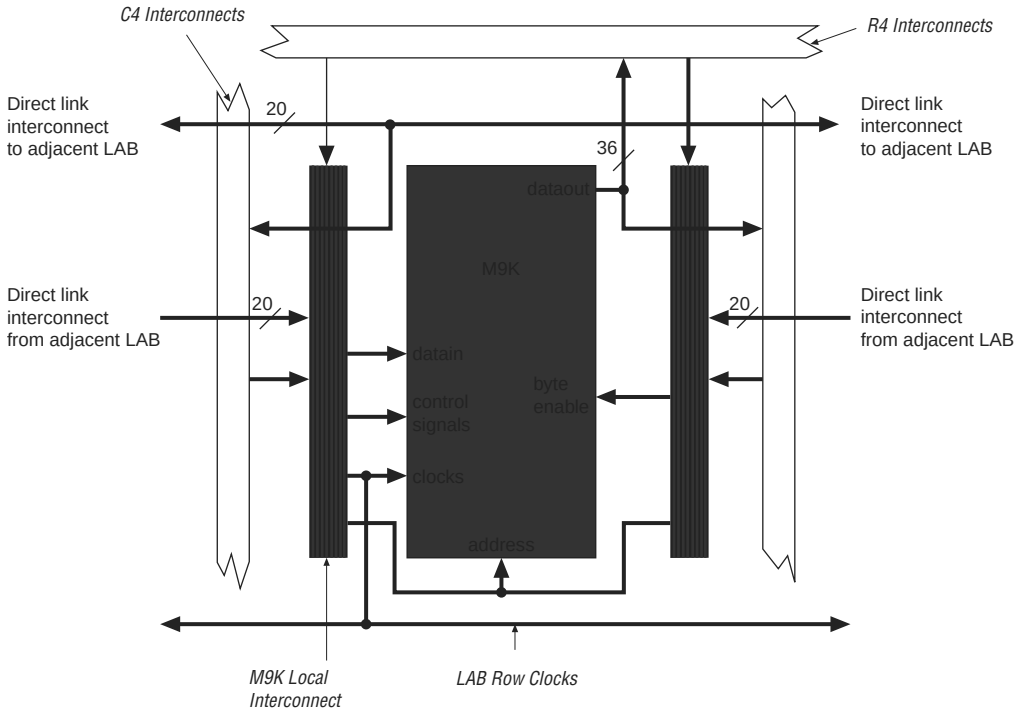


Figure 3–5. M9K RAM Block LAB Row Interface



The M144K blocks use eight interfaces in the same device column. The M144K block local interconnects are driven by R4, C4, and direct link interconnects from adjacent LABs on either the right or left side of the MRAM block. Up to 20 direct link input connections to the M144K block are possible from the left adjacent LABs and another 20 possible from the right adjacent LAB. M144K block outputs can also connect to the LABs on the block's left and right sides through direct link interconnect. Figure 3–6 shows the interface between the M144K RAM block and the logic array.

18 × 18 Complex Multiply

You can configure the DSP block when used in Two-Multiplier Adder mode to implement complex multipliers using the two-multiplier adder mode. A single half DSP block can implement one 18-bit complex multiplier.

A complex multiplication can be written as shown in Equation 5–4.

Equation 5–4. Complex Multiplication Equation

$$(a + jb) \times (c + jd) = ((a \times c) - (b \times d)) + j((a \times d) + (b \times c))$$

To implement this complex multiplication within the DSP block, the real part ((a × c) – (b × d)) is implemented using two multipliers feeding one subtractor block while the imaginary part ((a × d) + (b × c)) is implemented using another two multipliers feeding an adder block. Figure 5–16 shows an 18-bit complex multiplication. This mode automatically assumes all inputs are using signed numbers.

Figure 5–16. Complex Multiplier Using Two-Multiplier Adder Mode

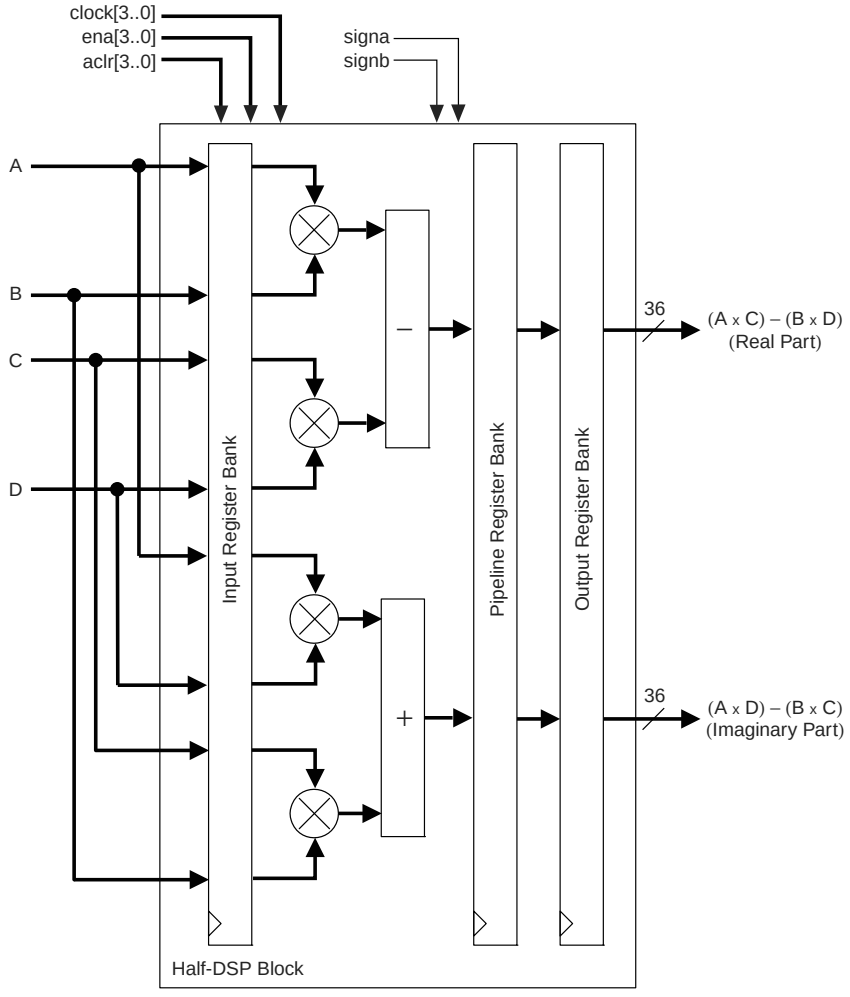


Figure 6–8. Periphery Clock Networks (EP3SE260 Devices)

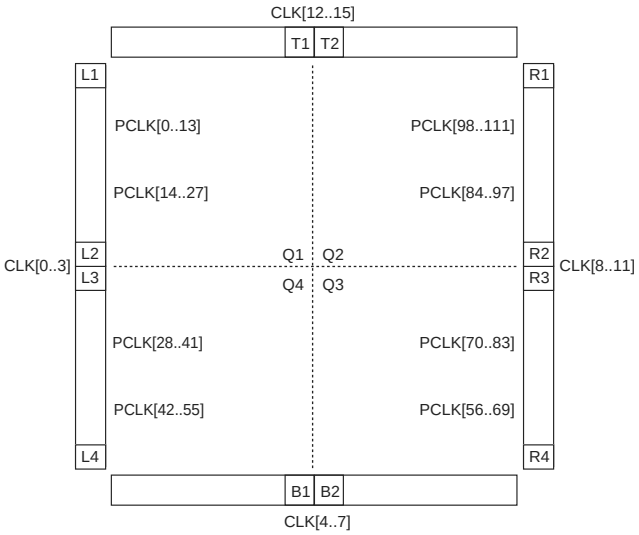
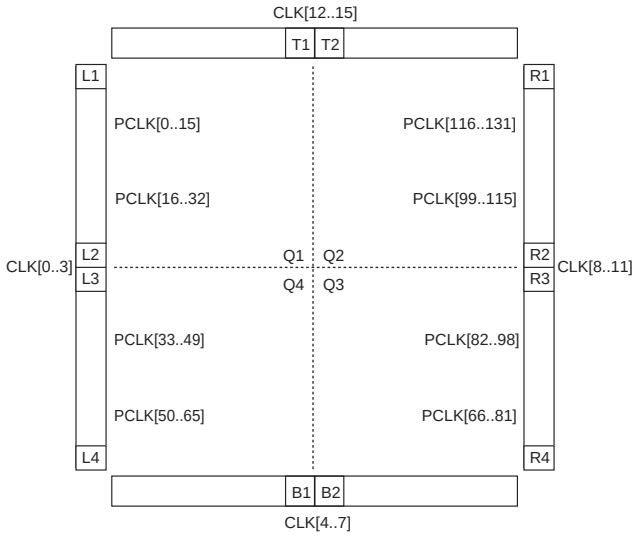


Figure 6–9. Periphery Clock Networks (EP3SL340 Devices)



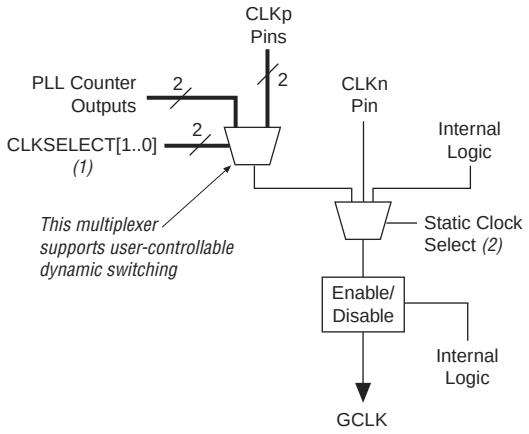
Clocking Regions

Stratix III devices provide up to 104 distinct clock domains (16 GCLKs + 88 RCLKs) in the entire device. You can utilize these clock resources to form the following three different types of clock regions:

- Entire device clock region
- Regional clock region
- Dual-regional clock region

Figure 6–13 and Figure 6–14 show the global clock and regional clock select blocks, respectively.

Figure 6–13. Stratix III Global Clock Control Block

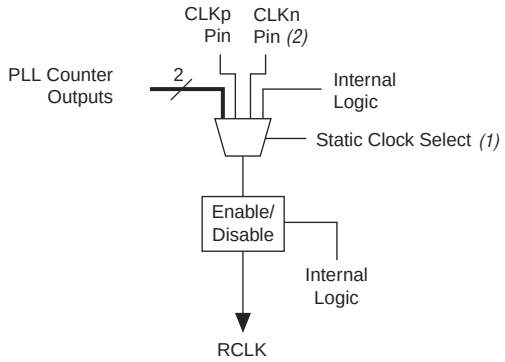


Notes to Figure 6–13:

(1) These clock select signals can only be dynamically controlled through internal logic when the device is operating in user mode.

(2) These clock select signals can only be set through a configuration file (**.sof** or **.pof**) and cannot be dynamically controlled during user mode operation.

Figure 6–14. Regional Clock Control Block



Notes to Figure 6–14:

(1) This clock select signal can only be statically controlled through a configuration file (**.sof** or **.pof**) and cannot be dynamically controlled during user mode operation.

(2) CLKn pin is not a dedicated clock input when it is use as a single-ended PLL clock input and it is not fully compensated.

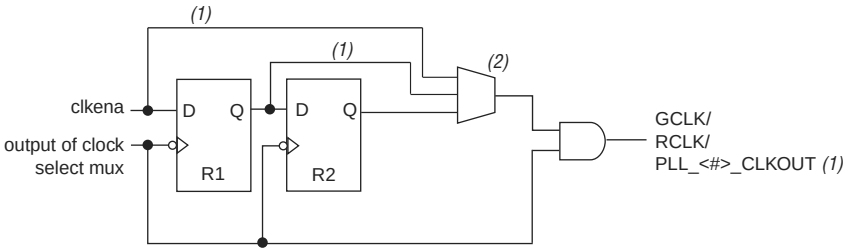
The clock source selection for the regional clock select block can only be controlled statically using configuration bit settings in the configuration file (**.sof** or **.pof**) generated by the Quartus II software.

The Stratix III clock networks can be powered down by both static and dynamic approaches. When a clock net is powered down, all the logic fed by the clock net is in an off-state, thereby reducing the overall power consumption of the device. The unused global and regional clock networks are automatically powered down through configuration bit settings in the configuration file (**.sof** or **.pof**) generated by the

Clock Enable Signals

Figure 6–16 shows how the clock enable/disable circuit of the clock control block is implemented in Stratix III devices.

Figure 6–16. clkena Implementation



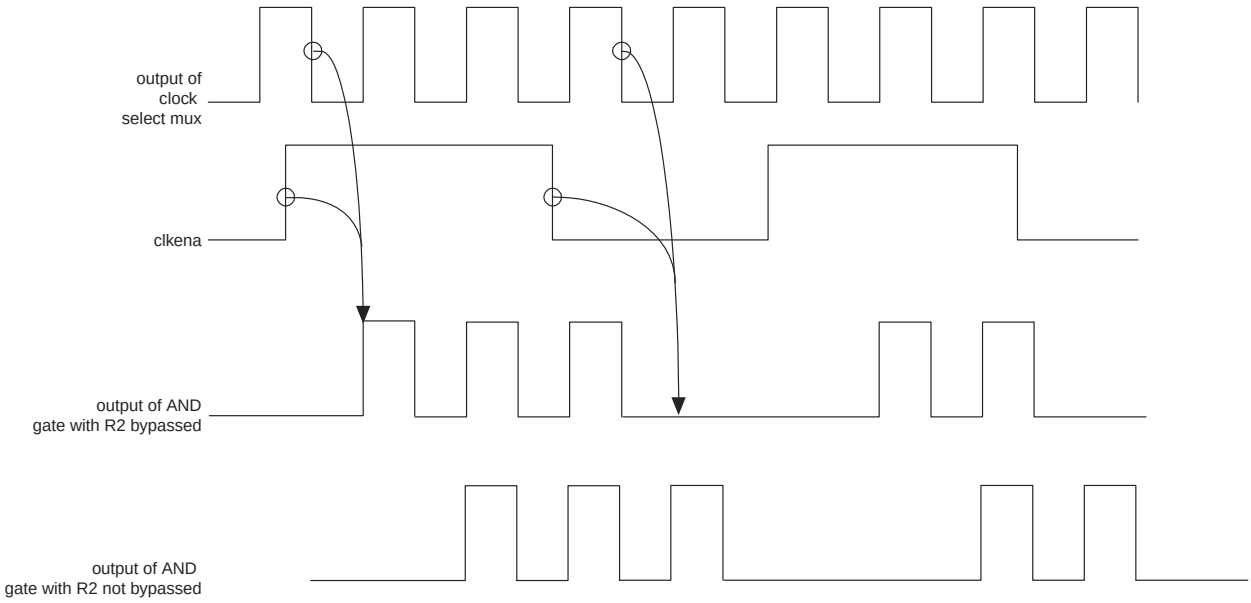
Notes to Figure 6–16:

(1) The R1 and R2 bypass paths are not available for PLL external clock outputs.
(2) The select line is statically controlled by a bit setting in the configuration file (**.sof** or **.pof**).

In Stratix III devices, the `clkena` signals are supported at the clock network level instead of at the PLL output counter level. This allows you to gate off the clock even when a PLL is not being used. You can also use the `clkena` signals to control the dedicated external clocks from the PLLs. Figure 6–17 shows the waveform example for a clock output enable. `clkena` is synchronous to the falling edge of the clock output.

Stratix III devices also have an additional metastability register that aids in asynchronous enable/disable of the GCLK and RCLK networks. This register can be optionally bypassed in the Quartus II software.

Figure 6–17. clkena Signals

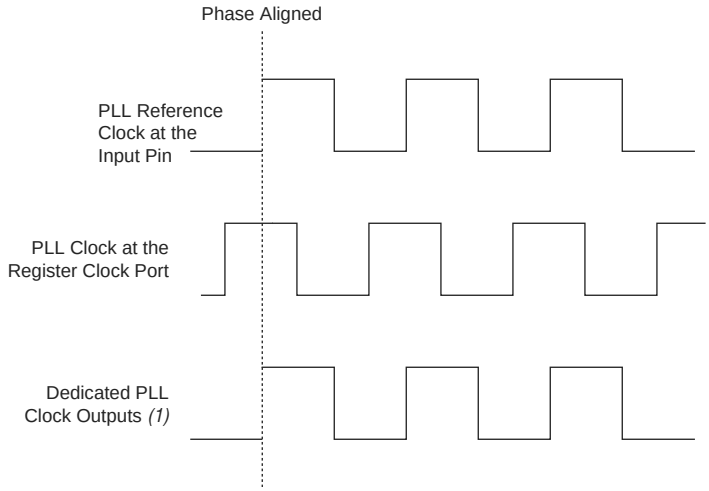


Note to Figure 6–17:

(1) You can use the `clkena` signals to enable or disable the global and regional networks or the `PLL_<#>_CLKOUT` pins.

Figure 6–28 shows an example waveform of the PLL clocks' phase relationship in ZDB mode.

Figure 6–28. Phase Relationship Between PLL Clocks in Zero Delay Buffer Mode



Note to Figure 6–28:

(1) The internal PLL clock output can lead or lag the external PLL clock outputs.

External Feedback Mode

In external feedback (EFB) mode, the external feedback input pin (`fbin`) is phase-aligned with the clock input pin, as shown in Figure 6–30. Aligning these clocks allows you to remove clock delay and skew between devices. This mode is supported on all Stratix III PLLs.

In this mode, the output of the `M` counter (`FBOUT`) feeds back to the PLL `fbin` input (using a trace on the board) becoming part of the feedback loop. Also, you can use one of the dual-purpose external clock outputs as the `fbin` input pin in EFB mode.

When using this mode, you must use the same I/O standard on the input clock, feedback input, and output clocks. Left/Right PLLs support EFB mode when using single-ended I/O standards only. Figure 6–29 shows the EFB mode implementation in Stratix III devices.

High-bandwidth PLL settings are not supported in external feedback mode. Select a ”low“ or “medium” PLL bandwidth in the ALTPLL MegaWizard Plug-In Manager when using PLLs in external feedback mode.

Figure 6–29. External Feedback Mode in Stratix III Devices

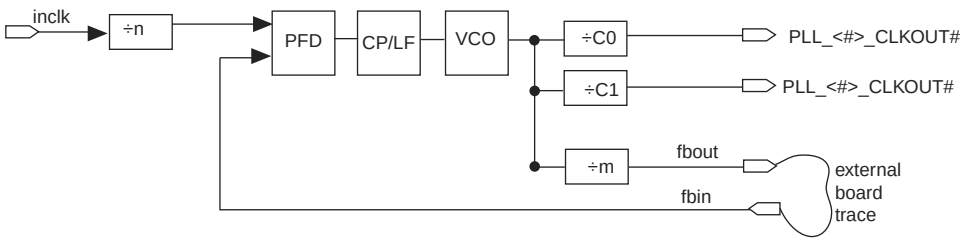
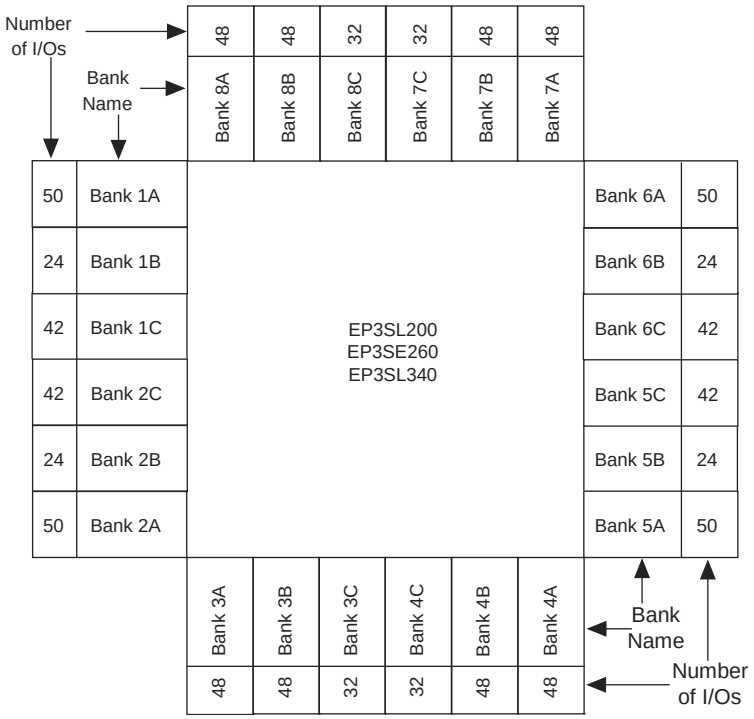


Figure 7–5. Number of I/Os in Each Bank in EP2SL200, EP3SE260, and EP3SL340 Devices in the 1517-Pin FineLine BGA Package *(Note 1), (2)*



Notes to Figure 7–5:

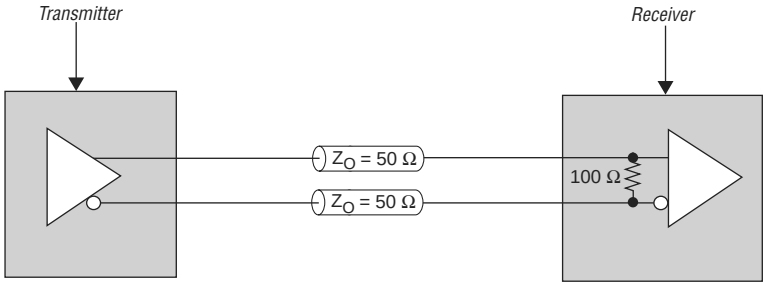
(1) All I/O pin counts include dedicated clock inputs pins. The pin count includes all general purpose I/O, dedicated clock pins, and dual-purpose configuration pins. Dedicated configuration pins are not included in the pin count.

(2) Figure 7–5 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

LVDS Input On-Chip Termination (R_D)

Stratix III devices support OCT for differential LVDS input buffers with a nominal resistance value of 10 Ω, as shown in Figure 7–12. You can enable OCT R_D in row I/O banks when V_{CCIO} and V_{CCPD} are set to 2.5 V. The column I/O banks do not support OCT R_D. The dedicated clock input pairs `CLK[1,3,8,10][p,n]`, `PLL_L[1,4]_CLK[p,n]`, and `PLL_R[1,4]_CLK[p,n]` on the row I/O banks of the Stratix III devices do not support OCT R_D. Dedicated clock input pairs `CLK[0,2,9,11][p,n]` on row I/O banks support OCT R_D. Dedicated clock input pairs `CLK[4,5,6,7][p,n]` and `CLK[12,13,14,15][p,n]` on column I/O banks do not support OCT R_D.

Figure 7–12. Differential Input On-Chip Termination



For more information about OCT R_D, refer to the *High Speed Differential I/O Interfaces with DPA in Stratix III Devices* chapter.

Table 7–11 lists the assignment name and its value for OCT R_D in the Quartus II software Assignment Editor.

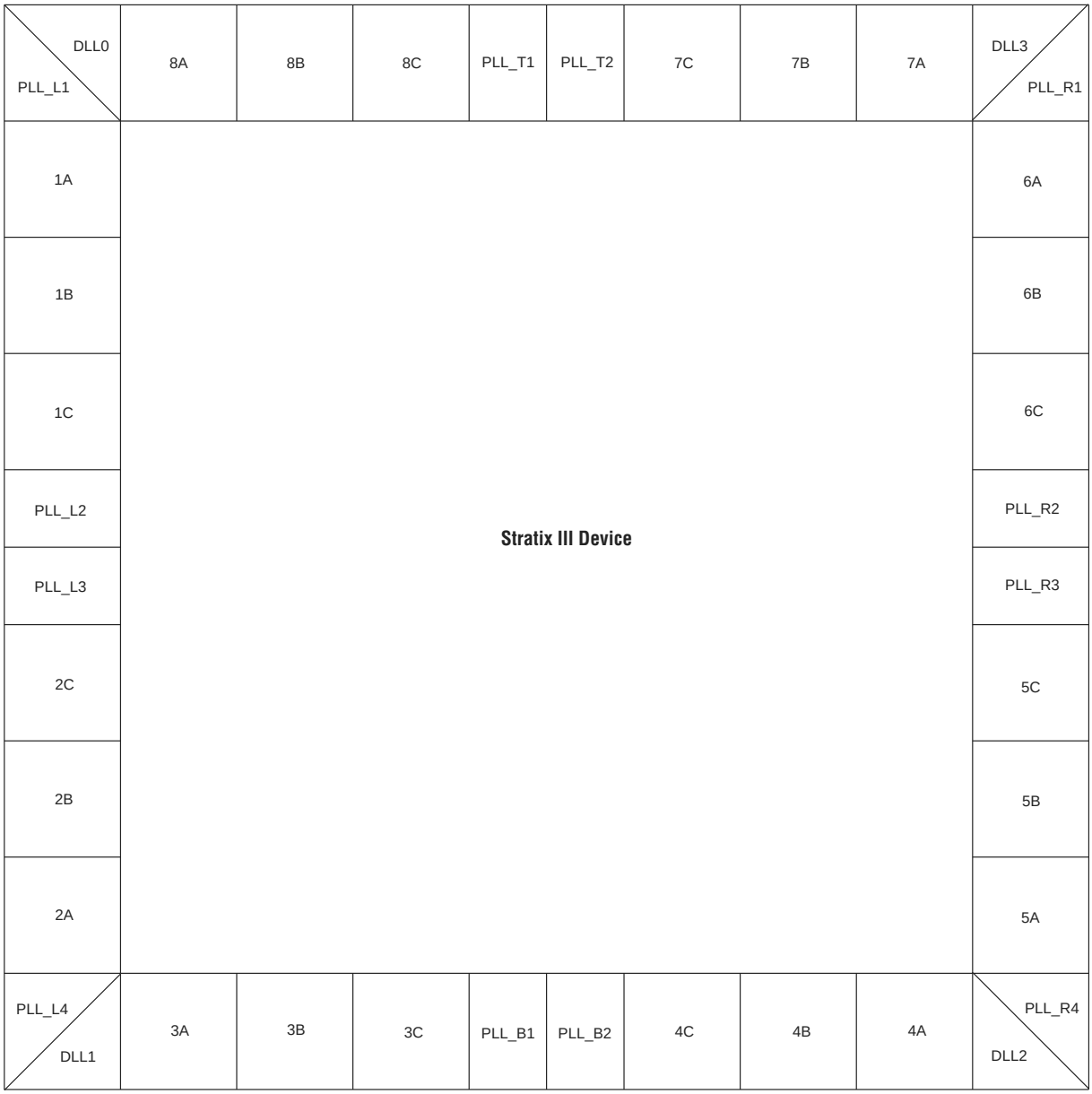
You must set the V_{CCIO} to 2.5 V when OCT R_D is used for the LVDS input buffer, even if the LVDS input buffer is powered by V_{CCPD}.

Table 7–11. On-Chip Differential Termination in Quartus II Software Assignment Editor

Assignment Name	Allowed Values	Applies To
Input Termination (Accepts wildcards/groups)	Parallel 50 Ω with calibration	Input buffers for single-ended and differential-HSTL/SSTL standards
	Differential	Input buffers for LVDS receivers on row I/O banks.
Output Termination	Series 25 Ω without calibration	Output buffers for single-ended LVTTL/LVCMOS and HSTL/SSTL standards as well as differential HSTL/SSTL standards.
	Series 50 Ω without calibration	
	Series 25 Ω with calibration	
	Series 40 Ω with calibration	
	Series 50 Ω with calibration	
	Series 60 Ω with calibration	

Figure 8–1 shows a package bottom view for Stratix III external memory support, showing the phase-locked loop (PLL), delay-locked loop (DLL), and I/O banks. The number of available I/O banks and PLLs depend on the device density.

Figure 8–1. Package Bottom View for Stratix III Devices *(Note 1), (2)*



Notes to Figure 8–1:

(1) The number of I/O banks and PLLs available depends on the device density.

(2) There is only one PLL in the center of each side of the device in EP3SL50, EP3SL70, and EP3SE50 devices.

Figure 8–7. DQS/DQ Bus Mode Support per Bank in EP3SL340 Devices in the 1760-pin FineLine BGA Package

Notes to Figure 8–7:

(1) You can also use DQS/DQSn pins in some of the ×4 groups as RUP/RDN pins. You cannot use a ×4 group for memory interfaces if two pins of the group are being used as RUP and RDN pins for OCT calibration. You can still use the ×16/×18 or ×32/×36 groups that includes these ×4 groups. However, there are restrictions on using ×8/×9 groups that include these ×4 groups as described on page 8–5.

(2) All I/O pin counts include eight dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n, CLK8p, CLK8n, CLK10p, and CLK10n) and eight dedicated corner PLL clock inputs (PLL_L1_CLKp, PLL_L1_CLKn, PLL_L4_CLKp, PLL_L4_CLKn, PLL_R4_CLKp, PLL_R4_CLKn, PLL_R1_CLKp, and PLL_R1_CLKn) that can be used for data inputs.

(3) Some of the DQS/DQ pins in this bank can also be used as configuration pins. Choose the DQS/DQ pins that are not going to be used by your configuration scheme.

Memory Clock Pins

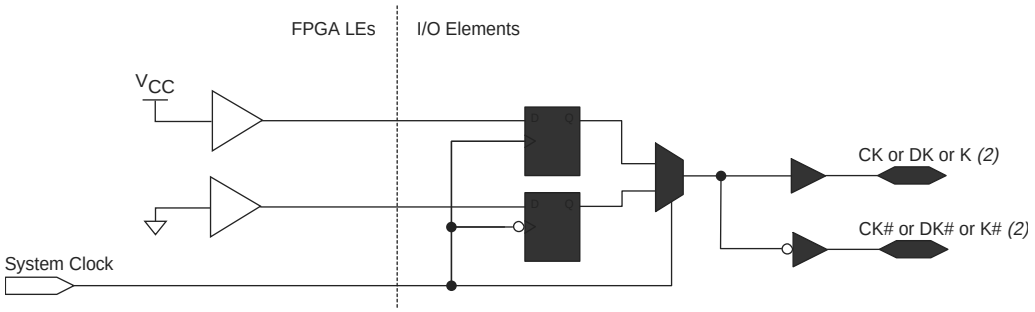
In addition to DQS (and CQn) signals to capture data, DDR3, DDR2, DDR SDRAM, and RLDRAM II use an extra pair of clocks, called CK and CK# signals, to capture the address and control/command signals. The CK/CK# signals must be generated to mimic the write data-strobe using Stratix III DDR I/O registers (DDIOs) to ensure that timing relationships between the CK/CK# and DQS signals (t_{DQSS} in DDR3, DDR2, and DDR SDRAM or t_{CKDK} in RLDRAM II) are met. QDR II+ and QDR II SRAM devices use the same clock (K/K#) to capture data, address, and control/command signals.

Memory clock pins in Stratix III devices are generated with a DDIO register going to differential output pins, marked in the pin table with `DIFFOUT`, `DIFFIO_TX`, and `DIFFIO_RX` prefixes.

For more information about which pins to use for memory clock pins, refer to the *Section I. Device and Pin Planning* chapter in volume 2 of the *External Memory Interface Handbook*.

Figure 8–9 shows the memory clock generation block diagram for Stratix III devices.

Figure 8–9. Memory Clock Generation Block Diagram *(Note 1)*



Notes to Figure 8–9:

(1) For more information about pin location requirements for these pins, refer *Section I. Device and Pin Planning* chapter in volume 2 of the *External Memory Interface Handbook*.

(2) The `mem_clk[0]` and `mem_clk_n[0]` pins for DDR3, DDR2, and DDR SDRAM interfaces use the I/O input buffer for feedback; therefore, bi-directional I/O buffers are used for these pins. For memory interfaces using a differential DQS input, the input feedback buffer is configured as differential input; for memory interfaces using a single-ended DQS input, the input buffer is configured as a single-ended input. Using a single-ended input feedback buffer requires that I/O standard's V_{REF} voltage is provided to that I/O bank's VREF pins.

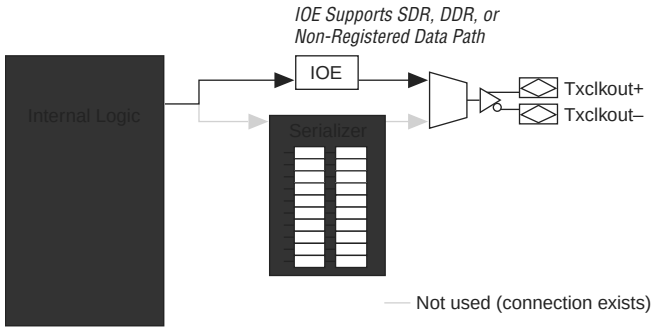
Stratix III External Memory Interface Features

Stratix III devices are rich with features that allow robust high-performance external memory interfacing. The ALTMEMPHY megafunction allows you to set these external memory interface features and helps set up the physical interface (PHY) best suited for your system. This section describes each Stratix III device feature that is used in external memory interfaces from the DQS phase-shift circuitry, DQS logic block, leveling multiplexers, dynamic OCT control block, IOE registers, IOE features, and PLLs.

You can bypass the Stratix III serializer to support DDR (×2) and SDR (×1) operations to achieve a serialization factor of 2 and 1, respectively. The I/O element (IOE) contains two data output registers that can each operate in either DDR or SDR mode. The clock source for the registers in the IOE can come from any routing resource, from the left/right PLL (PLL_Lx/PLL_Rx) or from the top/bottom (PLL_Tx/PLL_Bx) PLL.

Figure 9–4 shows the serializer bypass path.

Figure 9–4. Serializer Bypass for Stratix III Devices



For more information about how to use the differential transmitter, refer to the *ALTLVDS Megafunction User Guide*.

Differential Receiver

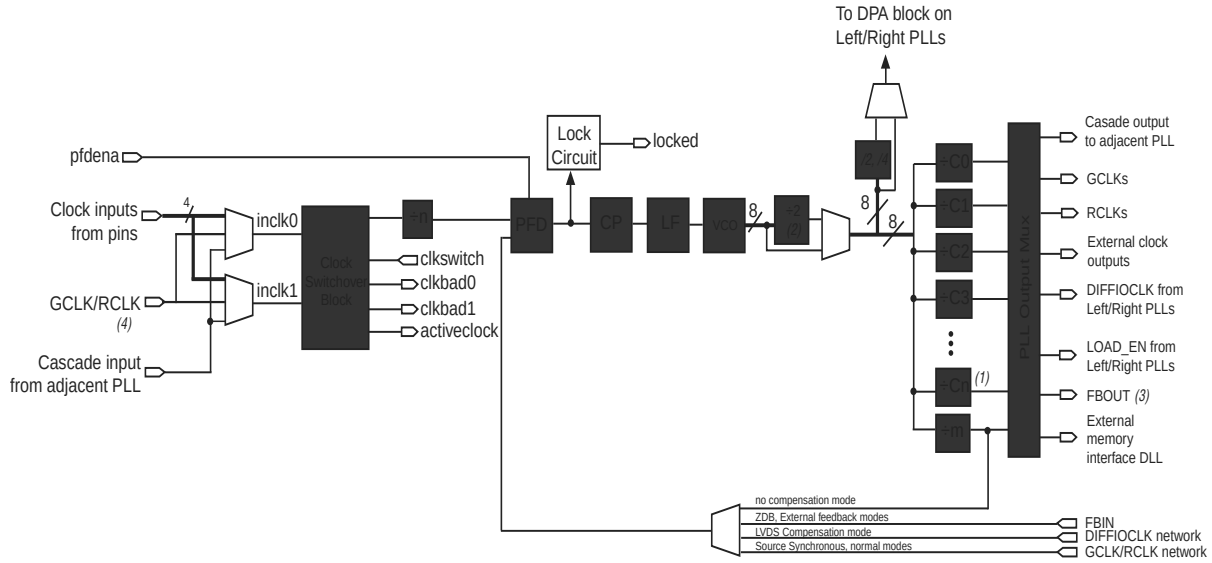
The Stratix III device has dedicated circuitry to receive high-speed differential signals. The receiver has a differential buffer, a shared PLL_Lx/PLL_Rx, DPA block, synchronization FIFO buffer, data realignment block, and a deserializer. The differential buffer can receive LVDS, mini-LVDS, and RSDS signal levels, which are statically set in the Quartus II software Assignment Editor. The PLL receives the external source clock input that is transmitted with the data and generates different phases of the same clock. The DPA block chooses one of the clocks from the left/right PLL and aligns the incoming data on each channel.

The synchronizer circuit is a 1-bit wide by 6-bit deep FIFO buffer that compensates for any phase difference between the DPA clock and the data realignment block. If necessary, the data realignment circuit can insert a single bit of latency in the serial bit stream to align to the word boundary. The deserializer includes shift registers and parallel load registers, and sends a maximum of 10 bits to the internal logic. The data path in the Stratix III receiver is clocked by either a `dffioclk` signal or the DPA recovered clock. The deserialization factor can be statically set to ×3, ×4, ×5, ×6, ×7, ×8, ×9, or ×10 with the Quartus II software. The left/right PLLs (PLL_Lx/PLL_Rx) generate the load enable signal, which is derived from the deserialization factor setting.

To support DDR (×2) or SDR (×1) operations, you can bypass the Stratix III deserializer in MegaWizard Plug-In Manager in the Quartus II software. You cannot use the DPA and the data realignment circuit when the deserializer is bypassed. The IOE contains two data input registers that can operate in DDR or SDR mode. The clock source for the registers in the IOE can come from any routing resource, from the left/right PLLs or from the top/bottom PLLs. Figure 9–5 shows the block of the Stratix III receiver.

Figure 9–12 shows a simplified block diagram of the major components of the Stratix III PLL.

Figure 9–12. PLL Block Diagram for Stratix III Devices



Notes to Figure 9–12:

(1) n = 6 for Left/Right PLLs; n = 9 for Top/Bottom PLLs.

(2) This is the VCO post-scale counter K.

(3) The FBOUT port is fed by the M counter in Stratix III PLLs.

(4) The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal or general purpose I/O pin cannot drive the PLL.

Chapter Revision History

Table 10–4 lists the revision history for this chapter.

Table 10–4. Chapter Revision History

Date	Version	Changes Made
March 2010	1.7	■ Updated for the Quartus II software version 9.1 SP2 release. ■ Minor text edits.
February 2009	1.6	■ Updated "Hot Socketing Feature Implementation in Stratix III Devices" section. ■ Removed "Referenced Documents" section.
October 2008	1.5	■ Updated Table 10–3. ■ Updated "Insertion or Removal of a Stratix III Device from a Powered-Up System" and "Power-On Reset Circuitry" sections. ■ Updated Figure 10–3. ■ Added Table 10–1. ■ Updated New Document Format.
July 2008	1.4	Updated Table 10–2.
May 2008	1.3	■ Updated "Insertion or Removal of a Stratix III Device from a Powered-Up System", "Hot Socketing Feature Implementation in Stratix III Devices", and "Power-On Reset Circuitry" sections. ■ Updated "Power-On Reset Specifications" section tables.
October 2007	1.2	■ Added section "Referenced Documents". ■ Added live links for references.
May 2007	1.1	All instances of VCCR changed to VCCPT in text, and in Figure 10–3, and Table 10–1.
November 2006	1.0	Initial Release.

Upon power-up, the Stratix III devices go through a POR. The POR delay is dependent on the PORSEL pin setting. When PORSEL is driven low, the POR time is approximately 100 ms. If PORSEL is driven high, the POR time is approximately 12 ms. During POR, the device will reset, hold nSTATUS low, and tri-state all user I/O pins. After the device successfully exits POR, all user I/O pins continue to be tri-stated. If nIO_pullup is driven low during power-up and configuration, the user I/O pins and dual-purpose I/O pins will have weak pull-up resistors which are on (after POR) before and during configuration. If nIO_pullup is driven high, the weak pull-up resistors are disabled.

The configuration cycle consists of three stages: reset, configuration and initialization. While nCONFIG or nSTATUS are low, the device is in reset. To initiate configuration in this scheme, the download cable generates a low-to-high transition on the nCONFIG pin.

To begin configuration, power the V_{CC}, V_{CCIO}, V_{CCPGM}, and V_{CCPD} voltages (for the banks where the configuration and JTAG pins reside) to the appropriate voltage levels.

When nCONFIG goes high, the device comes out of reset and releases the open-drain nSTATUS pin, which is then pulled high by an external 10-kΩ pull-up resistor. After nSTATUS is released, the device is ready to receive configuration data and the configuration stage begins. The programming hardware or download cable then places the configuration data one bit at a time on the device's DATA0 pin. The configuration data is clocked into the target device until CONF_DONE goes high. The CONF_DONE pin must have an external 10-kΩ pull-up resistor in order for the device to initialize.

When using a download cable, setting the **Auto-restart configuration after error** option does not affect the configuration cycle because you must manually restart configuration in the Quartus II software when an error occurs. Additionally, the **Enable user-supplied start-up clock** (**CLKUSR**) option has no affect on the device initialization since this option is disabled in the SOF when programming the device using the Quartus II programmer and download cable. Therefore, if you turn on the CLKUSR option, you do not need to provide a clock on CLKUSR when you are configuring the device with the Quartus II programmer and a download cable.

Figure 11–17 shows PS configuration for Stratix III devices using a USB-Blaster, MasterBlaster, ByteBlaster II, ByteBlasterMV, or EthernetBlaster cable.

Security Against Reverse Engineering

Reverse engineering from an encrypted configuration file is very difficult and time consuming because the Stratix III configuration file formats are proprietary and the file contains million of bits which require specific decryption. Reverse engineering the Stratix III device is just as difficult because the device is manufactured on the most advanced 65-nm process technology.

Security Against Tampering

The non-volatile keys are one-time programmable. Once the tamper protection bit is set in the key programming file generated by the Quartus® II software, the Stratix III device can only be configured with configuration files encrypted with the same key.

For more information about why this feature is secured, refer to the *Design Security in Stratix III Devices white paper*.

AES Decryption Block

The main purpose of the AES decryption block is to decrypt the configuration bitstream prior to entering data decompression or configuration.

Prior to receiving encrypted data, you must enter and store the 256-bit security key in the device. You can choose between a non-volatile security key and a volatile security key with battery backup.

The security key is scrambled prior to storing it in key storage in order to make it more difficult for anyone to retrieve the stored key using de-capsulation of the device.

Flexible Security Key Storage

Stratix III devices support two types of security key programming: volatile and non-volatile. Table 14–1 shows the differences between volatile keys and non-volatile keys.

Table 14–1. Security Keys Options

Options	Volatile Key	Non-Volatile Key
Key programmability	Reprogrammable and erasable	One-time programmable
External battery	Required	Not required
Key programming method *(1)*	On-board	On and off board
Design protection	Secure against copying and reverse engineering	Secure against copying and reverse engineering. Tamper resistant if tamper protection bit is set.

Note to Table 14–1:

(1) Key programming is carried out using JTAG interface.

You can program the non-volatile key to the Stratix III device without an external battery. Also, there are no additional requirements to any of the Stratix III power supply inputs.

Thermal Resistance

For Stratix III devices thermal resistance specifications, refer to the *Stratix Series Device Thermal Resistance Data Sheet*.

Package Outlines

You can download Stratix III device package outlines from the *Device Packaging Specifications* web page.

Chapter Revision History

Table 17–2 lists the revision history for this chapter.

Table 17–2. Chapter Revision History

Date	Version	Changes Made
March 2010	1.7	Updated for the Quartus II software version 9.1 SP2 release: ■ Updated Table 17–1. ■ Minor text edits.
February 2009	1.6	Removed "Referenced Documents" section.
October 2008	1.5	Updated New Document Format.
May 2008	1.4	Updated "Package Outlines" section hyperlink.
November 2007	1.3	Updated Table 17–1.
October 2007	1.2	■ Added new section "Referenced Documents". ■ Added live links for references.
May 2007	1.1	Removed thermal resistance and package outline information and replaced with links referencing this information.
November 2006	1.0	Initial Release.