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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	10200
Number of Logic Elements/Cells	255000
Total RAM Bits	16672768
Number of I/O	488
Number of Gates	-
Voltage - Supply	0.86V ~ 1.15V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-HBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep3se260h780c3n

Table 1–5. Speed Grades for Stratix III Devices (Part 2 of 2)

Device	Temperature Grade	484 -Pin FineLine BGA	780-Pin FineLine BGA	780-Pin Hybrid FineLine BGA	1152-Pin FineLine BGA	1152-Pin Hybrid FineLine BGA	1517-Pin FineLine BGA	1760-Pin FineLine BGA
EP3SE260	Commercial	—	—	–2, –3, –4, –4L	–2,– 3, –4, –4L	—	–2, –3, –4, –4L	—
	Industrial *(1)*	—	—	–3, –4, –4L	–3, –4, –4L	—	–3, –4,–4L	—

Note to Table 1–5:

(1) For EP3SL340, EP3SL200, and EP3SE260 devices, the industrial junction temperature range for –4L is 0–100°C, regardless of supply voltage.

Architecture Features

The following section describes the various features of the Stratix III family FPGAs.

Logic Array Blocks and Adaptive Logic Modules

The Logic Array Block (LAB) is composed of basic building blocks known as Adaptive Logic Modules (ALMs) that can be configured to implement logic, arithmetic, and register functions. Each LAB consists of ten ALMs, carry chains, shared arithmetic chains, LAB control signals, local interconnect, and register chain connection lines. ALMs are part of a unique, innovative logic structure that delivers faster performance, minimizes area, and reduces power consumption. ALMs expand the traditional 4-input look-up table architecture to 7 inputs, increasing performance by reducing LEs, logic levels, and associated routing. In addition, ALMs maximize DSP performance with dedicated functionality to efficiently implement adder trees and other complex arithmetic functions. The Quartus II Compiler places associated logic in an LAB or adjacent LABs, allowing the use of local, shared arithmetic chain, and register chain connections for performance and area efficiency.

The Stratix III LAB has a new derivative called Memory LAB (or MLAB), which adds SRAM memory capability to the LAB. MLAB is a superset of the LAB and includes all LAB features. MLABs support a maximum of 320 bits of simple dual-port Static Random Access Memory (SRAM). Each ALM in an MLAB can be configured as a 16×2 block, resulting in a configuration of 16×20 simple dual port SRAM block. MLAB and LAB blocks always co-exist as pairs in all Stratix III families, allowing up to 50% of the logic (LABs) to be traded for memory (MLABs).

For more information about LABs and ALMs, refer to the *Logic Array Blocks and Adaptive Logic Modules in Stratix III Devices* chapter.

For more information about MLAB modes, features and design considerations, refer to the *TriMatrix Embedded Memory Blocks in Stratix III Devices* chapter.

Stratix III devices support configuration data decompression, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and transmit this compressed bitstream to Stratix III devices. During configuration, the Stratix III device decompresses the bitstream in real time and programs its SRAM cells.

Stratix III devices support decompression in the FPP when using a MAX II device/microprocessor plus flash, fast AS, and PS configuration schemes. The Stratix III decompression feature is not available in the FPP when using the enhanced configuration device and JTAG configuration schemes.

For more information, refer to the *Configuring Stratix III Devices* chapter.

Remote System Upgrades

Stratix III devices feature remote system upgrade capability, allowing error-free deployment of system upgrades from a remote location securely and reliably. Soft logic (either the Nios embedded processor or user logic) implemented in a Stratix III device can download a new configuration image from a remote location, store it in configuration memory, and direct the dedicated remote system upgrade circuitry to initiate a reconfiguration cycle. The dedicated circuitry performs error detection during and after the configuration process, and can recover from an error condition by reverting back to a safe configuration image, and provides error status information. This dedicated remote system upgrade circuitry is unique to Stratix series FPGAs and helps to avoid system downtime.

For more information, refer to the *Remote System Upgrades with Stratix III Devices* chapter.

IEEE 1149.1 (JTAG) Boundary-Scan Testing

Stratix III devices support the JTAG IEEE Std. 1149.1 specification. The Boundary-Scan Test (BST) architecture offers the capability to test pin connections without using physical test probes and capture functional data while a device is operating normally. Boundary-scan cells in the Stratix III device can force signals onto pins or capture data from pin or logic array signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared to expected results. In addition to BST, you can use the IEEE Std. 1149.1 controller for Stratix III device in-circuit reconfiguration (ICR).

For more information, refer to the *IEEE 1149.1 (JTAG) Boundary Scan Testing in Stratix III Devices* chapter.

Design Security

Stratix III devices are high-density, high-performance FPGAs with support for 256-bit volatile and non-volatile security keys to protect designs against copying, reverse engineering, and tampering. Stratix III devices have the ability to decrypt a configuration bitstream using the Advanced Encryption Standard (AES) algorithm, an industry standard encryption algorithm that is FIPS-197 certified and requires a 256-bit security key.

Each ALM has two sets of outputs that drive the local, row, and column routing resources. The LUT, adder, or register output can drive these output drivers (refer to Figure 2–6). For each set of output drivers, two ALM outputs can drive column, row, or direct link routing connections, and one of these ALM outputs can also drive local interconnect resources. This allows the LUT or adder to drive one output while the register drives another output.

This feature, called register packing, improves device utilization because the device can use the register and the combinational logic for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same ALM so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The ALM can also drive out registered and unregistered versions of the LUT or adder output.

ALM Operating Modes

The Stratix III ALM can operate in one of the following modes:

- Normal
- Extended LUT Mode
- Arithmetic
- Shared Arithmetic
- LUT-Register

Each mode uses ALM resources differently. In each mode, eleven available inputs to an ALM—the eight data inputs from the LAB local interconnect, carry-in from the previous ALM or LAB, the shared arithmetic chain connection from the previous ALM or LAB, and the register chain connection—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all ALM modes.

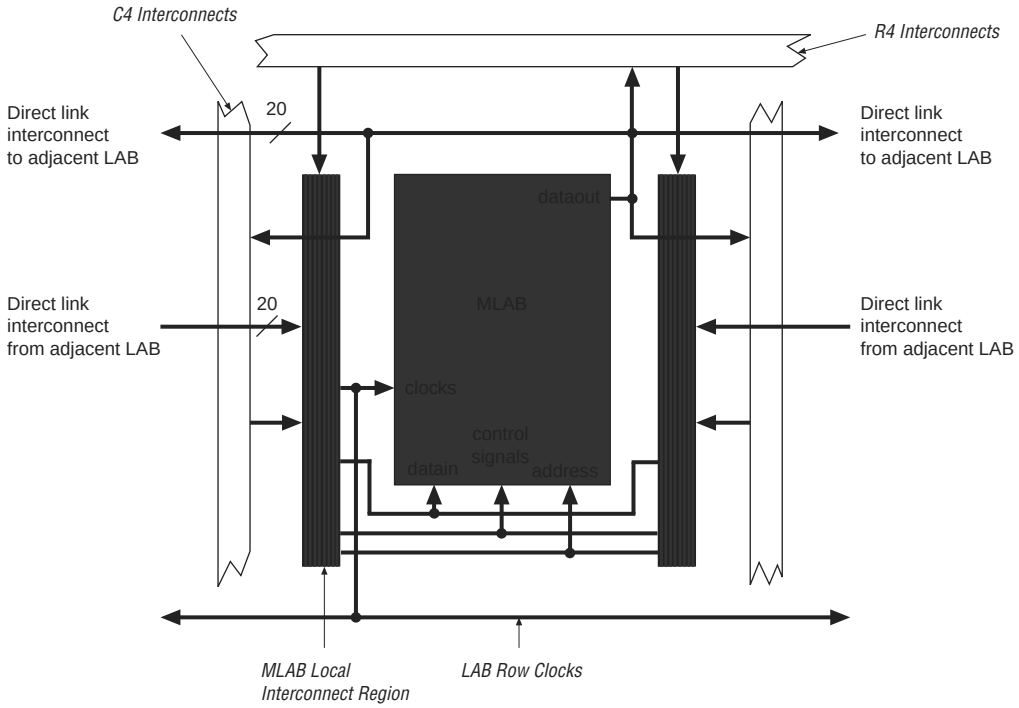
☞ Refer to “LAB Control Signals” on page 2–4 for more information on the LAB-wide control signals.

The Quartus II software and supported third-party synthesis tools, in conjunction with parameterized functions such as the library of parameterized modules (LPM) functions, automatically choose the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions.

Normal Mode

The normal mode is suitable for general logic applications and combinational functions. In this mode, up to eight data inputs from the LAB local interconnect are inputs to the combinational logic. The normal mode allows two functions to be implemented in one Stratix III ALM, or an ALM to implement a single function of up to six inputs. The ALM can support certain combinations of completely independent functions and various combinations of functions that have common inputs. Figure 2–7 shows the supported LUT combinations in normal mode.

Figure 3–4. MLAB RAM Block LAB Row Interface



The M9K RAM block local interconnect is driven by the R4, C4, and direct link interconnects from adjacent LABs. The M9K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 20 direct link input connections to the M9K RAM Block are possible from the left adjacent LABs and another 20 possible from the right adjacent LAB. M9K RAM block outputs can also connect to left and right LABs through direct link interconnect. Figure 3–5 shows the M9K RAM block to logic array interface.

In simple dual-port mode, M9K and M144K blocks support separate write-enable and read-enable signals. You can save power by keeping the read-enable signal low (inactive) when not reading. Read-during-write operations to the same address can either output a don't care value or old data. To choose the desired behavior, set the read-during-write behavior to either don't care or old data in the RAM MegaWizard Plug-In Manager in the Quartus II software. See "Read During Write" on page 4–21 for more details about this behavior.

MLABs only support a write-enable signal. Read-during-write behavior for the MLABs can be either don't care, new data, or old data. The available choices depend on the configuration of the MLAB.

Figure 4–13 shows the timing waveforms for read and write operations in simple dual-port mode with unregistered outputs in M9K and M144K. Registering the RAM's outputs would simply delay the q output by one clock cycle in M9k and M144K.

Figure 4–13. Stratix III Simple Dual-Port Timing Waveforms for M9K and M144K

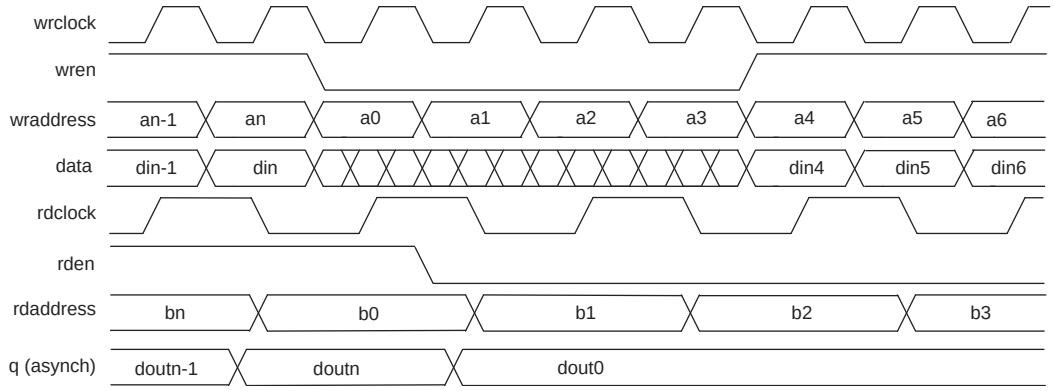


Figure 4–14 shows the timing waveforms for read and write operations in simple dual-port mode with unregistered outputs in MLABs. In MLABs, the write operation is triggered by the falling clock edges.

Figure 4–14. Stratix III Simple Dual-Port Timing Waveforms for MLABs

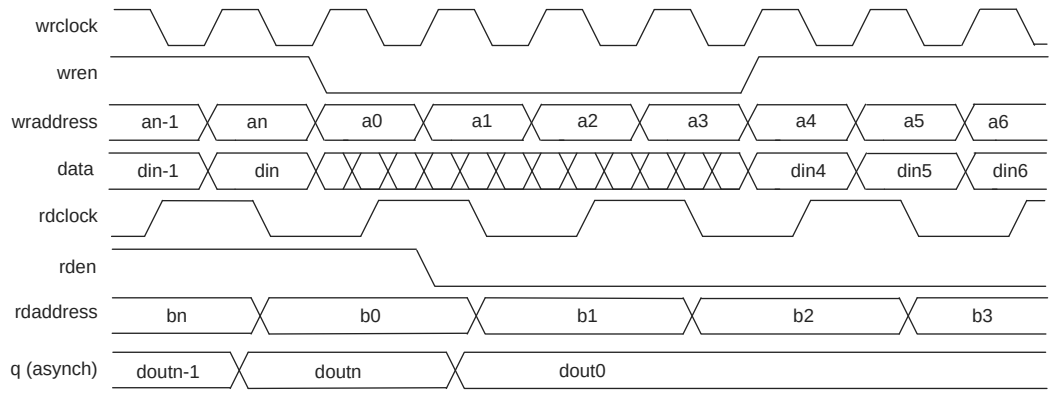
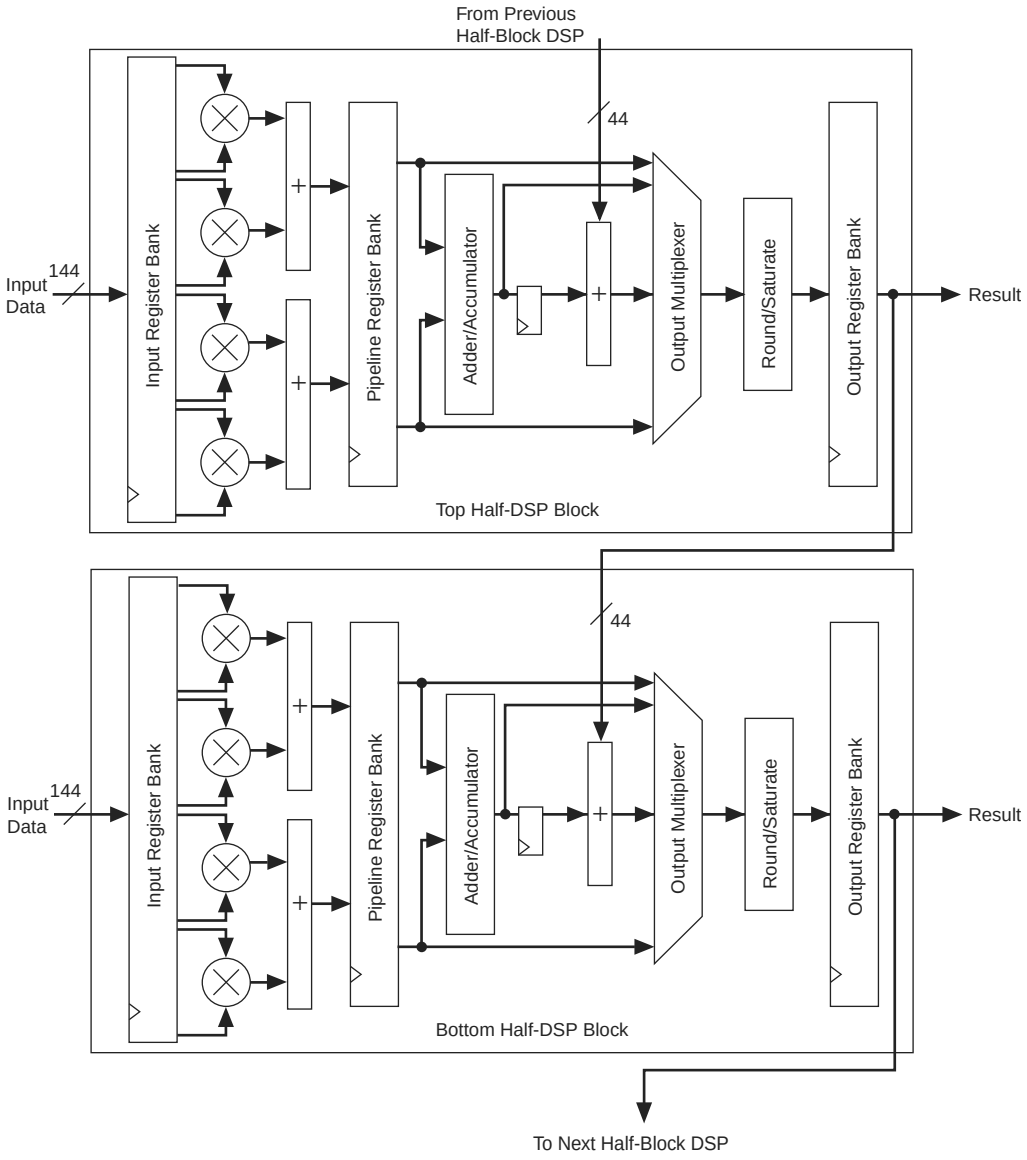


Figure 5–5. Stratix III Full DSP Block Summary



Shift registers are useful in DSP functions such as FIR filters. When implementing 18 × 18 or smaller width multipliers, you do not need external logic to create the shift register chain because the input shift registers are internal to the DSP block. This implementation significantly reduces the logical element (LE) resources required, avoids routing congestion, and results in predictable timing.

The first multiplier in every half DSP block (top- and bottom-half) in Stratix III devices has a multiplexer for the first multiplier B-input (lower-leg input) register to select between general routing and loopback, as shown in Figure 5–6. In loopback mode, the most significant 18-bit registered outputs are connected as feedback to the multiplier input of the first top multiplier in each half DSP block. Loopback modes are used by recursive filters where the previous output is needed to compute the current output.

The loopback mode is described in detail in "Two-Multiplier Adder Sum Mode" on page 5–21.

Table 5–3 lists the input register modes for the DSP block.

Table 5–3. Input Register Modes

Register Input Mode *(1)*	9 × 9	12 × 12	18 × 18	36 × 36	Double
Parallel input	✓	✓	✓	✓	✓
Shift register input *(2)*	—	—	✓	—	—
Loopback input *(3)*	—	—	✓	—	—

Notes to Table 5–3:

(1) The multiplier operand input wordlengths are statically configured at compile time.
(2) Available only on the A-operand.
(3) Only one loopback input is allowed per Half-Block. See Figure 5–15 for details.

Multiplier and First-Stage Adder

The multiplier stage natively supports 9 × 9, 12 × 12, 18 × 18, or 36 × 36 multipliers. Other wordlengths are padded up to the nearest appropriate native wordlength; for example, 16 × 16 would be padded up to use 18 × 18. Refer to "Independent Multiplier Modes" on page 5–15 for more details. Depending on the data width of the multiplier, a single DSP block can perform many multiplications in parallel.

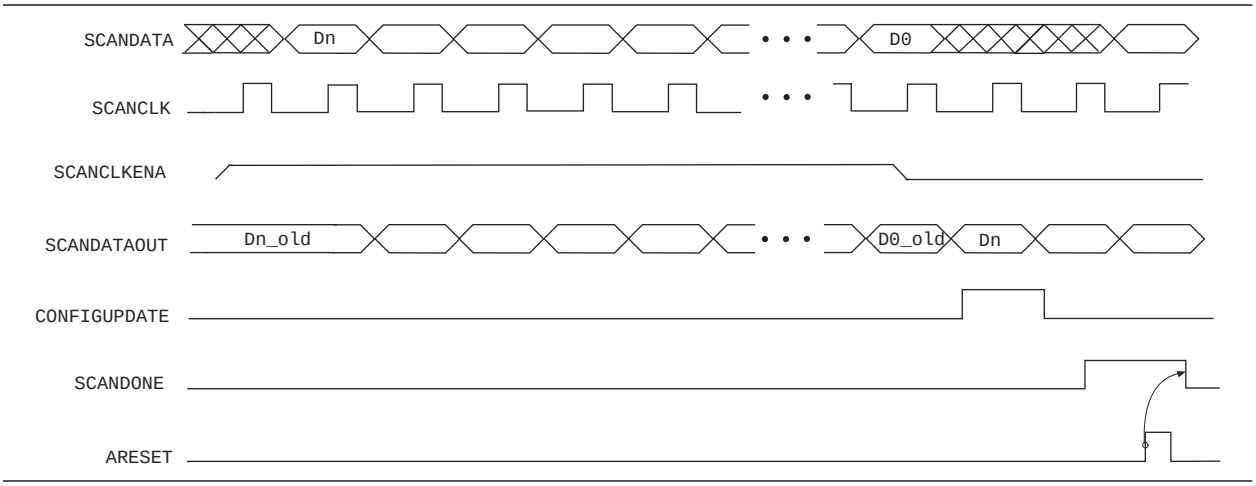
Each multiplier operand can be a unique signed or unsigned number. Two dynamic signals, `signa` and `signb`, control the representation of each operand, respectively. A `logic 1` value on the `signa/signb` signal indicates that `data A/data B` is a signed number; a `logic 0` value indicates an unsigned number. Table 5–4 lists the sign of the multiplication result for the various operand sign representations. The result of the multiplication is signed if any one of the operands is a signed value.

Table 5–4. Multiplier Sign Representation

Data A (signa Value)	Data B (signb Value)	Result
Unsigned (`logic 0`)	Unsigned (`logic 0`)	Unsigned
Unsigned (`logic 0`)	Signed (`logic 1`)	Signed
Signed (`logic 1`)	Unsigned (`logic 0`)	Signed
Signed (`logic 1`)	Signed (`logic 1`)	Signed

Figure 6–41 shows a functional simulation of the PLL reconfiguration feature.

Figure 6–41. PLL Reconfiguration Waveform



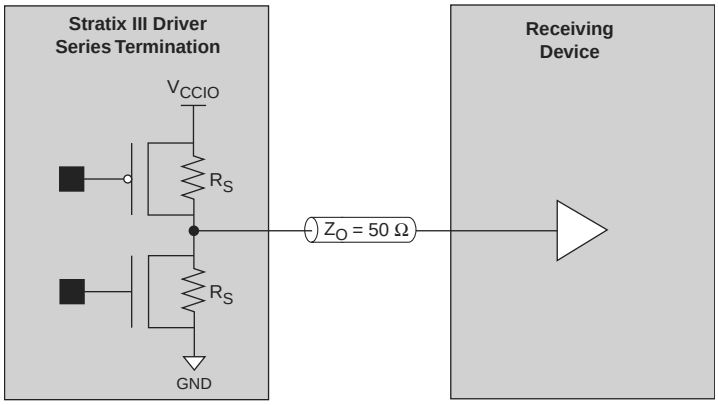
When you reconfigure the counter clock frequency, you cannot reconfigure the corresponding counter phase shift settings using the same interface. Instead, reconfigure the phase shifts in real time using the dynamic phase shift reconfiguration interface. If you reconfigure the counter frequency, but wish to keep the same non-zero phase shift setting (for example, 90 degrees) on the clock output, you must reconfigure the phase shift immediately after reconfiguring the counter clock frequency.

Post-Scale Counters (C0 to C9)

The multiply or divide values and duty cycle of post-scale counters can be reconfigured in real time. Each counter has an 8-bit high-time setting and an 8-bit low-time setting. The duty cycle is the ratio of output high- or low-time to the total cycle time, which is the sum of the two. Additionally, these counters have two control bits, `rbypass`, for bypassing the counter, and `rselodd`, to select the output clock duty cycle.

When the `rbypass` bit is set to 1, it bypasses the counter, resulting in a divide by 1. When this bit is set to 0, the high- and low-time counters are added to compute the effective division of the VCO output frequency. For example, if the post-scale divide factor is 10, the high- and low-count values could be set to 5 and 5, respectively, to achieve a 50-50% duty cycle. The PLL implements this duty cycle by transitioning the output clock from high to low on the rising edge of the VCO output clock. However, a 4 and 6 setting for the high- and low-count values, respectively, would produce an output clock with 40-60% duty cycle.

Figure 7–8. On-Chip Series Termination without Calibration for Stratix III Devices



To use OCT for the SSTL Class I standard, you should select the **50-Ω on-chip series termination** setting, eliminating the external 25-Ω R_S (to match the 50-Ω transmission line). For the SSTL Class II standard, you should select the **25-Ω on-chip series termination** setting (to match the 50-Ω transmission line and the near-end external 50-Ω pull-up to V_{TT}).

On-Chip Series Termination with Calibration

Stratix III devices support OCT R_S with calibration in all banks. The OCT R_S calibration circuit compares the total impedance of the I/O buffer to the external 25-Ω ±1% or 50-Ω ±1% resistors connected to the RUP and RDN pins, and dynamically enables or disables the transistors until they match. The R_S shown in Figure 7–9 is the intrinsic impedance of transistors. Calibration occurs at the end of device configuration. When the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers. When calibration is not taking place, the RUP and RDN pins go to a tri-state condition.

Figure 7–9. On-Chip Series Termination with Calibration for Stratix III Devices

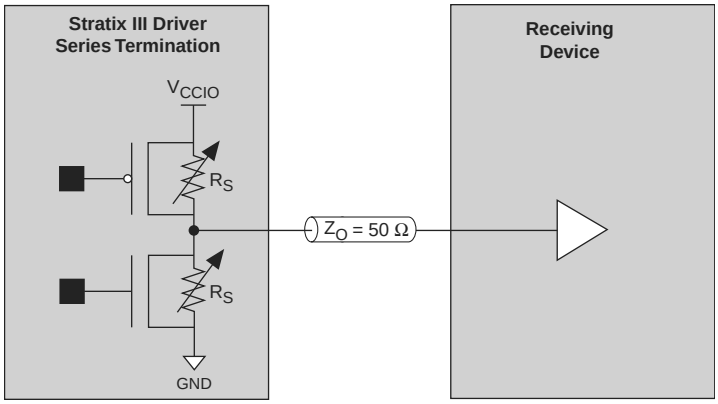
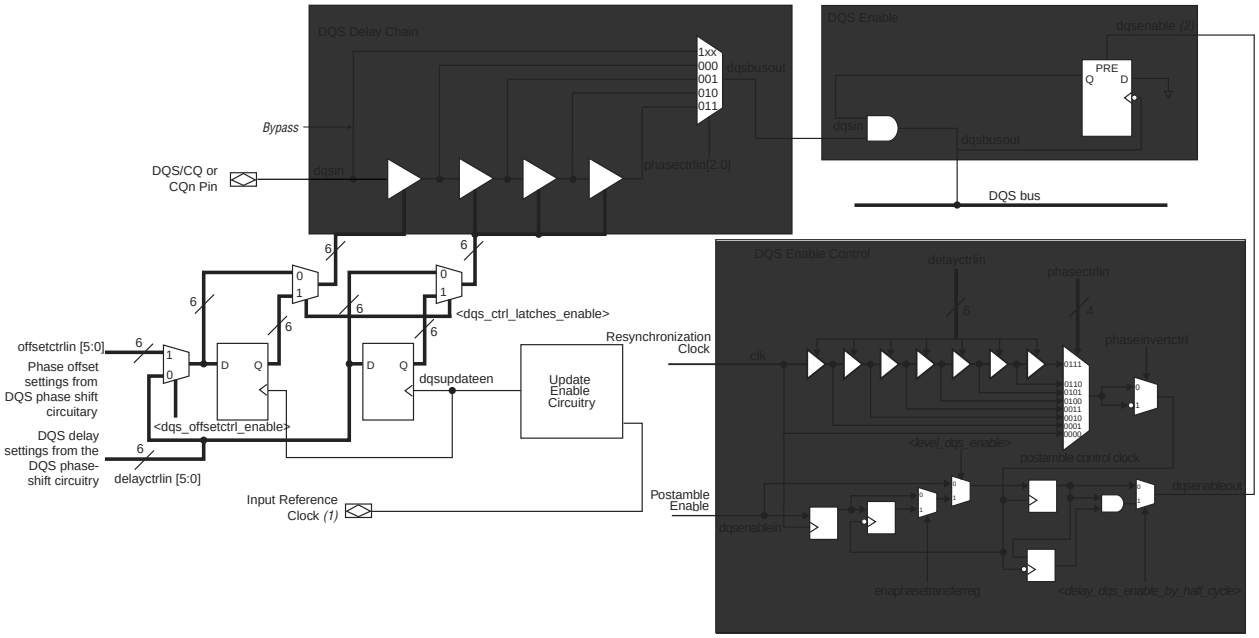


Table 7–8 lists I/O standards that support OCT R_S with calibration.

DQS Logic Block

Each DQS and CQn pin is connected to a separate DQS logic block, which consists of the DQS delay chains, update enable circuitry, and DQS postamble circuitry, as shown in Figure 8–13.

Figure 8–13. Stratix III DQS Logic Block



Notes to Figure 8–13:

(1) The input reference clock for the DQS phase-shift circuitry can come from a PLL output clock or an input clock pin. For the exact PLL and input clock pin location, refer to Table 8–6 through Table 8–9.

(2) The `dqsenable` signal can also come from the Stratix III FPGA fabric.

DQS Delay Chain

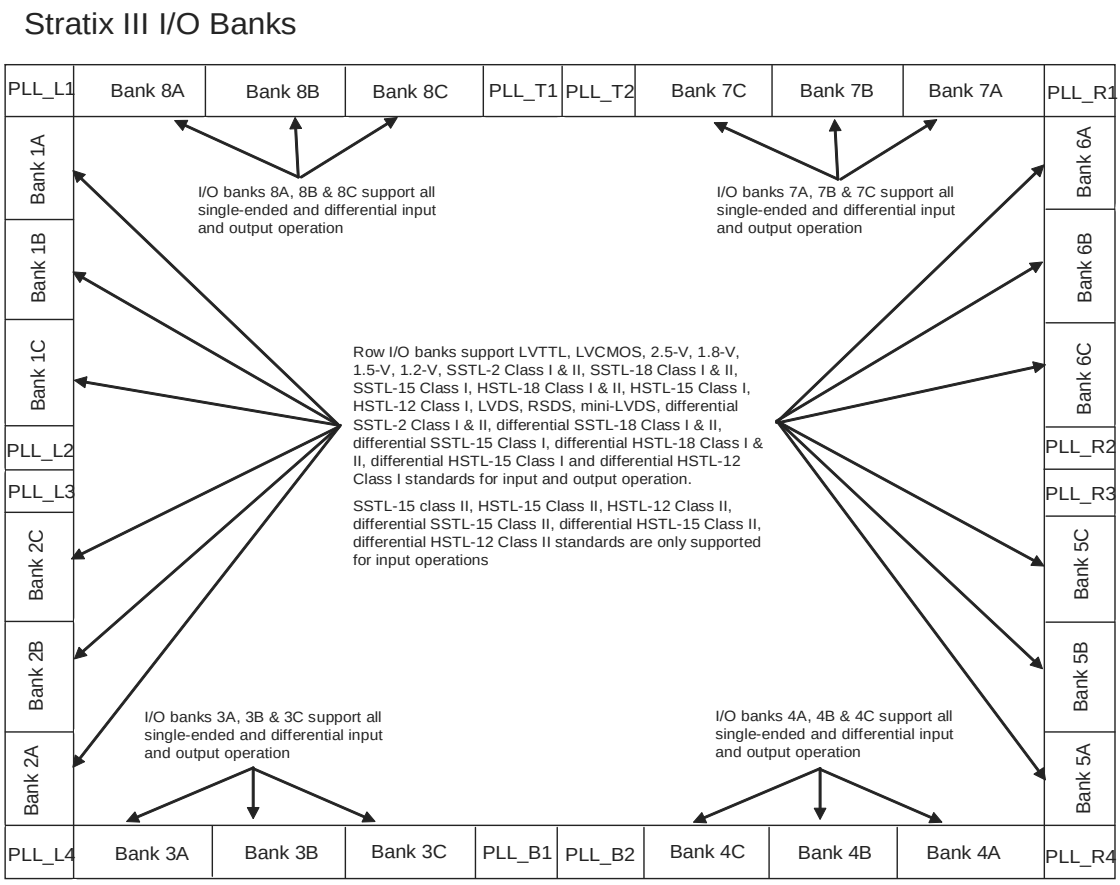
The DQS delay chains consist of a set of variable delay elements to allow the input DQS/CQ and CQn signals to be shifted by the amount specified by the DQS phase-shift circuitry or the logic array. There are four delay elements in the DQS delay chain; the first delay chain closest to the DQS/CQ pin can either be shifted by the DQS delay settings or by the sum of the DQS delay setting and the phase-offset setting. The number of delay chains required is transparent because the ALTMEMPHY megafunction automatically sets it when you choose the operating frequency. The DQS delay settings can come from the DQS phase-shift circuitry on either end of the I/O banks or from the logic array.

Delay elements in the DQS logic block have the same characteristics as the delay elements in the DLL. When the DLL is not used to control the DQS delay chains, you can input your own Gray-coded 6-bit or 5-bit settings using the `dqs_delayctrlin[5..0]`signals available in the ALTMEMPHY megafunction. These settings control 1, 2, 3, or all 4 delay elements in the DQS delay chains. The ALTMEMPHY megafunction can also dynamically choose the number of DQS delay chains required for the system. The amount of delay is equal to the sum of the delay element's intrinsic delay and the product of the number of delay steps and the value of the delay steps.

I/O Banks

Stratix III I/Os are divided into 16 to 24 I/O banks. The dedicated serializer and deserializer (SERDES) circuitry with DPA that supports high-speed differential I/Os is located in banks in the right side and left side of the device. Figure 9–1 shows the different banks and the I/O standards supported by the banks.

Figure 9–1. I/O Banks in Stratix III Devices *(Note 1), (2), (3), (4), (5), (6)*



Notes to Figure 9–1:

(1) Figure 9–1 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only. For exact locations, refer to the pin list and the Quartus II software.

(2) Differential HSTL and SSTL outputs use two single-ended (SE) outputs with the second output programmed as inverted to support differential I/O operations.

(3) Column I/O differential HSTL and SSTL inputs use LVDS differential input buffers without on-chip differential termination (OCT R_D) support.

(4) Column I/O supports LVDS outputs using SE buffers and external resistor networks.

(5) Row I/O supports PCI/PCI-X without on-chip clamping diodes.

(6) The PLL blocks are shown for location purposes only and are not considered additional banks. The PLL input and output uses the I/Os in adjacent banks.

Table 9–2 lists the LVDS channels (emulated) supported in Stratix III device column I/O banks.

Table 9–2. LVDS Channels (Emulated) Supported in Stratix III Device Column I/O Banks *(Note 1), (2)*

Device	484-Pin FineLine BGA	780-Pin FineLine BGA	1152-Pin FineLine BGA	1517-Pin FineLine BGA	1780-Pin FineLine BGA
EP3SL50	24Rx/eTx + 24eTx	64Rx/eTx + 64eTx	—	—	—
EP3SL70	24Rx/eTx + 24eTx	64Rx/eTx + 64eTx	—	—	—
EP3SL110	—	64Rx/eTx + 64eTx	96Rx/eTx + 96eTx	—	—
EP3SL150	—	64Rx/eTx + 64eTx	96Rx/eTx + 96eTx	—	—
EP3SL200	—	64Rx/eTx + 64eTx *(3)*	96Rx/eTx + 96eTx	128Rx/eTx + 128eTx	—
EP3SL340	—	—	96Rx/eTx + 96eTx *(4)*	128Rx/eTx + 128eTx	144Rx/eTx + 144eTx
EP3SE50	24Rx/eTx + 24eTx	64Rx/eTx + 64eTx	—	—	—
EP3SE80	—	64Rx/eTx + 64eTx	96Rx/eTx + 96eTx	—	—
EP3SE110	—	64Rx/eTx + 64eTx	96Rx/eTx + 96eTx	—	—
EP3SE260	—	64Rx/eTx + 64eTx *(3)*	96Rx/eTx + 96eTx	128Rx/eTx + 128eTx	—

Notes to Table 9–2:

(1) Rx = true LVDS input buffers without on-chip differential input termination.

(2) eTx = emulated LVDS output buffers, either `LVDS_E3R` or `LVDS_E1R`.

(3) The EP3SL200 and EP3SE260 FPGAs are offered in the H780 package, instead of the F780 package.

(4) The EP3SL340 FPGA is offered in the H1152 package, instead of the F1152 package.

Differential Transmitter

The Stratix III transmitter has dedicated circuitry to provide support for LVDS signaling. The dedicated circuitry consists of a differential buffer, a serializer, and a shared analog PLL (left/right PLL). The differential buffer can drive out LVDS, mini-LVDS, and RSDS signaling levels. The serializer takes up to 10-bits wide parallel data from the FPGA core, clocks it into the load registers, and serializes it using shift registers clocked by the left/right PLL before sending the data to the differential buffer. The most significant bit (MSB) of the parallel data is transmitted first.

The load and shift registers are clocked by the load enable (`load_en`) signal and the `diffioclk` (clock running at serial data rate) signal generated from PLL_Lx (left PLL) or PLL_Rx (right PLL). The serialization factor can be statically set to ×3, ×4, ×5, ×6, ×7, ×8, ×9, or ×10 with the Quartus II software. The load enable signal is derived from the serialization factor setting. Figure 9–2 shows a block diagram of the Stratix III transmitter.

Differential Pin Placement Guidelines

To ensure proper high-speed operation, differential pin placement guidelines have been established. The Quartus II compiler automatically checks that these guidelines are followed and issues an error message if they are not met.

Because DPA usage adds some constraints on the placement of high-speed differential channels, this section is divided into pin placement guidelines with and without DPA usage.

Guidelines for DPA-Enabled Differential Channels

The Stratix III device has differential receivers and transmitters in I/O banks on the left and right sides of the device. Each receiver has a dedicated DPA circuit to align the phase of the clock to the data phase of its associated channel. When DPA-enabled channels are used in differential banks, you must adhere to the guidelines listed in the following sections.

DPA-Enabled Channels and Single-Ended I/Os

When there is a DPA channel enabled in a bank, both single-ended I/Os and differential I/O standards are allowed in the bank.

Single-ended I/Os are allowed in the same I/O bank as long as the single-ended I/O standard uses the same V_{CCIO} as the DPA-enabled differential I/O bank.

DPA-Enabled Channel Driving Distance

If the number of DPA channels driven by each left/right PLL exceeds 25 LAB rows, Altera recommends implementing data realignment (bit-slip) circuitry for all the DPA channels.

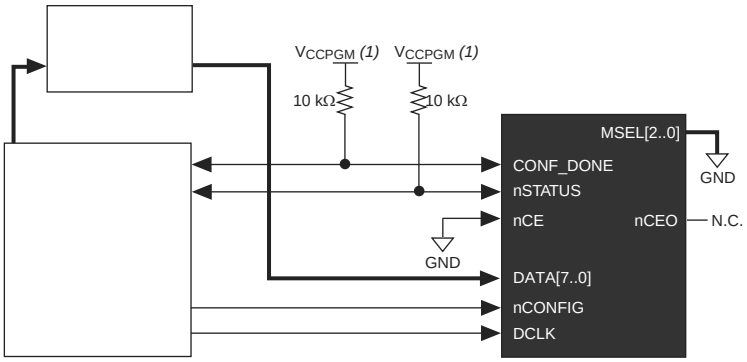
Using Corner and Center Left/Right PLLs

If a differential bank is being driven by two left/right PLLs, where the corner left/right PLL is driving one group and the center left/right PLL is driving another group, there must be at least one row of separation between the two groups of DPA-enabled channels (refer to Figure 9–18). The two groups can operate at independent frequencies.

No separation is necessary if a single left/right PLL is driving DPA-enabled channels as well as DPA-disabled channels.

Figure 11–3 shows the configuration interface connections between the Stratix III device and a MAX II device for single device configuration.

Figure 11–3. Single Device FPP Configuration Using an External Host



Note to Figure 11–3:

(1) Connect the resistor to a supply that provides an acceptable input signal for the Stratix III device. V_{CCPGM} should be high enough to meet the V_{IH} specification of the I/O on the external host. It is recommended to power up all configuration system's I/O with V_{CCPGM}.

Upon power-up, the Stratix III device goes through a POR. The POR delay is dependent on the PORSEL pin setting. When PORSEL is driven low, the POR time is approximately 100 ms. When PORSEL is driven high, the POR time is approximately 12 ms. During POR, the device resets, holds nSTATUS low, and tri-states all user I/O pins. After the device successfully exits POR, all user I/O pins continue to be tri-stated. If nIO_pullup is driven low during power-up and configuration, the user I/O pins and dual-purpose I/O pins have weak pull-up resistors, which are on (after POR) before and during configuration. If nIO_pullup is driven high, the weak pull-up resistors are disabled.

The configuration cycle consists of three stages: reset, configuration, and initialization. While nCONFIG or nSTATUS is low, the device is in the reset stage. To initiate configuration, the MAX II device must drive the nCONFIG pin from low to high.

☞ V_{CC}, V_{CCIO}, V_{CCPGM}, and V_{CCPD} of the banks where the configuration and JTAG pins reside must be fully powered to the appropriate voltage levels to begin the configuration process.

When nCONFIG goes high, the device comes out of reset and releases the open-drain nSTATUS pin, which is then pulled high by an external 10-kΩ pull-up resistor. After nSTATUS is released, the device is ready to receive configuration data and the configuration stage begins. When nSTATUS is pulled high, the MAX II device places the configuration data one byte at a time on the DATA[7..0] pins.

☞ Stratix III devices receive configuration data on the DATA[7..0] pins and the clock is received on the DCLK pin. Data is latched into the device on the rising edge of DCLK. If you are using the Stratix III decompression feature, design security feature, or both, the configuration data is latched on the rising edge of every fourth DCLK cycle. After the configuration data is latched in, it is processed during the following three DCLK cycles.

Figure 12–3. Enabling Remote Update for Stratix III Devices in Compiler Settings

Configuration Image Types

When using a remote system upgrade, Stratix III device configuration bitstreams are classified as factory configuration images or application configuration images. An image, also referred to as a configuration, is a design loaded into the Stratix III device that performs certain user-defined functions.

Each Stratix III device in your system requires one factory configuration image or the addition of one or more application configuration images. The factory configuration image is a user-defined fall-back, or safe configuration, and is responsible for administering remote updates in conjunction with the dedicated circuitry. Application configuration images implement user-defined functionality in the target Stratix III device. You may include the default application configuration image functionality in the factory configuration image.

A remote system upgrade involves storing a new application configuration image or updating an existing one through the remote communication interface. After an application configuration image is stored or updated remotely, the user design in the Stratix III device initiates a reconfiguration cycle with the new image. Any errors during or after this cycle are detected by the dedicated remote system upgrade circuitry and cause the device to automatically revert to the factory configuration image. The factory configuration image then performs error processing and recovery. The factory configuration is written to the serial configuration device only once by the system manufacturer and should not be remotely updated. On the other hand, application configurations may be remotely updated in the system. Both images can initiate system reconfiguration.

Remote System Upgrade Mode

Remote system upgrade has one mode of operation: remote update mode. The remote update mode allows you to determine the functionality of your system upon power-up and offers different features.

In remote update mode, Stratix III devices load the factory configuration image upon power up. The user-defined factory configuration determines which application configuration is to be loaded and triggers a reconfiguration cycle. The factory configuration may also contain application logics.

When used with serial configuration devices, the remote update mode allows an application configuration to start at any flash sector boundary. This translates to a maximum of 128 pages in the EPCS64 device and 32 pages in the EPCS16 device, where the minimum size of each page is 512 KBits. Additionally, the remote update mode features a user watchdog timer that determines the validity of an application configuration.

Remote Update Mode

When a Stratix III device is first powered-up in remote update mode, it loads the factory configuration located at page zero (page registers `PGM[23:0] = 24'b0`). You should always store the factory configuration image for your system at page address zero. This corresponds to the start address location 0×000000 in the serial configuration device.

The factory configuration image is user-designed and contains soft logic to do the following:

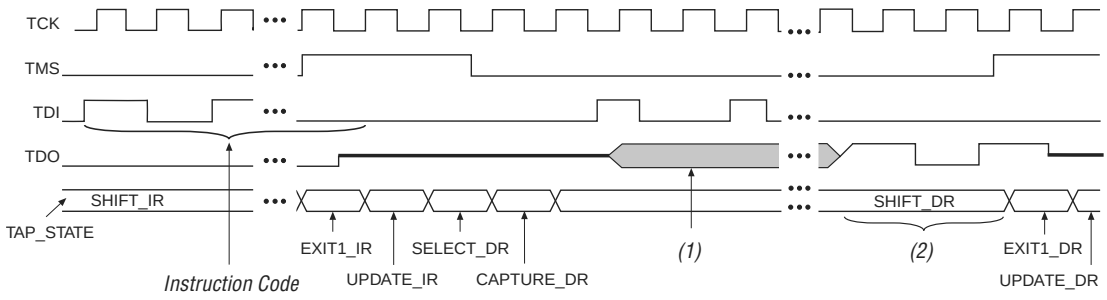
- Process any errors based on status information from the dedicated remote system upgrade circuitry
- Communicate with the remote host and receive new application configurations and store this new configuration data in the local non-volatile memory device
- Determine which application configuration is to be loaded into the Stratix III device
- Enable or disable the user watchdog timer and load its time-out value (optional)
- Instruct the dedicated remote system upgrade circuitry to initiate a reconfiguration cycle

Figure 12–4 shows the transitions between the factory and application configurations in remote update mode.

During the capture phase, multiplexers preceding the capture registers select the active device data signals. This data is then clocked into the capture registers. The multiplexers at the outputs of the update registers also select active device data to prevent functional interruptions to the device. During the shift phase, the boundary-scan shift register is formed by clocking data through the capture registers around the device periphery and then out of the TDO pin. The device can simultaneously shift new test data into TDI and replace the contents of the capture registers. During the update phase, data in the capture registers is transferred to the update registers. You can then use this data in the EXTEST instruction mode. Refer to "EXTEST Instruction Mode" on page 13–13 for more information.

Figure 13–9 shows the SAMPLE/PRELOAD waveforms. The SAMPLE/PRELOAD instruction code is shifted in through the TDI pin. The TAP controller advances to the CAPTURE_DR state and then to the SHIFT_DR state, where it remains if TMS is held low. The data that was present in the capture registers after the capture phase is shifted out of the TDO pin. New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register. If TMS is held high on two consecutive TCK clock cycles, the TAP controller advances to the UPDATE_DR state for the update phase.

Figure 13–9. SAMPLE/PRELOAD Shift Data Register Waveforms



Note to Figure 13–9:

(1) Data stored in boundary-scan register is shifted out of TDO.

(2) After boundary-scan register data has been shifted out, data entered into TDI will shift out of TDO.

Chapter Revision History

Table 13–8 lists the revision history for this chapter.

Table 13–8. Chapter Revision History

Date	Version	Changes Made
July 2010	1.9	Updated Table 13–1.
March 2010	1.8	Updated for the Quartus II software version 9.1 SP2 release: ■ Removed "IEEE Std. 1149.1 BST for Configured Devices" and "Conclusion" section. ■ Updated Table 13–5.
May 2009	1.7	■ Updated Table 13–1. ■ Updated "I/O Voltage Support in JTAG Chain" and "IEEE Std. 1149.1 BST Circuitry" sections.
February 2009	1.6	Removed "Referenced Documents" section.
October 2008	1.5	■ Updated Table 13–4. ■ Updated New Document Format.
May 2008	1.4	■ Updated Table 13–2 and Table 13–5 with EP3SL150ES information. ■ Updated Table 13–6. ■ Updated Figure 13–6.
November 2007	1.3	Updated Table 13–2.
October 2007	1.2	■ Added new section "Referenced Documents". ■ Added live links for references.
May 2007	1.1	■ Updated Note 3 to Table 13–3. Updated Figure 13–6. ■ Added Table 13–2, Table 13–4, Table 13–5, and Table 13–7. ■ Removed opening paragraph and footnote for "IEEE Std. 1149.1 BST Operation Control" on page 13–9. ■ Added warning on page 13-22.
November 2006	1.0	Initial Release.

Security Against Reverse Engineering

Reverse engineering from an encrypted configuration file is very difficult and time consuming because the Stratix III configuration file formats are proprietary and the file contains million of bits which require specific decryption. Reverse engineering the Stratix III device is just as difficult because the device is manufactured on the most advanced 65-nm process technology.

Security Against Tampering

The non-volatile keys are one-time programmable. Once the tamper protection bit is set in the key programming file generated by the Quartus® II software, the Stratix III device can only be configured with configuration files encrypted with the same key.

For more information about why this feature is secured, refer to the *Design Security in Stratix III Devices white paper*.

AES Decryption Block

The main purpose of the AES decryption block is to decrypt the configuration bitstream prior to entering data decompression or configuration.

Prior to receiving encrypted data, you must enter and store the 256-bit security key in the device. You can choose between a non-volatile security key and a volatile security key with battery backup.

The security key is scrambled prior to storing it in key storage in order to make it more difficult for anyone to retrieve the stored key using de-capsulation of the device.

Flexible Security Key Storage

Stratix III devices support two types of security key programming: volatile and non-volatile. Table 14–1 shows the differences between volatile keys and non-volatile keys.

Table 14–1. Security Keys Options

Options	Volatile Key	Non-Volatile Key
Key programmability	Reprogrammable and erasable	One-time programmable
External battery	Required	Not required
Key programming method *(1)*	On-board	On and off board
Design protection	Secure against copying and reverse engineering	Secure against copying and reverse engineering. Tamper resistant if tamper protection bit is set.

Note to Table 14–1:

(1) Key programming is carried out using JTAG interface.

You can program the non-volatile key to the Stratix III device without an external battery. Also, there are no additional requirements to any of the Stratix III power supply inputs.

17. Stratix III Device Packaging Information

SIII51017-1.7

This chapter provides thermal resistance values and package information for Altera® Stratix® III devices, including:

- "Thermal Resistance" on page 17–2
- "Package Outlines" on page 17–2

Table 17–1 lists which Stratix III device, are available in FineLine BGA or Hybrid FineLine BGA packages.

Table 17–1. FineLine and Hybrid FineLine BGA Packages for Stratix III Devices

Device	Package	Pins
EP3SL50	FineLine BGA - Flip Chip (Option 1)	484
	FineLine BGA - Flip Chip (Option 1)	780
EP3SL70	FineLine BGA - Flip Chip (Option 1)	484
	FineLine BGA - Flip Chip (Option 1)	780
EP3SL110	FineLine BGA - Flip Chip (Option 1)	780
	FineLine BGA - Flip Chip (Option 1)	1152
EP3SL150	FineLine BGA - Flip Chip (Option 1)	780
	FineLine BGA - Flip Chip (Option 1)	1152
EP3SL200	Hybrid FineLine BGA - Flip Chip (Option 1)	780
	FineLine BGA - Flip Chip (Option 1)	1152
	FineLine BGA - Flip Chip (Option 1)	1517
EP3SL340	Hybrid FineLine BGA - Flip Chip (Option 1)	1152
	FineLine BGA - Flip Chip (Option 1)	1517
	FineLine BGA - Flip Chip (Option 1)	1760
EP3SE50	FineLine BGA - Flip Chip (Option 1)	484
	FineLine BGA - Flip Chip (Option 1)	780
EP3SE80	FineLine BGA - Flip Chip (Option 1)	780
	FineLine BGA - Flip Chip (Option 1)	1152
EP3SE110	FineLine BGA - Flip Chip (Option 1)	780
	FineLine BGA - Flip Chip (Option 1)	1152
EP3SE260	Hybrid FineLine BGA - Flip Chip (Option 1)	780
	FineLine BGA - Flip Chip (Option 1)	1152
	FineLine BGA - Flip Chip (Option 1)	1517