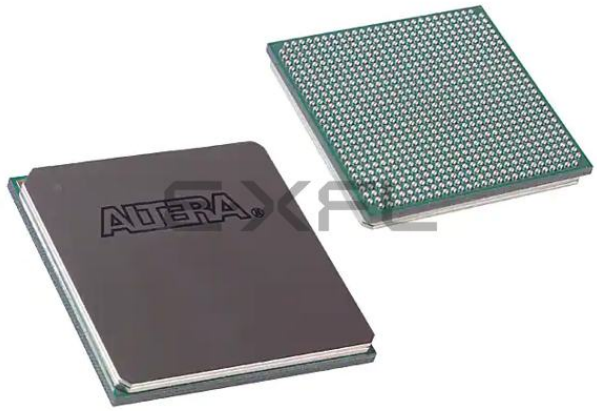

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1900
Number of Logic Elements/Cells	47500
Total RAM Bits	5760000
Number of I/O	488
Number of Gates	-
Voltage - Supply	0.86V ~ 1.15V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep3se50f780c3n

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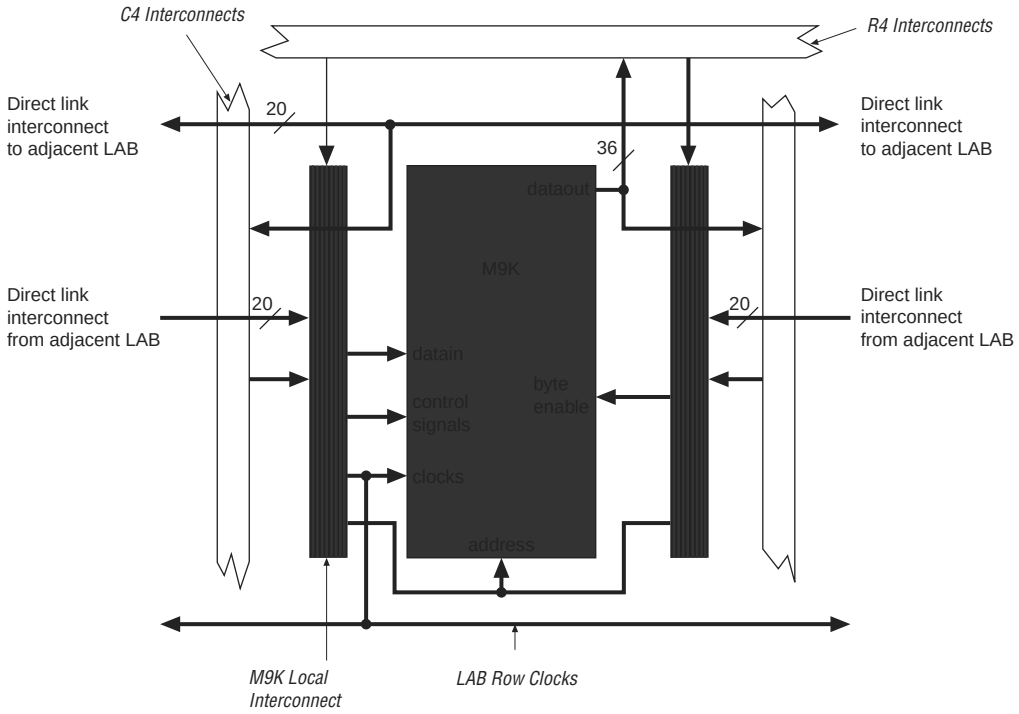
Figure 3–5. M9K RAM Block LAB Row Interface



The M144K blocks use eight interfaces in the same device column. The M144K block local interconnects are driven by R4, C4, and direct link interconnects from adjacent LABs on either the right or left side of the MRAM block. Up to 20 direct link input connections to the M144K block are possible from the left adjacent LABs and another 20 possible from the right adjacent LAB. M144K block outputs can also connect to the LABs on the block's left and right sides through direct link interconnect. Figure 3–6 shows the interface between the M144K RAM block and the logic array.

Figure 4–3 shows an address clock enable block diagram. The address clock enable is referred to by the port name `addressstall`.

Figure 4–3. Stratix III Address Clock Enable Block Diagram

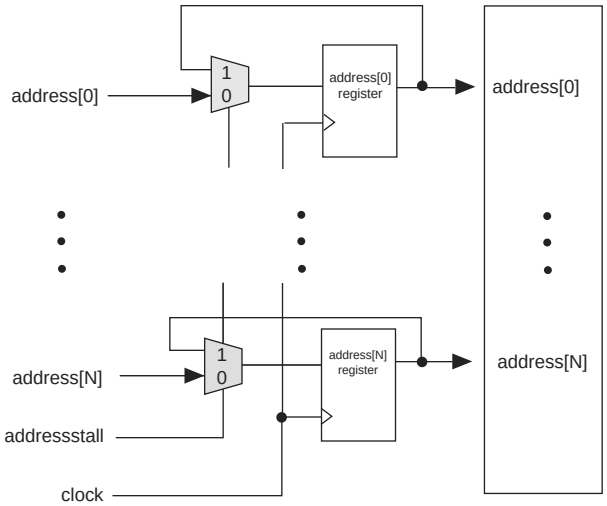


Figure 4–4 shows the address clock enable waveform during the read cycle.

Figure 4–4. Stratix III Address Clock Enable during Read Cycle Waveform

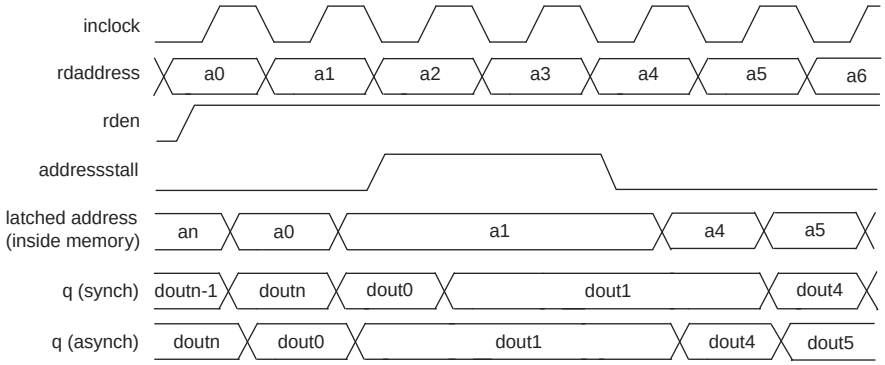
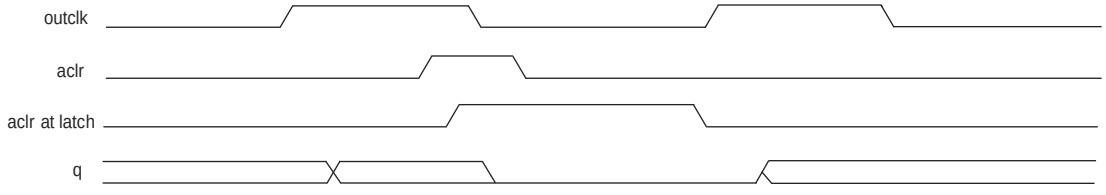


Figure 4–7. Output Latch Asynchronous Clear Waveform



You can selectively enable asynchronous clears per logical memory via the Quartus II RAM MegaWizard Plug-In Manager.

For more information, refer to the *RAM Megafunction User Guide*.

Error Correction Code Support

Stratix III M144K blocks have built-in support for error correction code (ECC) when in ×64-wide simple dual-port mode. ECC allows you to detect and correct data errors in the memory array. The M144K blocks have a single-error-correction double-error-detection (SECDED) implementation. SECDED can detect and fix a single-bit error in a 64-bit word or detect two-bit errors in a 64-bit word. It cannot detect three or more errors.

The M144K ECC status is communicated via a three-bit status flag `eccstatus[2..0]`. The status flag can be either registered or unregistered. When registered, it uses the same clock and asynchronous clear signals as the output registers. When not registered, it cannot be asynchronously cleared.

Table 4–3 shows the truth table for the ECC status flags.

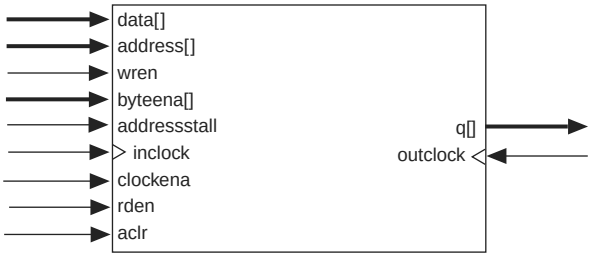
Table 4–3. Truth Table for ECC Status Flags

Status	eccstatus[2]	eccstatus[1]	eccstatus[0]
No error	0	0	0
Single error and fixed	0	1	1
Double error and no fix	1	0	1
Illegal	0	0	1
Illegal	0	1	0
Illegal	1	0	0
Illegal	1	1	X

You cannot use the byte-enable feature when ECC is engaged.

Read during write “old data” mode is not supported when ECC is engaged.

Figure 4–9. Single-Port Memory *(Note 1)*



Note to Figure 4–9:

(1) You can implement two single-port memory blocks in a single M9K or M144K block. See "Packed Mode Support" on page 4–5 for more details.

During a write operation, behavior of the RAM outputs is configurable. If you use the read-enable signal and perform a write operation with the read enable deactivated, the RAM outputs retain the values they held during the most recent active read enable. If you activate read enable during a write operation, or if you are not using the read-enable signal at all, the RAM outputs either show the new data being written, the old data at that address, or a don't care value. To choose the desired behavior, set the read-during-write behavior to either new data, old data, or don't care in the RAM MegaWizard Plug-In Manager in the Quartus II software. See "Read During Write" on page 4–21 for more details on this behavior.

Table 4–4 shows the possible port width configurations for TriMatrix memory blocks in single-port mode.

Table 4–4. Stratix III Port Width Configurations for MLABs, M9K Blocks, and M144K Blocks (Single-Port Mode)

Port Width	MLABs *(1)*	M9K Blocks	M144K Blocks
Port Width Configurations	16 × 8	8 K × 1	16 K × 8
	16 × 9	4 K × 2	16 K × 9
	16 × 10	2 K × 4	8 K × 16
	16 × 16	1 K × 8	8 K × 18
	16 × 18	1 K × 9	4 K × 32
	16 × 20	512 × 16	4 K × 36
		512 × 18	2 K × 64
		256 × 32	2 K × 72
		256 × 36	

Note to Table 4–4:

(1) Configurations of 64 × 8, 64 × 9, 64 × 10, 32 × 16, 32 × 18, and 32 × 20 are supported by stitching multiple MLAB blocks.

Figure 5–18. Four-Multiplier Adder Mode for Half-DSP Block

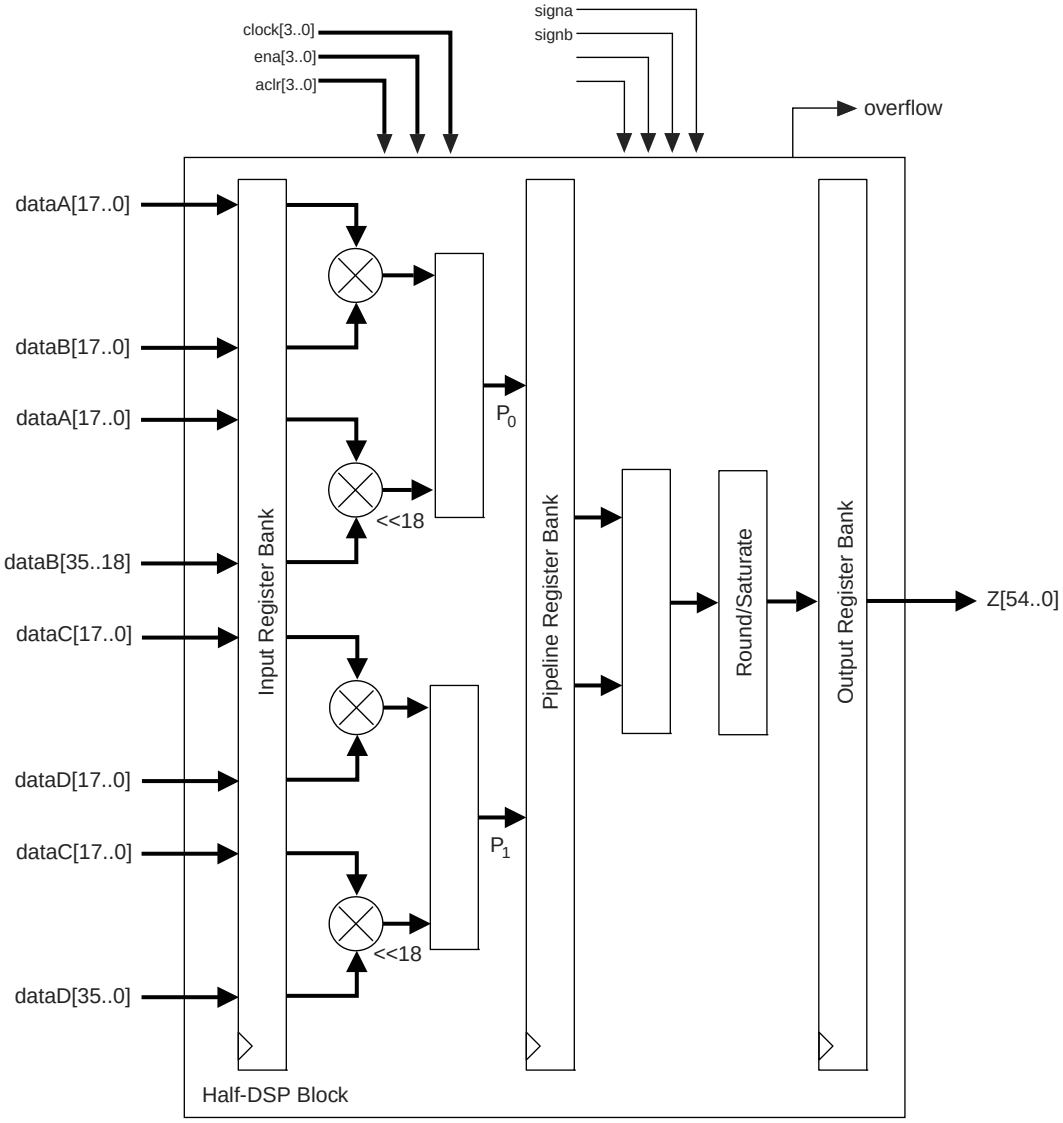


Table 5–7. Comparison of Round-to-Nearest-Integer and Round-to-Nearest-Even

Round-To-Nearest-Integer	Round-To-Nearest-Even
010111 ⇒0110	010111 ⇒0110
001101 ⇒0011	001101 ⇒0011
001010 ⇒0011	001010 ⇒0010
001110 ⇒0100	001110 ⇒0100
110111 ⇒1110	110111 ⇒1110
101101 ⇒1011	101101 ⇒1011
110110 ⇒1110	110110 ⇒1110
110010 ⇒1101	110010 ⇒1100

Two saturation modes are supported in Stratix III:

- Asymmetric saturation mode
- Symmetric saturation mode

You must select one of the two options at compile time.

In 2's complement format, the maximum negative number that can be represented is $-2^{(n-1)}$ while the maximum positive number is $2^{(n-1)}-1$. Symmetrical saturation will limit the maximum negative number to $-2^{(n-1)} + 1$. For example, for 32 bits:

- Asymmetric 32-bit saturation: Max = 0x7FFFFFFF, Min = 0x80000000
- Symmetric 32-bit saturation: Max = 0x7FFFFFFF, Min = 0x80000001

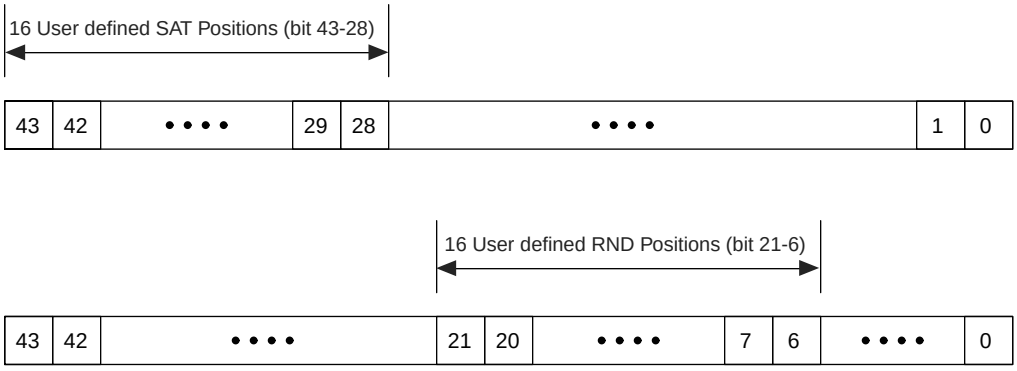
Table 5–8 lists how the saturation works. In this example, a 44-bit input is saturated to 36-bits.

Table 5–8. Examples of Saturation

44 to 36 Bits Saturation	Symmetric SAT Result	Asymmetric SAT Result
5926AC01342h	7FFFFFFFh	7FFFFFFFh
ADA38D2210h	800000001h	800000000h

Stratix III devices have up to 16 configurable bit positions out of the 44-bit bus ([43:0]) for the round and saturate logic unit providing higher flexibility. You must select the 16 configurable bit positions at compile time. These 16-bit positions are located at bits [21:6] for rounding and [43:28] for saturation, as shown in Figure 5–21.

Figure 5–21. Round and Saturation Locations



For symmetric saturation, the RND bit position is also used to determine where the LSP for the saturated data is located.

You can use the rounding and saturation function described above in regular supported multiplication operations as specified in Table 5–2. However, for accumulation type operations, the following convention is used.

The functionality of the round logic unit is in the format of:

Result = RND[S(A × B)], when used for an accumulation type of operation.

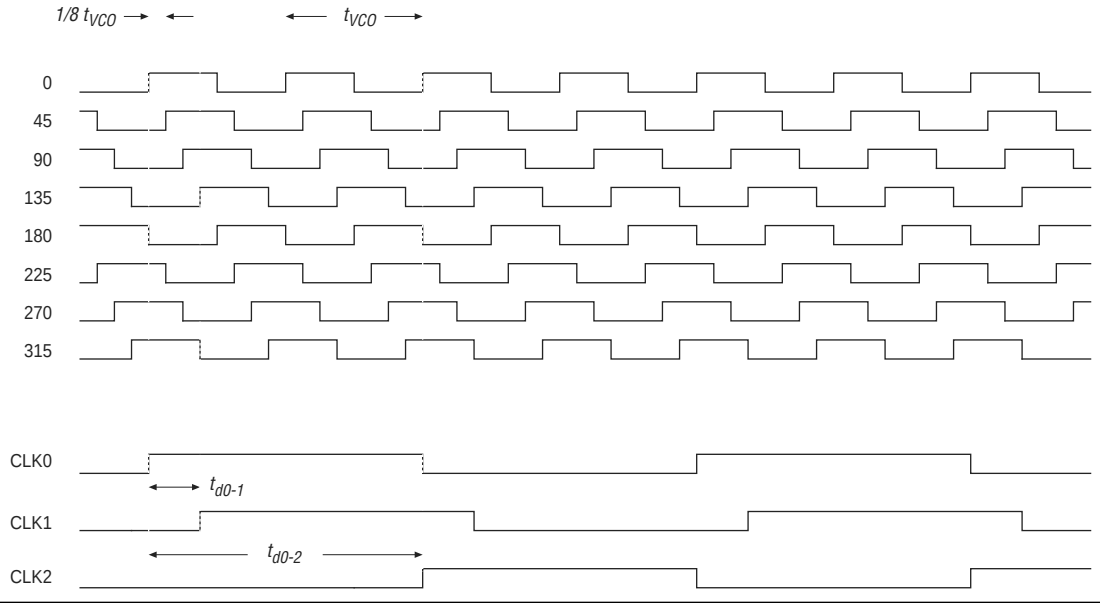
Likewise, the functionality of the saturation logic unit is in the format of:

Result = SAT[S(A × B)], when used for an accumulation type of operation.

If both the round and saturation logic units are used for an accumulation type of operation, the format is:

Result = SAT[RND[S(A × B)]]

Figure 6–39. Delay Insertion Using VCO Phase Output and Counter Delay Time



You can use the coarse- and fine-phase shifts to implement clock delays in Stratix III devices.

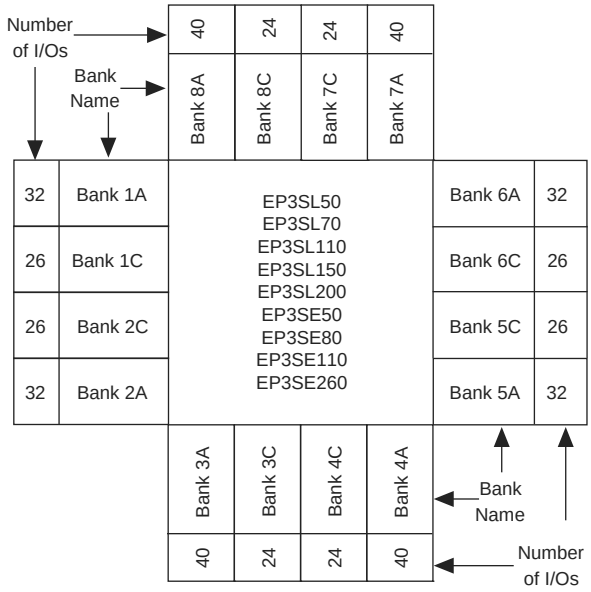
Stratix III devices support dynamic phase-shifting of VCO phase taps only. The phase shift is reconfigurable any number of times, and each phase shift takes about one SCANCLK cycle, allowing you to implement large phase shifts quickly.

PLL Reconfiguration

PLLs use several divide counters and different VCO phase taps to perform frequency synthesis and phase shifts. In Stratix III PLLs, you can reconfigure both the counter settings and phase-shift the PLL output clock in real time. You can also change the charge pump and loop-filter components, which dynamically affects the PLL bandwidth. You can use these PLL components to update the output-clock frequency and the PLL bandwidth and to phase-shift in real time, without reconfiguring the entire Stratix III device.

The ability to reconfigure the PLL in real time is useful in applications that operate at multiple frequencies. It is also useful in prototyping environments, allowing you to sweep PLL output frequencies and adjust the output-clock phase dynamically. For example, a system generating test patterns is required to generate and transmit patterns at 75 or 150 MHz, depending on the requirements of the device under test. Reconfiguring the PLL components in real time allows you to switch between two such output frequencies within a few microseconds. You can also use this feature to adjust clock-to-out (t_{co}) delays in real time by changing the PLL output clock phase shift. This approach eliminates the need to regenerate a configuration file with the new PLL settings.

Figure 7–3. Number of I/Os in Each Bank in the 780-pin FineLine BGA Package *(Note 1)*, *(2)*, *(3)*, *(4)*



Notes to Figure 7–3:

(1) All I/O pin counts include dedicated clock inputs pins. The pin count includes all general purpose I/O, dedicated clock pins, and dual-purpose configuration pins. Dedicated configuration pins are not included in the pin count.

(2) Figure 7–3 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

(3) Number of I/Os in each Bank in EP3SL50,EP3SL70, EP3SL110, EP3SL150, EP3SE50, EP3SE80 and EP3SE110 in the 780-pin FineLine BGA package.

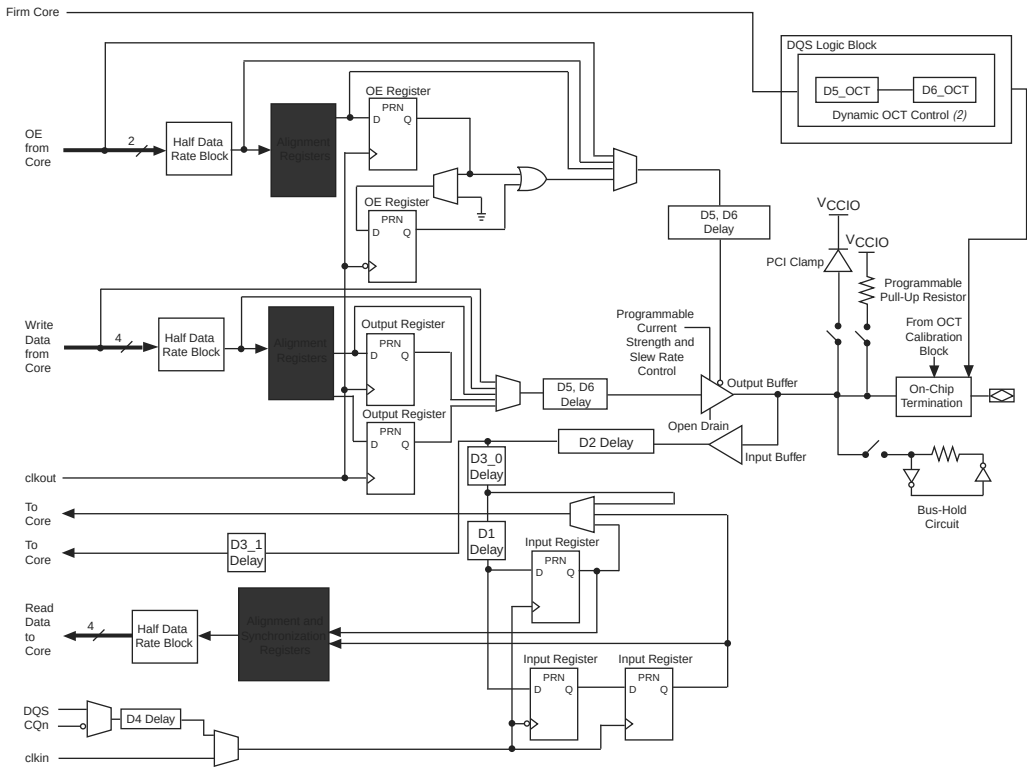
(4) Number of I/Os in each Bank in EP3SL200 and EP3SE260 in the 780-pin Hybrid FineLine BGA package.

- On-chip series termination without calibration
- On-chip parallel termination with calibration (OCT R_T)
- On-chip differential termination (OCT R_D)
- PCI clamping diode

The I/O registers are composed of the input path for handling data from the pin to the core, the output path for handling data from the core to the pin, and the output-enable (OE) path for handling the OE signal for the output buffer. These registers allow faster source-synchronous register-to-register transfers and resynchronization. The input path consists of the DDR input registers, alignment and synchronization registers, and HDR. You can bypass each block of the input path.

Figure 7–7 shows the Stratix III IOE structure.

Figure 7–7. IOE Structure for Stratix III Devices *(Note 1)*, *(2)*



Notes to Figure 7–7:

(1) `D3_0` and `D3_1` delays have the same available settings in the Quartus® II software.

(2) One dynamic OCT control is available per DQ/DQS group.

The output and OE paths are divided into output or OE registers, alignment registers, and HDR blocks. You can bypass each block of the output and OE path.

For more information about I/O registers and how they are used for memory applications, refer to the *External Memory Interfaces in Stratix III Devices* chapter.

Bus Hold

Each Stratix III device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can weakly hold the signal on an I/O pin at its last-driven state. Because the bus-hold feature holds the last-driven state of the pin until the next input signal is present, you do not need an external pull-up or pull-down resistor to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls non-driven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than V_{CCIO} to prevent over-driving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. Disable the bus-hold feature if the I/O pin is configured for differential signals.

The bus-hold circuitry uses a resistor with a nominal resistance (R_{BH}) of approximately 7 kΩ to weakly pull the signal level to the last-driven state.

For the specific sustaining current driven through this resistor and the overdrive current used to identify the next-driven input level, refer to the *DC and Switching Characteristics of Stratix III Devices* chapter. This information is provided for each V_{CCIO} voltage level.

The bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

Programmable Pull-Up Resistor

Each Stratix III device I/O pin provides an optional programmable pull-up resistor during user mode. If you enable this feature for an I/O pin, the pull-up resistor (typically 25 kΩ) weakly holds the I/O to the V_{CCIO} level.

Programmable pull-up resistors are only supported on user I/O pins and are not supported on dedicated configuration pins, JTAG pins, or dedicated clock pins. If the programmable pull-up option is enabled, you cannot use the bus-hold feature.

When the optional `DEV_OE` signal drives low, all I/O pins remain tri-stated even with programmable pull-up option enabled.

Programmable Pre-Emphasis

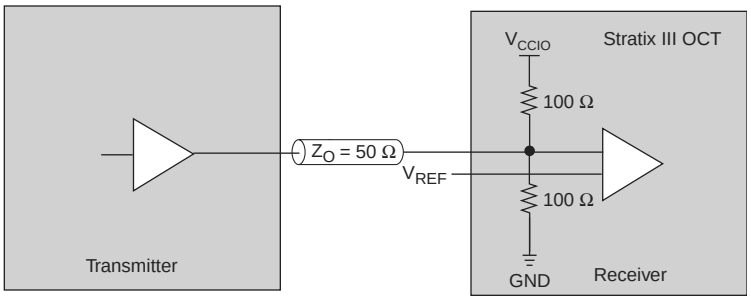
Stratix III LVDS transmitters support programmable pre-emphasis to compensate for the frequency dependent attenuation of the transmission line. The Quartus II software allows four settings for programmable pre-emphasis—zero, low, medium, and high. The default setting is low.

For more information about programmable pre-emphasis, refer to the *High-Speed Differential I/O Interfaces with DPA* in the *Stratix III Devices* chapter.

On-Chip Parallel Termination with Calibration

Stratix III devices support OCT R_T with calibration in all banks. OCT R_T with calibration is only supported for input or bi-directional pin configurations. For input pins, you can enable OCT R_T continuously. However, for bi-directional I/O, OCT R_T is enabled or disabled depending on whether or not the bi-directional I/O acts as a transmitter or receiver. Output pin configurations do not support OCT R_T with calibration. Figure 7–10 shows OCT R_T with calibration. When OCT R_T is used, the V_{CCIO} of the bank has to match the I/O standard of the pin where the parallel OCT is enabled.

Figure 7–10. On-Chip Parallel Termination with Calibration for Stratix III Devices



The OCT R_T calibration circuit compares the total impedance of the I/O buffer to the external 50-Ω ±1% resistors connected to the RUP and RDN pins and dynamically enables or disables the transistors until they match. Calibration occurs at the end of device configuration. When the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers. Table 7–10 lists the I/O standards that support OCT R_T with calibration.

Table 7–10. Selectable I/O Standards that Support On-Chip Parallel Termination with Calibration

I/O Standard	On-Chip Parallel Termination Setting (Column I/O)	On-Chip Parallel Termination Setting (Row I/O)	Unit
SSTL-2 Class I, II	50	50	Ω
SSTL-18 Class I, II	50	50	Ω
SSTL-15 Class I, II	50	50	Ω
HSTL-18 Class I, II	50	50	Ω
HSTL-15 Class I, II	50	50	Ω
HSTL-12 Class I, II	50	50	Ω
Differential SSTL-2 Class I, II	50	50	Ω
Differential SSTL-18 Class I, II	50	50	Ω
Differential SSTL-15 Class I, II	50	50	Ω
Differential HSTL-18 Class I, II	50	50	Ω
Differential HSTL-15 Class I, II	50	50	Ω
Differential HSTL-12 Class I, II	50	50	Ω

User Mode

During user mode, OCTUSRCLK, ENAOCT, nCLRUSR, and ENASER[9..0] signals are used to calibrate and serially transfer calibrated codes from each OCT calibration block to any I/O. Table 7–12 lists the user controlled calibration block signal names and their descriptions.

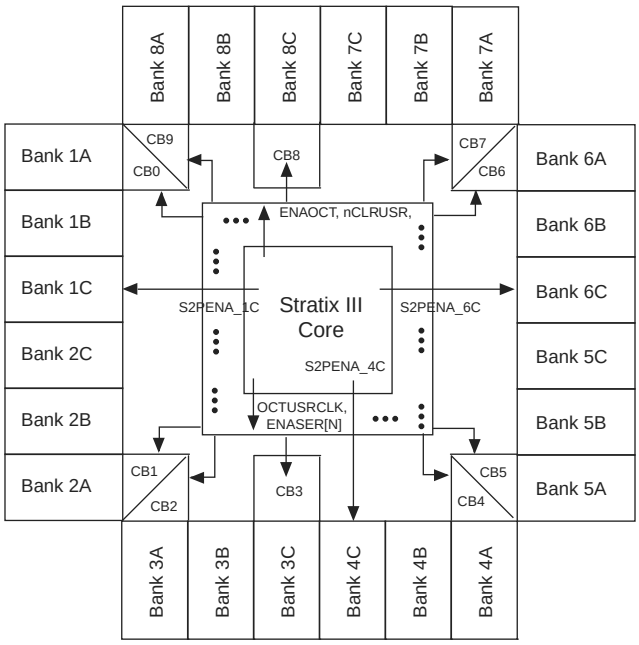
Table 7–12. OCT Calibration Block Ports for User Control and Description

Signal Name	Description
OCTUSRCLK	Clock for OCT block.
ENAOCT	Enable OCT Termination (generated by user IP).
ENASER[9..0]	When ENAOCT = 0, each signal enables the OCT serializer for the corresponding OCT calibration block. When ENAOCT = 1, each signal enables OCT calibration for the corresponding OCT calibration block.
S2PENA_<*bank#*>	Serial-to-parallel load enable per I/O bank.
nCLRUSR	Clear user.

Figure 7–17 shows the flow of the user signal. When ENAOCT is 1, all OCT calibration blocks are in calibration mode, and when ENAOCT is 0, all OCT calibration blocks are in serial data transfer mode. The OCTUSRCLK clock frequency must be 20 MHz or less.

☞ You must generate all user signals on the rising edge of OCTUSRCLK.

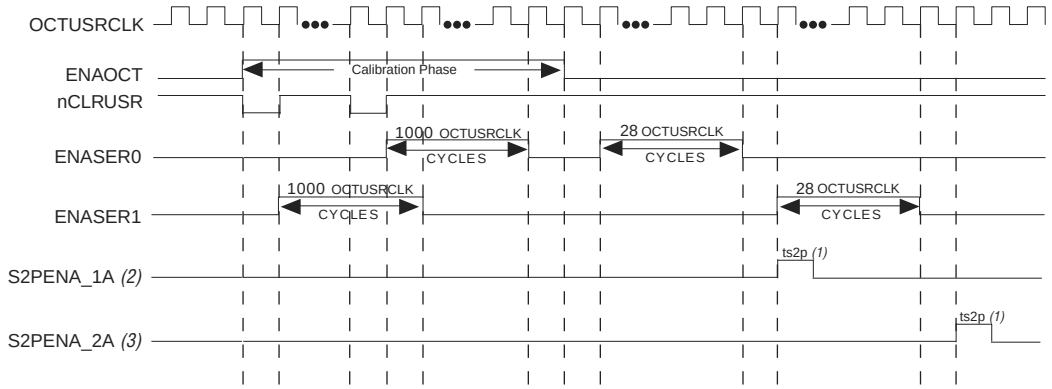
Figure 7–17. Signals Used for User Mode Calibration *(Note 1)*



Note to Figure 7–17:

(1) Figure 7–17 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

Figure 7–19. OCT User-Mode Signal Timing Waveform for Two OCT Blocks



Notes to Figure 7–19:

(1) ts2p ≥ 25 ns

(2) S2PENA_1A is asserted in Bank 1A for calibration block 0.

(3) S2PENA_2A is asserted in Bank 2A for calibration block 1.

RS Calibration

If only RS calibration is used for an OCT calibration block, its corresponding ENASER signal must be asserted for 240 OCTUSRCLK cycles for calibration.

You still have to assert the ENASER signal for 28 OCTUSRCLK cycles for serial transfer.

For more information, refer to the *ALT_OCT Megafunction User Guide* and *AN 465: Implementing OCT Calibration in Stratix III Devices*.

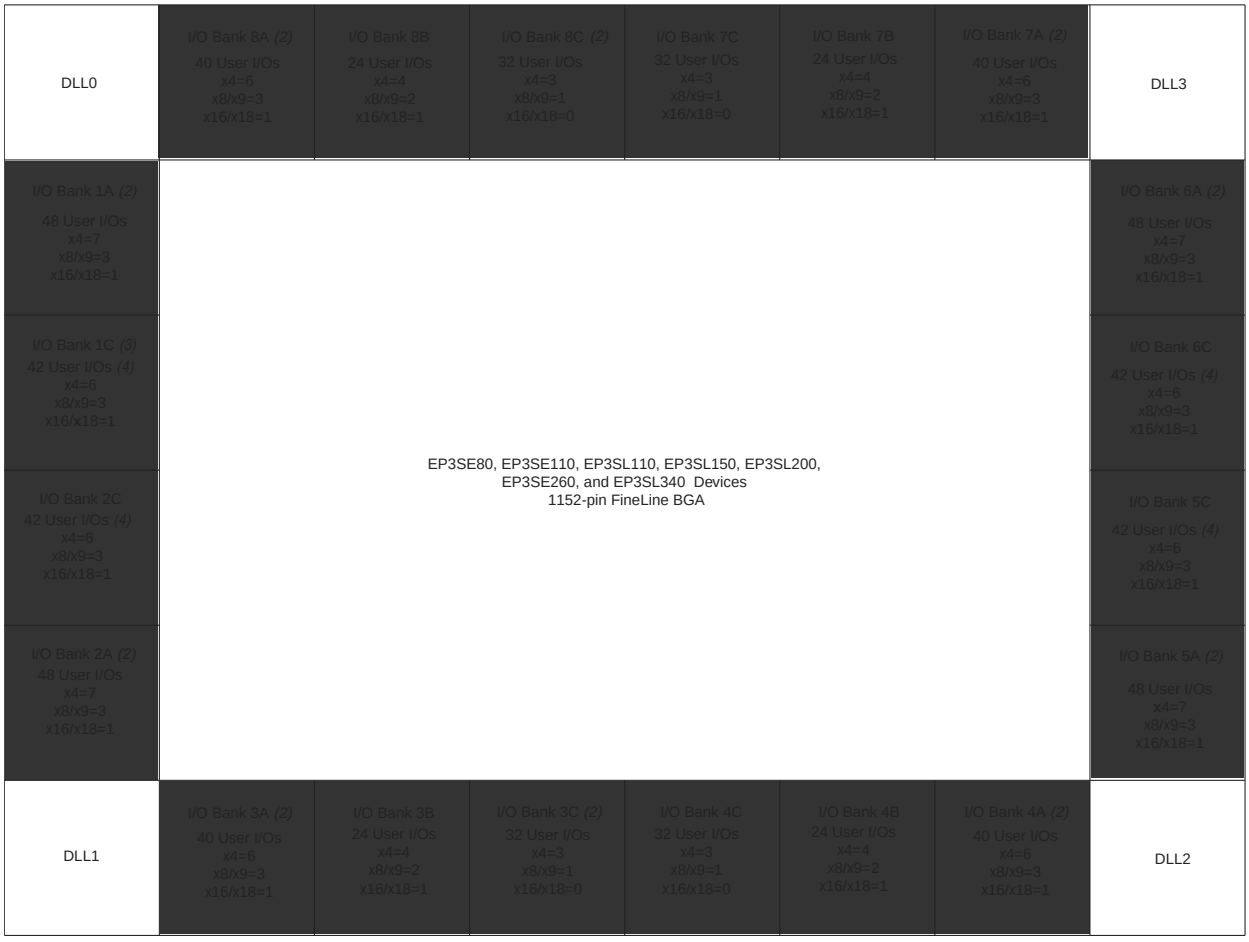
Termination Schemes for I/O Standards

The following section describes the different termination schemes for the I/O standards used in Stratix III devices.

Single-Ended I/O Standards Termination

Voltage-referenced I/O standards require both an input reference voltage, V_{REF}, and a termination voltage (V_{TT}). The reference voltage of the receiving device tracks the termination voltage of the transmitting device. Figure 7–20 and Figure 7–21 show the details of SSTL and HSTL I/O termination on Stratix III devices.

Figure 8–5. Number of DQS/DQ Groups in EP3SE80, EP3SE110, EP3SL110, EP3SL150, EP3SL200, EP3SE260, and EP3SL340 Devices in the 1152-pin FineLine BGA Package *(Note 1)*



Notes to Figure 8–5:

(1) This device does not support ×32/×36 mode.

(2) You can also use DQS/DQSn pins in some of the ×4 groups as RUP/RDN pins. You cannot use a ×4 group for memory interfaces if two pins of the group are being used as RUP and RDN pins for OCT calibration. You can still use the ×16/×18 or ×32/×36 groups that includes these ×4 groups. However, there are restrictions on using ×8/×9 groups that include these ×4 groups as described on page 8–5.

(3) Some of the DQS/DQ pins in this bank can also be used as configuration pins. Choose the DQS/DQ pins that are not going to be used by your configuration scheme.

(4) All I/O pin counts include eight dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n, CLK8p, CLK8n, CLK10p, and CLK10n).

Source-Synchronous Timing Budget

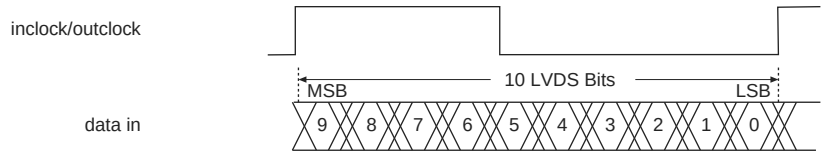
This section discusses the timing budget, waveforms, and specifications for source-synchronous signaling in Stratix III devices. LVDS I/O standards enable high-speed data transmission. This high data transmission rate results in better overall system performance. To take advantage of fast system performance, it is important to understand how to analyze timing for these high-speed signals. Timing analysis for the differential block is different from traditional synchronous timing analysis techniques.

Rather than focusing on clock-to-output and setup times, source synchronous timing analysis is based on the skew between the data and the clock signals. High-speed differential data transmission requires the use of timing parameters provided by IC vendors and is strongly influenced by board skew, cable skew, and clock jitter. This section defines the source-synchronous differential data orientation timing parameters, the timing budget definitions for Stratix III devices, and ways to use these timing parameters to determine the maximum performance of your design.

Differential Data Orientation

There is a set relationship between an external clock and the incoming data. For an operation at 1 Gbps and SERDES factor of 10, the external clock is multiplied by 10, and phase-alignment can be set in the PLL to coincide with the sampling window of each data bit. The data is sampled on the falling edge of the multiplied clock. Figure 9–15 shows the data bit orientation of the ×10 mode.

Figure 9–15. Bit Orientation in Quartus II Software



Differential I/O Bit Position

Data synchronization is necessary for successful data transmission at high frequencies. Figure 9–16 shows the data bit orientation for a channel operation. These figures are based on the following:

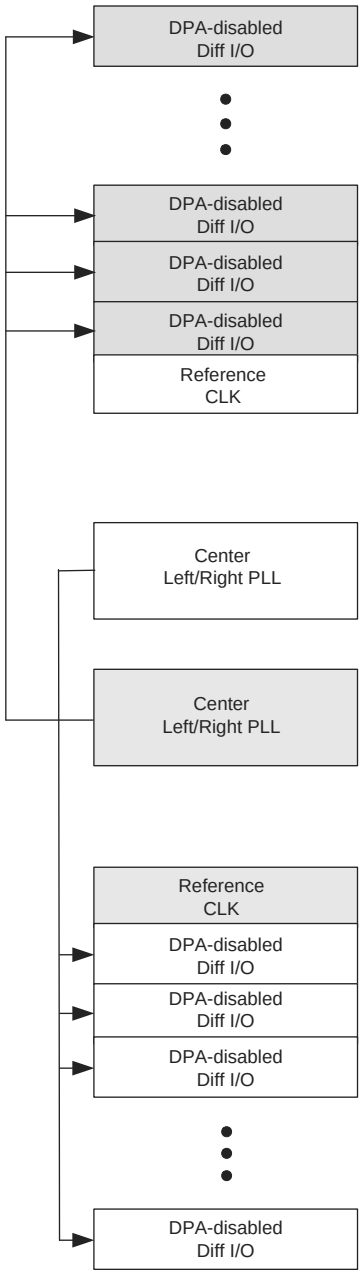
- SERDES factor equals clock multiplication factor
- Edge alignment is selected for phase alignment
- Implemented in hard SERDES

For other serialization factors, use the Quartus II software tools and find the bit position within the word and the bit positions after deserialization.

Using Both Center Left/Right PLLs

Both center left/right PLLs can be used simultaneously to drive DPA-disabled channels on upper and lower differential banks. Unlike DPA-enabled channels, the center left/right PLLs can drive cross-banks. For example, the upper center left/right PLL can drive the lower differential bank at the same time the lower center left/right PLL is driving the upper differential bank and vice versa, as shown in Figure 9–23.

Figure 9–23. Both Center Left/Right PLLs Driving Cross-Bank DPA-Disabled Channels Simultaneously



Chapter Revision History

Table 12–7 lists the revision history for this chapter.

Table 12–7. Chapter Revision History

Date	Version	Changes Made
March 2010	1.5	Updated for the Quartus II version 9.1 SP2 release: ■ Updated "Remote System Upgrade State Machine" and "User Watchdog Timer" sections. ■ Updated Table 12–6. ■ Updated Figure 12–1. ■ Removed "Conclusion" section. ■ Minor text edits.
February 2009	1.4	Removed "Referenced Documents" section.
October 2008	1.3	■ Updated "Introduction" section. ■ Updated New Document Format.
October 2007	1.2	■ Added new section "Referenced Documents". ■ Added live links for references.
May 2007	1.1	■ Minor text edits to page 4 and 5. ■ Changes to Figure 12–2. Added Figure 12–3. Added a note to Figure 12–5. Added Figure 12–8. ■ Added new section, "Enabling Remote Update" on page 12–4. ■ Removed references to "Remote System Upgrade atom" and section of same title. Removed "Interface Signals Between Remote System Upgrade Circuitry and Stratix III Device Logic Array" section. Removed Table titled "Interface Signals between Remote System Upgrade Circuitry and Stratix III Device Logic Array." Removed footnote, table titled "Input Ports of the altremote_update Megafunction," table titled "Output Ports of the altremote_update Megafunction," and table titled "Parameter Settings for the altremote_update Megafunction" in section "altremote_update Megafunction" on page 12–15. Removed "System Design Guidelines Using Remote System Upgrade With Serial Configuration Devices" section.
November 2006	1.0	Initial Release.

Thermal Resistance

For Stratix III devices thermal resistance specifications, refer to the *Stratix Series Device Thermal Resistance Data Sheet*.

Package Outlines

You can download Stratix III device package outlines from the *Device Packaging Specifications* web page.

Chapter Revision History

Table 17–2 lists the revision history for this chapter.

Table 17–2. Chapter Revision History

Date	Version	Changes Made
March 2010	1.7	Updated for the Quartus II software version 9.1 SP2 release: ■ Updated Table 17–1. ■ Minor text edits.
February 2009	1.6	Removed "Referenced Documents" section.
October 2008	1.5	Updated New Document Format.
May 2008	1.4	Updated "Package Outlines" section hyperlink.
November 2007	1.3	Updated Table 17–1.
October 2007	1.2	■ Added new section "Referenced Documents". ■ Added live links for references.
May 2007	1.1	Removed thermal resistance and package outline information and replaced with links referencing this information.
November 2006	1.0	Initial Release.