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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3200
Number of Logic Elements/Cells	80000
Total RAM Bits	6843392
Number of I/O	744
Number of Gates	-
Voltage - Supply	0.86V ~ 1.15V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep3se80f1152c3n

Chapter 3. MultiTrack Interconnect in Stratix III Devices

Chapter 4. TriMatrix Embedded Memory Blocks in Stratix III Devices

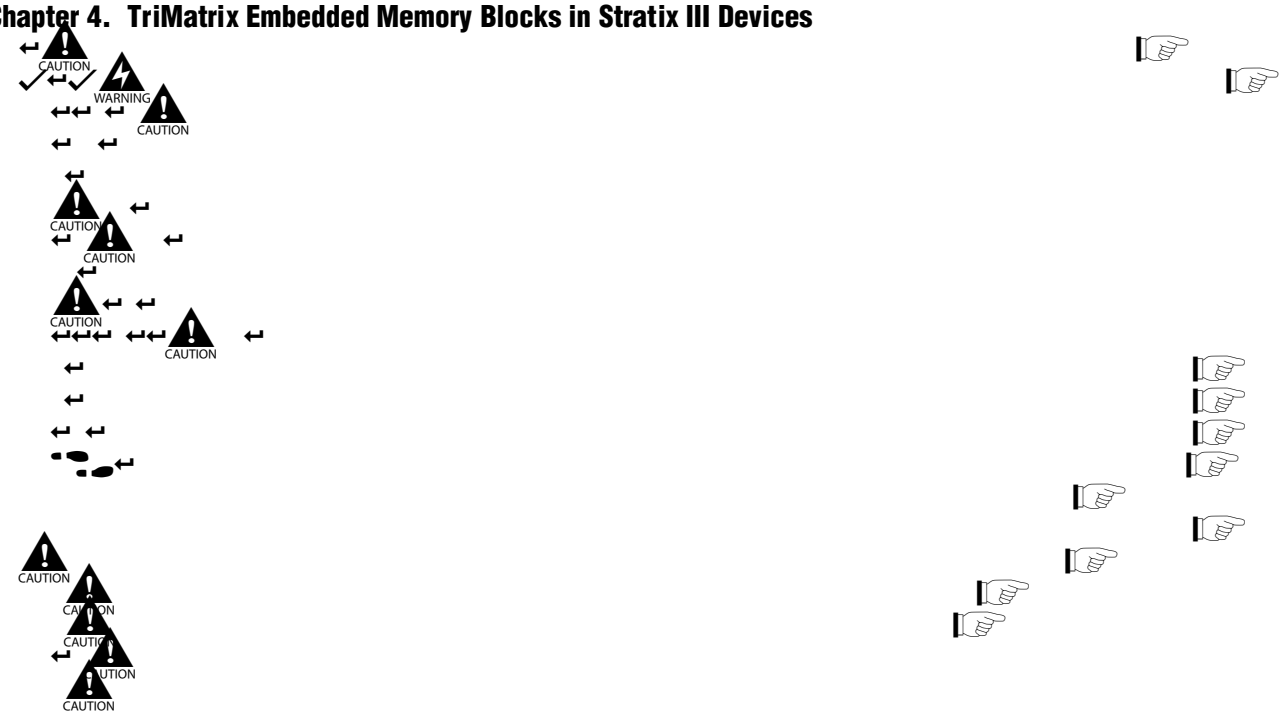


Table 7 5. Programmable Current Strength (Note 1)

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA) for Column I/O Pins	I_{OH} / I_{OL} Current Strength Setting (mA) for Row I/O Pins
3.3-V LVTTL	16, 12, 8, 4	12, 8, 4
3.3-V LVCMOS	16, 12, 8, 4	8, 4
3.0-V LVTTL	16, 12, 8, 4	12, 8, 4
3.0-V LVCMOS	16, 12, 8, 4	8, 4
2.5-V LVTTL/LVCMOS	16, 12, 8, 4	12, 8, 4
1.8-V LVTTL/LVCMOS	12, 10, 8, 6, 4, 2	8, 6, 4, 2
1.5-V LVTTL/LVCMOS	12, 10, 8, 6, 4, 2	8, 6, 4, 2
1.2-V LVTTL/LVCMOS	8, 6, 4, 2	4, 2
SSTL-2 Class I	12, 10, 8	12, 8
SSTL-2 Class II	16	16
SSTL-18 Class I	12, 10, 8, 6, 4	12, 10, 8, 6, 4
SSTL-18 Class II	16, 8	16, 8
SSTL-15 Class I	12, 10, 8, 6, 4	8, 6, 4
SSTL-15 Class II	16, 8	
HSTL-18 Class I	12, 10, 8, 6, 4	12, 10, 8, 6, 4
HSTL-18 Class II	16	16
HSTL-15 Class I	12, 10, 8, 6, 4	8, 6, 4
HSTL-15 Class II	16	
HSTL-12 Class I	12, 10, 8, 6, 4	8, 6, 4
HSTL-12 Class II	16	

Note to Table 7–5

(1) The default setting in the Quartus II software is 50 Ω R_S without calibration for all non-voltage reference and HSTL/SSTL class I I/O standards. The default setting is 25 Ω R_S without calibration for HSTL/SSTL class II I/O standards.

Altera recommends performing IBIS or SPICE simulations to determine the right current strength setting for your specific application.

Programmable Slew Rate Control

The output buffer for each Stratix III device regular- and dual-function I/O pin has a programmable output slew-rate control that you can configure for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. A slow slew rate can help reduce system noise, but adds a nominal delay to rising and falling edges. Each I/O pin has an individual slew-rate control, allowing you to specify the slew rate on a pin-by-pin basis.

1 You cannot use the programmable slew rate feature when using OCT R_S.

The Quartus II software allows four settings for programmable slew rate control 0, 1, 2, and 3 where 0 is slow slew rate and 3 is fast slew rate. Table 7 6 lists the default setting for the I/O standards supported in the Quartus II software.

Memory Clock Pins

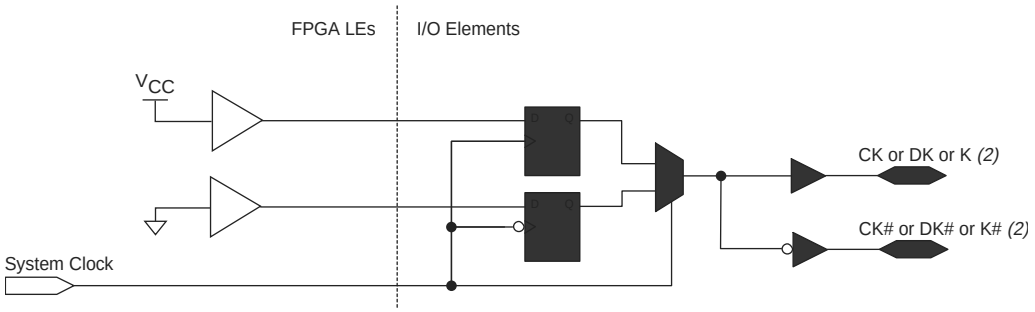
In addition to DQS (and CQn) signals to capture data, DDR3, DDR2, DDR SDRAM, and RLDRAM II use an extra pair of clocks, called CK and CK# signals, to capture the address and control/command signals. The CK/CK# signals must be generated to mimic the write data-strobe using Stratix III DDR I/O registers (DDIOs) to ensure that timing relationships between the CK/CK# and DQS signals (t_{DQSS} in DDR3, DDR2, and DDR SDRAM or t_{CKDK} in RLDRAM II) are met. QDR II+ and QDR II SRAM devices use the same clock (K/K#) to capture data, address, and control/command signals.

Memory clock pins in Stratix III devices are generated with a DDIO register going to differential output pins, marked in the pin table with DIFFOUT, DIFFIO_TX, and DIFFIO_RX prefixes.

f For more information about which pins to use for memory clock pins, refer to the Section I. Device and Pin Planning chapter in volume 2 of the External Memory Interface Handbook

Figure 8 9 shows the memory clock generation block diagram for Stratix III devices.

Figure 8 9. Memory Clock Generation Block Diagram (Note 1)



Notes to Figure 8–9:

(1) For more information about pin location requirements for these pins, refer to Section I. Device and Pin Planning chapter in volume 2 of the External Memory Interface Handbook

(2) The mem_clk[0] and mem_clk_n[0] pins for DDR3, DDR2, and DDR SDRAM interfaces use the I/O input buffer for feedback; therefore, bi-directional I/O buffers are used for these pins. For memory interfaces using a differential DQS input, the input buffer is configured as a differential input; for memory interfaces using a single-ended DQS input, the input buffer is configured as a single-ended input. Using a single-ended input feedback buffer requires that I/O standard's V_{REF} voltage is provided to that I/O bank's VREF pin.

Stratix III External Memory Interface Features

Stratix III devices are rich with features that allow robust high-performance external memory interfacing. The ALTMEMPHY megafunction allows you to set these external memory interface features and helps set up the physical interface (PHY) best suited for your system. This section describes each Stratix III device feature that is used in external memory interfaces from the DQS phase-shift circuitry, DQS logic block, leveling multiplexers, dynamic OCT control block, IOE registers, IOE features, and PLLs.

9. High-Speed Differential I/O Interfaces and DPA in Stratix III Devices

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Stratix® III devices offers up to 1.6-Gbps differential I/O capabilities to support source-synchronous communication protocols such as Utopia, Rapid I/O®, XSBI, SGMII, SFI, and SPI.

Stratix III devices have the following dedicated circuitry for high-speed differential I/O support:

- Differential I/O buffer
- Transmitter serializer
- Receiver deserializer
- Data realignment
- Dynamic phase aligner (DPA)
- Synchronizer (FIFO buffer)
- Analog Phase-Locked Loops (PLLs) (located on left and right sides of the device)

For high-speed differential interfaces, Stratix III devices support the following differential I/O standards:

- Low voltage differential signaling (LVDS)
- Mini-LVDS
- Reduced swing differential signaling (RSDS)
- High-speed Transceiver Logic (HSTL)
- Stub Series Terminated Logic (SSTL)