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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4300
Number of Logic Elements/Cells	107500
Total RAM Bits	4992000
Number of I/O	744
Number of Gates	-
Voltage - Supply	0.86V ~ 1.15V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep3sl110f1152c3n

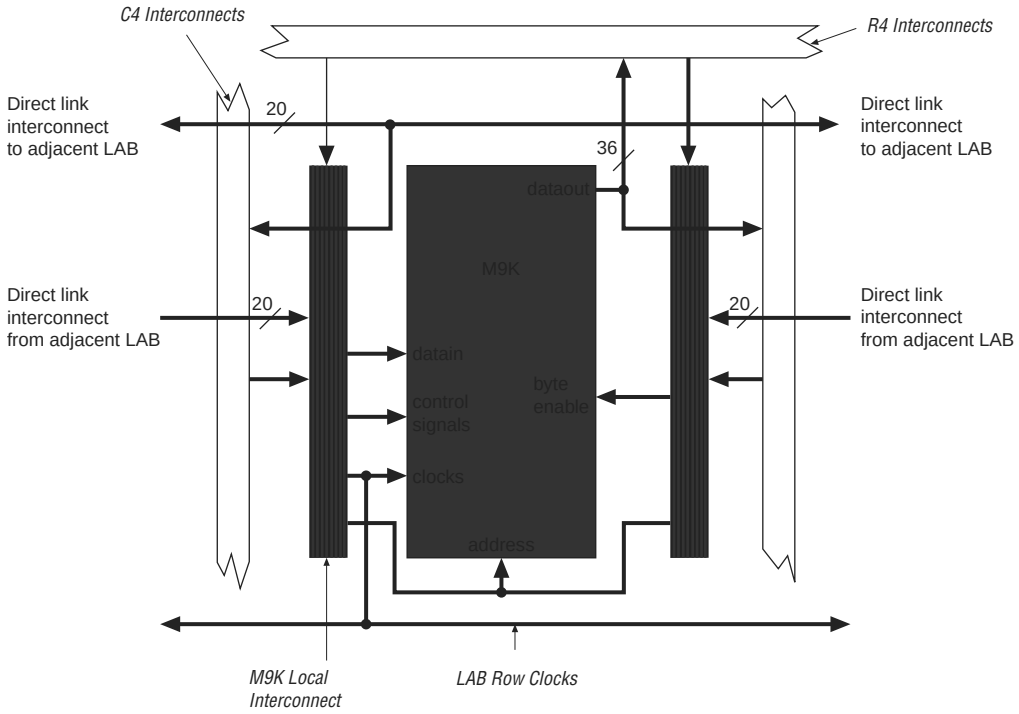
Chapter 12. Remote System Upgrades with Stratix III Devices

Chapter 13. IEEE 1149.1 (JTAG) Boundary-Scan Testing in Stratix III Devices

Chapter IV. Design Security and Single Event Upset (SEU) Mitigation

Chapter 14. Design Security in Stratix III Devices

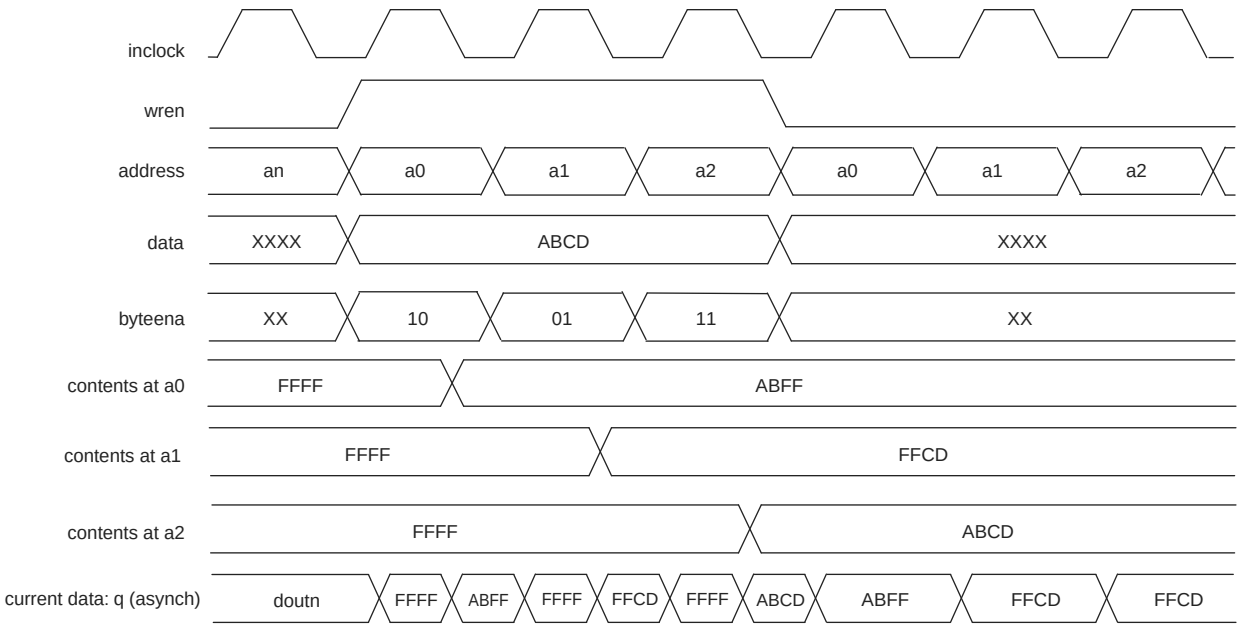
Figure 3–5. M9K RAM Block LAB Row Interface



The M144K blocks use eight interfaces in the same device column. The M144K block local interconnects are driven by R4, C4, and direct link interconnects from adjacent LABs on either the right or left side of the MRAM block. Up to 20 direct link input connections to the M144K block are possible from the left adjacent LABs and another 20 possible from the right adjacent LAB. M144K block outputs can also connect to the LABs on the block's left and right sides through direct link interconnect. Figure 3–6 shows the interface between the M144K RAM block and the logic array.

Figure 4–2 shows how the write enable (`wren`) and byte-enable (`byteena`) signals control the operations of the MLABs. The write operation in MLABs is triggered by failing clock edges.

Figure 4–2. Stratix III Byte-Enable Functional Waveform for MLABs



Packed Mode Support

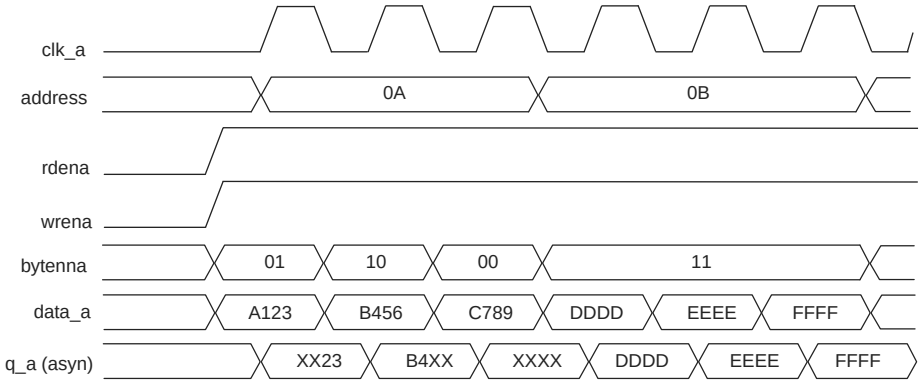
Stratix III M9K and M144K blocks support packed mode. The packed mode feature packs two independent single-port RAMs into one memory block. The Quartus II software automatically implements packed mode where appropriate by placing the physical RAM block into true dual-port mode and using the MSB of the address to distinguish between the two logical RAMs. The size of each independent single-port RAM must not exceed half of the target block size.

Address Clock Enable Support

All Stratix III memory blocks support address clock enable, which holds the previous address value for as long as the signal is enabled (`addressstall = 1`). When the memory blocks are configured in dual-port mode, each port has its own independent address clock enable. The default value for the address clock enable signals is low (disabled).

Figure 4–19 shows the sample functional waveforms of same-port read-during-write behavior with new data.

Figure 4–19. Same Port Read-During-Write: New Data Mode *(Note 1)*

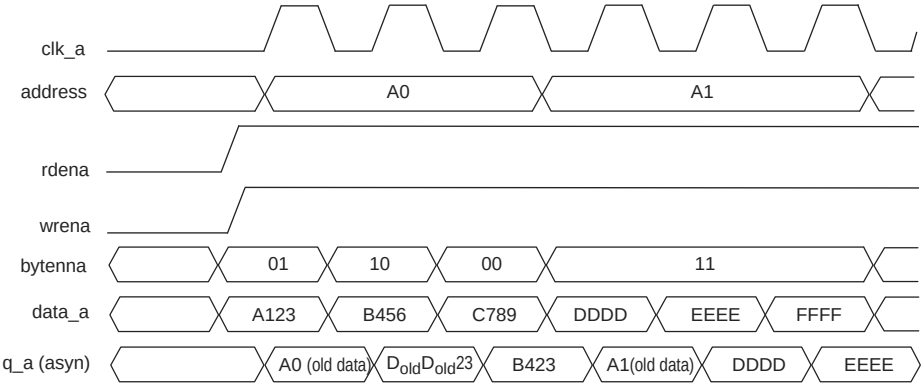


Note to Figure 4–19:

(1) "X" can be a don't care value or current data at that location, depending on the setting chosen in the Quartus II software.

Figure 4–20 shows the sample functional waveforms of same-port read-during-write behavior with old data mode.

Figure 4–20. Same Port Read-During-Write: Old Data Mode *(Note 1)*



Note to Figure 4–20:

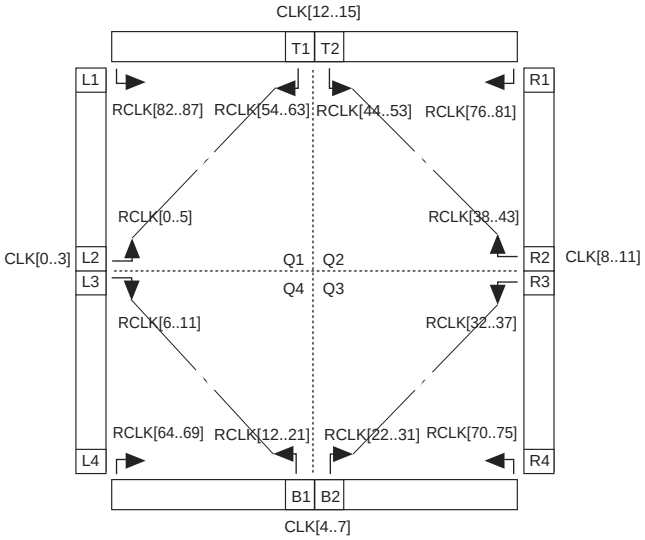
(1) D_{old} is the old data bit at address A0, A0 (old data) is the old data at address A0, and A1 (old data) is the old data at address A1.

Mixed-Port Read-During-Write Mode

This mode applies to a RAM in simple or true dual-port mode which has one port reading and the other port writing to the same address location with the same clock.

In this mode you also have two output choices: old data or don't care. In old data mode, a read-during-write operation to different ports causes the RAM outputs to reflect the old data at that address location. In don't care mode, the same operation results in a "don't care" or "unknown" value on the RAM outputs.

Figure 6–4. Regional Clock Networks (EP3SL200, EP3SE260, and EP3SL340 Devices) *(Note 1)*



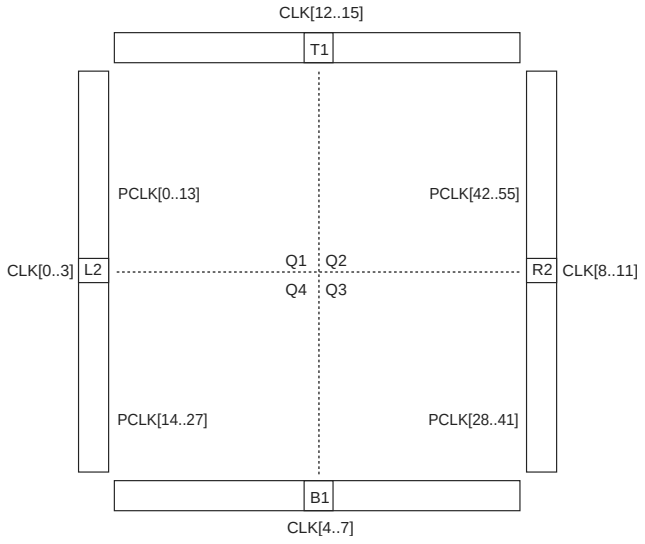
Note to Figure 6–4:

(1) The corner RCLKs [64..87] can only be fed by their respective corner PLL outputs. Refer to Table 6–9 on page 6–13 for connectivity.

Periphery Clock Networks

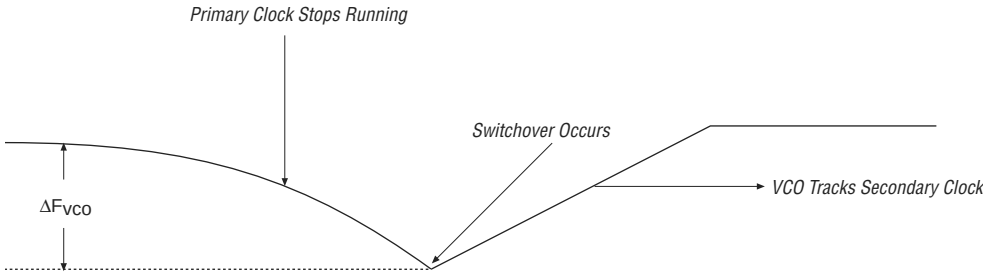
Periphery clock (PCLK) networks shown in Figure 6–5 to Figure 6–9 are a collection of individual clock networks driven from the periphery of the Stratix III device. Clock outputs from the DPA block, horizontal I/O pins, and internal logic can drive the PCLK networks. The EP3SL50, EP3SL70, and EP3SE50 devices contain 56 PCLKs; the EP3SL110, EP3SL150, EP3SL200, EP3SE80, and EP3SE110 devices contain 88 PCLKs; the EP3SE260 device contains 112 PCLKs, and the EP3SL340 device contains 132 PCLKs. These PCLKs have higher skew compared to GCLK and RCLK networks and can be used instead of general purpose routing to drive signals into and out of the Stratix III device.

Figure 6–5. Periphery Clock Networks (EP3SL50, EP3SL70, and EP3SE50 Devices)



- Applications that require a clock switchover feature and a small frequency drift should use a low-bandwidth PLL. The low-bandwidth PLL reacts more slowly than a high-bandwidth PLL to reference input clock changes. When the switchover happens, a low-bandwidth PLL propagates the stopping of the clock to the output more slowly than a high-bandwidth PLL. However, be aware that the low-bandwidth PLL also increases lock time.
- After a switchover occurs, there may be a finite resynchronization period for the PLL to lock onto a new clock. The exact amount of time it takes for the PLL to re-lock depends on the PLL configuration.
- The phase relationship between the input clock to the PLL and the output clock from the PLL is important in your design. Assert `areset` for at least 10 ns after performing a clock switchover. Wait for the locked signal to go high and be stable before re-enabling the output clocks from the PLL.
- Figure 6–36 shows how the VCO frequency gradually decreases when the current clock is lost and then increases as the VCO locks on to the backup clock.

Figure 6–36. VCO Switchover Operating Frequency



- Disable the system during clock switchover if it is not tolerant of frequency variations during the PLL resynchronization period. You can use the `clkbad[0]` and `clkbad[1]` status signals to turn off the PFD (`PFDENA = 0`) so the VCO maintains its most recent frequency. You can also use the state machine to switch over to the secondary clock. When the PFD is re-enabled, output clock-enable signals (`clkena`) can disable clock outputs during the switchover and resynchronization period. Once the lock indication is stable, the system can re-enable the output clocks.

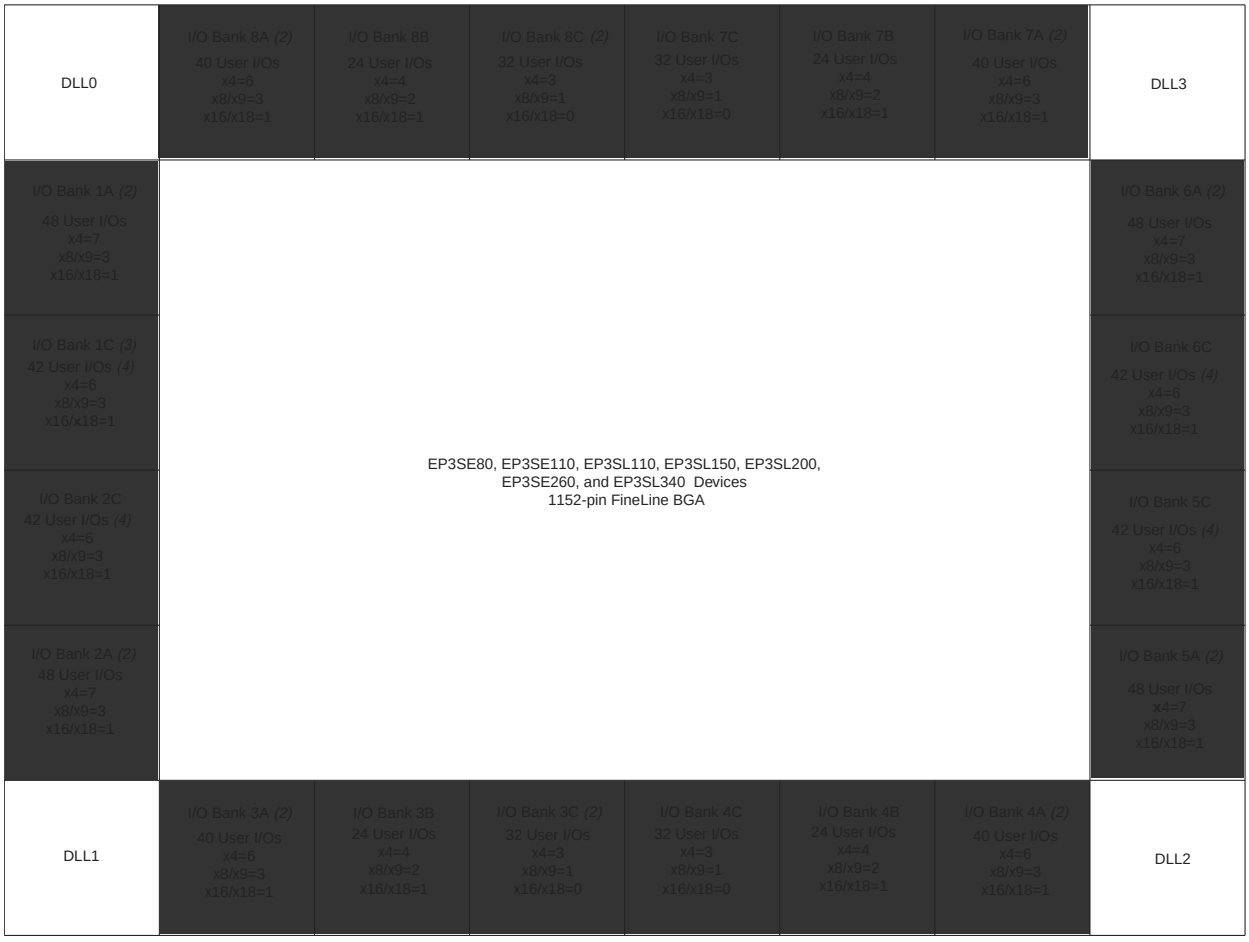
Table 7–8. Selectable I/O Standards with On-Chip Series Termination With or Without Calibration

I/O Standard	On-Chip Series Termination Setting		
	Row I/O	Column I/O	Unit
3.3-V LVTTL/LVCMOS	50	50	Ω
	25	25	Ω
3.0-V LVTTL/LVCMOS	50	50	Ω
	25	25	Ω
2.5-V LVTTL/LVCMOS	50	50	Ω
	25	25	Ω
1.8-V LVTTL/LVCMOS	50	50	Ω
	25	25	Ω
1.5-V LVTTL/LVCMOS	50	50	Ω
		25	Ω
1.2-V LVTTL/LVCMOS	50	50	Ω
		25	Ω
SSTL-2 Class I	50	50	Ω
SSTL-2 Class II	25	25	Ω
SSTL-18 Class I	50	50	Ω
SSTL-18 Class II	25	25	Ω
SSTL-15 Class I	50	50	Ω
SSTL-15 Class II	—	25	Ω
HSTL-18 Class I	50	50	Ω
HSTL-18 Class II	25	25	Ω
HSTL-15 Class I	50	50	Ω
HSTL-15 Class II	—	25	Ω
HSTL-12 Class I	50	50	Ω
HSTL-12 Class II	—	25	Ω

Expanded On-Chip Series Termination with Calibration

OCT calibration circuits always adjust OCT R_S to match the external resistors connected to the RUP and RDN pins, it is possible to achieve different OCT R_S values besides the 25- and 50-Ω resistors. Theoretically you can always change the resistance connected to the RUP and RDN pins accordingly if you require a different OCT R_S value. Practically, the OCT R_S range, which Stratix III devices can support, is limited due to the output buffer size and granularity limitations. Table 7–9 shows expanded OCT R_S with calibration supported in Stratix III devices.The Quartus II software only allows discrete OCT R_S calibration settings of 25 Ω, 40 Ω, 50 Ω, and 60 Ω. You can select the closest discrete value of OCT R_S with calibration settings in the Quartus II software to your system to get the closest timing and IBIS model information. For example, if you use 20-Ω OCT R_S with calibration in your system, you can select 25-Ω OCT R_S with calibration setting in the Quartus II software to get the closest timing and IBIS model information.

Figure 8–5. Number of DQS/DQ Groups in EP3SE80, EP3SE110, EP3SL110, EP3SL150, EP3SL200, EP3SE260, and EP3SL340 Devices in the 1152-pin FineLine BGA Package *(Note 1)*



Notes to Figure 8–5:

(1) This device does not support ×32/×36 mode.

(2) You can also use DQS/DQSn pins in some of the ×4 groups as RUP/RDN pins. You cannot use a ×4 group for memory interfaces if two pins of the group are being used as RUP and RDN pins for OCT calibration. You can still use the ×16/×18 or ×32/×36 groups that includes these ×4 groups. However, there are restrictions on using ×8/×9 groups that include these ×4 groups as described on page 8–5.

(3) Some of the DQS/DQ pins in this bank can also be used as configuration pins. Choose the DQS/DQ pins that are not going to be used by your configuration scheme.

(4) All I/O pin counts include eight dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n, CLK8p, CLK8n, CLK10p, and CLK10n).

Figure 8–20. Stratix III IOE Input Registers *(Note 1)*

Notes to Figure 8–20:

(1) You can bypass each register block in this path.
(2) This is the 0-phase resynchronization clock (from the read-leveling delay chain).
(3) The input clock can be from the DQS logic block (whether the postamble circuitry is bypassed or not) or from a global clock line.
(4) This input clock comes from the CQn logic block.
(5) This resynchronization clock can come either from the PLL or from the read-leveling delay chain.
(6) The I/O clock divider resides adjacent to the DQS logic block. In addition to the PLL and read-leveled resync clock, the I/O clock divider can also be fed by the DQS bus or CQn bus.
(7) The half-rate data and clock signals feed into a dual-port RAM in the FPGA core.
(8) You can dynamically change the `dataoutbypass` signal after configuration to select either the `directin` input or the output from the half data rate register to feed `dataout`.
(9) You must invert the strobe signal needs for DDR, DDR2, and DDR3 interfaces, except for QDR II or QDR II+ SRAM interfaces. This inversion is automatically done if you use the Altera external memory interface IPs.
(10) Each divider feeds up to six pins (from a × 4 DQS group) in the device. To feed wider DQS groups, you must chain multiple clock dividers together by feeding the `slaveout` output of one divider to the `masterin` input of the neighboring pins' divider.
(11) The **bypass_output_register** option allows you to select either the output from the second mux or the output of the fourth alignment/ synchronization register to feed `dataout`.

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10. Hot Socketing and Power-On Reset in Stratix III Devices

SIII51010-1.7

This chapter describes information about hot-socketing specifications, power-on reset (POR) requirements, and their implementation in Stratix® III devices.

Stratix III devices offer hot socketing, also known as hot plug-in or hot swap, and power sequencing support without the use of any external devices. You can insert or remove a Stratix III device or a board in a system during system operation without causing undesirable effects to the running system bus or board that is inserted into the system.

The hot socketing feature also removes some of the difficulty when you use Stratix III devices on PCBs that contain a mixture of 3.3-, 3.0-, 2.5-, 1.8-, 1.5-, and 1.2-V devices. With the Stratix III hot socketing feature, you no longer need to ensure a proper power-up sequence for each device on the board.

The Stratix III hot-socketing feature provides:

- Board or device insertion and removal without external components or board manipulation
- Support for any power-up sequence
- I/O buffers non-intrusive to system buses during hot insertion

This section also describes the POR circuitry in Stratix III devices. POR circuitry keeps the devices in the reset state until the power supplies are within operating range.

Stratix III Hot-Socketing Specifications

Stratix III devices are hot-socketing compliant without the need for external components or special design requirements. Hot socketing support in Stratix III devices has the following advantages:

- You can drive the device before power-up without damaging it.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby not affecting other buses in operation.
- You can insert a Stratix III device into or remove it from a powered-up system board without damaging or interfering with normal system/board operation.

Stratix III Devices Can Be Driven Before Power Up

You can drive signals into I/O pins, dedicated input pins, and dedicated clock pins of Stratix III devices before or during power up or power down without damaging the device. Stratix III devices support power up or power down of the power supplies in any sequence in order to simplify system-level design.

The POR circuit does not monitor the power supplies listed in Table 10–3.

Table 10–3. Power Supplies That Are Not Monitored by the POR Circuitry

Voltage Supply	Description	Setting (V)
V_{CCIO}	I/O power supply	1.2, 1.5, 1.8, 2.5, 3.0, 3.3
V_{CCA_PLL}	PLL analog global power supply	2.5
V_{CCD_PLL}	PLL digital power supply	1.1
V_{CC_CLKIN}	PLL differential clock input power supply (top and bottom I/O banks only)	2.5
V_{CCBAT}	Battery back-up power supply for design security volatile key storage	1.0 – 3.3 *(1)*

Note to Table 10–3:

(1) The nominal voltage for V_{CCBAT} is 3.0-V.

During power up, all power supplies listed in Table 10–2 and Table 10–3 are required to monotonically reach their full-rail values within t_{RAMP}.

The POR specification is designed to ensure that all the circuits in the Stratix III device are at certain known states during power up.

The POR signal pulse width is programmable using the PORSEL input pin. When PORSEL is set to low, the POR signal pulse width is set to 100 ms. A POR pulse width of 100 ms allows serial flash devices with 65 ms to 100 ms internal POR delay to be powered up and ready to receive the nSTATUS signal from Stratix III. When the PORSEL is set to high, the POR signal pulse width is set to 12 ms. A POR pulse width of 12 ms allows time for power supplies to ramp-up to full rail.

For more information about the POR specification, refer to the *DC and Switching Characteristics* chapter.

Table 11–10. PS Timing Parameters for Stratix III Devices (Part 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units
t	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode *(2)*	20	100	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	tCD2CU + (4,436 × CLKUSR period)	—	—

Notes to Table 11–10:

(1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for starting the device.

Device configuration options and how to create configuration files are discussed further in the *Device Configuration Options and Configuration File Formats* chapters in volume 2 of the *Configuration Handbook*.

PS Configuration Using a Microprocessor

In this PS configuration scheme, a microprocessor can control the transfer of configuration data from a storage device, such as flash memory, to the target Stratix III device.

You can do a PS configuration using MicroBlaster™ Passive Serial Software Driver. For more information, refer to *AN423: Configuring the MicroBlaster Passive Serial Software Driver*.

For all configuration and timing information, refer to "PS Configuration Using a MAX II Device as an External Host" on page 11–27. This section is also applicable when using a microprocessor as an external host.

PS Configuration Using a Download Cable

In this section, the generic term *download cable* includes the Altera USB-Blaster USB port download cable, MasterBlaster™ serial/USB communications cable, ByteBlaster II parallel port download cable, ByteBlasterMV™ parallel port download cable, and the EthernetBlaster download cable.

In PS configuration with a download cable, an intelligent host (such as a PC) transfers data from a storage device to the device by using the USB-Blaster, MasterBlaster, ByteBlaster II, EthernetBlaster, or ByteBlasterMV cable.

Table 11–14. Dedicated Configuration Pins on the Stratix III Device (Part 4 of 5)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
CONF_DONE	N/A	All	Bi-directional open-drain	Status output. The target device drives the CONF_DONE pin low before and during configuration. After all configuration data is received without error and the initialization cycle starts, the target device releases CONF_DONE. Status input. After all data is received and CONF_DONE goes high, the target device initializes and enters user mode. The CONF_DONE pin must have an external 10-kΩ pull-up resistor in order for the device to initialize. Driving CONF_DONE low after configuration and initialization does not affect the configured device. Do not connect bus holds or ADC to CONF_DONE pin.
nCE	N/A	All	Input	Active-low chip enable. The nCE pin activates the device with a low signal to allow configuration. The nCE pin must be held low during configuration, initialization, and user mode. In single device configuration, it should be tied low. In multi-device configuration, nCE of the first device is tied low while its nCEO pin is connected to nCE of the next device in the chain. The nCE pin must also be held low for successful JTAG programming of the device.
nCEO	N/A	All	Output	Output that drives low when device configuration is complete. In single device configuration, this pin is left floating. In multi-device configuration, this pin feeds the next device's nCE pin. The nCEO of the last device in the chain is left floating. The nCEO pin is powered by V_{CCPGM}.
ASDO *(1)*	N/A	AS	Output	Control signal from the Stratix III device to the serial configuration device in AS mode used to read out configuration data. In AS mode, ASDO has an internal pull-up resistor that is always active.
nCSO *(1)*	N/A	AS	Output	Output control signal from the Stratix III device to the serial configuration device in AS mode that enables the configuration device. In AS mode, nCSO has an internal pull-up resistor that is always active.

Table 11–14. Dedicated Configuration Pins on the Stratix III Device (Part 5 of 5)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
DCLK *(1)*	N/A	Synchronous configuration schemes (PS, FPP, AS)	Input (PS, FPP) Output (AS)	DCLK has an internal pull-up resistor (typically 25 kΩ) that is always active. In AS mode, DCLK is an output from the Stratix III device that provides timing for the configuration interface. After AS configuration, this pin is driven to an inactive state. In schemes that use a configuration device, DCLK will be driven low after configuration is done. In schemes that use a control host, DCLK should be driven either high or low, whichever is more convenient. Toggling this pin after configuration does not affect the configured device.
DATA0 *(1)*	N/A in AS mode. I/O in PS or FPP mode	PS, FPP, AS	Input	Data input. In serial configuration modes, bit-wide configuration data is presented to the target device on the DATA0 pin. In AS mode, DATA0 has an internal pull-up resistor that is always active. After PS or FPP configuration, DATA0 is available as a user I/O pin and the state of this pin depends on the **Dual-Purpose Pin** settings.
DATA[7..1]	I/O	Parallel configuration schemes (FPP)	Inputs	Data inputs. Byte-wide configuration data is presented to the target device on DATA[7..0]. In serial configuration schemes, they function as user I/O pins during configuration, which means they are tri-stated. After configuration, DATA[7..1] are available as user I/O pins and the state of these pin depends on the **Dual-Purpose Pin** settings.

Note to Table 11–14:

(1) To tri-state AS configuration pins in AS configuration scheme, turn on **Enable input tri-state on active configuration pins in user mode** option from the **Device and Pin Options** dialog box. This tri-states DCLK, nCSO, Data0, and ASDO pins. Dual-purpose Pins Setting for Data0 is ignored. To set Data0 to a different setting, for example to use Data0 pin as a regular I/O in user mode, turn off **Enable input tri-state on active configuration pins in user mode** option and set your desired setting from the Dual-purpose Pins Setting menu.

ALTREMOTE_UPDATE Megafunction

The ALTREMOTE_UPDATE megafunction provides a memory-like interface to the remote system upgrade circuitry and handles the shift register read/write protocol in Stratix III device logic. This implementation is suitable for designs that implement the factory configuration functions using a Nios II processor or user logic in the device.

Figure 12–8 shows the interface signals between the ALTREMOTE_UPDATE megafunction and Nios II processor / user logic.

Figure 12–8. Interface Signals Between the ALTREMOTE_UPDATE Megafunction and the Nios II Processor

For more information about the ALTREMOTE_UPDATE Megafunction and the description of ports listed in Figure 12–8, refer to the *ALTREMOTE_UPDATE Megafunction User Guide*.

Table 13–1 summarizes the functions of each of these pins.

Table 13–1. IEEE Std. 1149.1 Pin Descriptions

Pin	Description	Function
TDI	Test data input	Serial input pin for instructions as well as test and programming data. Signal applied to TDI is expected to change state at the falling edge of TCK. Data is shifted in on the rising edge of TCK.
TDO	Test data output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device.
TMS	Test mode select	Input pin that provides the control signal to determine the transitions of the test access port (TAP) controller state machine. Transitions within the state machine occur at the rising edge of TCK. Therefore, you must set up TMS before the rising edge of TCK. TMS is evaluated on the rising edge of TCK. During non-JTAG operation, Altera recommends you drive TMS high.
TCK	Test clock input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge.
TRST *(1)*	Test reset input (optional)	Active-low input to asynchronously reset the boundary-scan circuit. For non-JTAG users, you should permanently tie the pin to GND.

Note to Table 13–1:

(1) The minimum TRST pulse width to reset the JTAG TAP controller is 60 ns.

The IEEE Std. 1149.1 BST circuitry requires the following registers:

- The instruction register determines the action to be performed and the data register to be accessed.
- The bypass register is a one-bit-long data register that provides a minimum-length serial path between TDI and TDO.
- The boundary-scan register is a shift register composed of all the boundary-scan cells of the device.

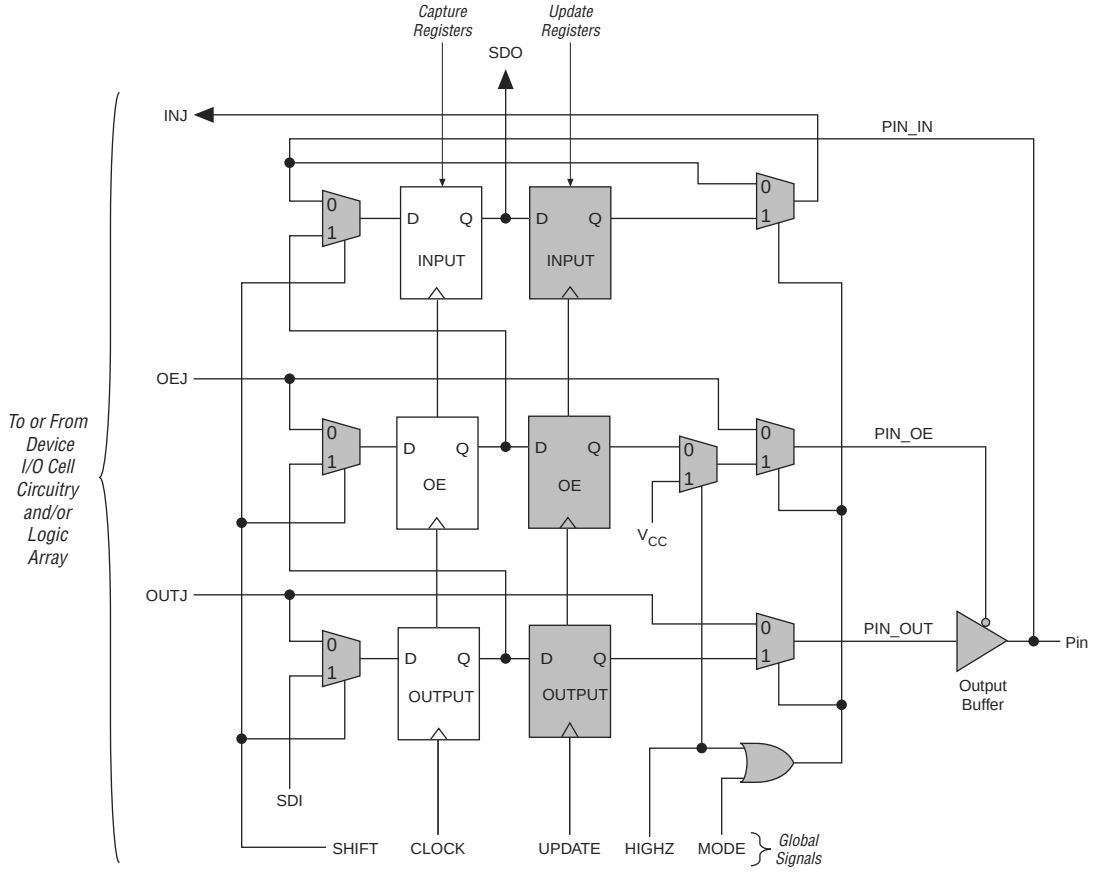
Boundary-Scan Cells of a Stratix III Device I/O Pin

The Stratix III device three-bit boundary-scan cell (BSC) consists of a set of capture registers and a set of update registers. The capture registers can connect to internal device data through the `OUTJ`, `OEJ`, and `PIN_IN` signals, while the update registers connect to external data through the `PIN_OUT` and `PIN_OE` signals.

The global control signals for the IEEE Std. 1149.1 BST registers (such as `shift`, `clock`, and `update`) are generated internally by the TAP controller. The `MODE` signal is generated by a decode of the instruction register. The `HIGHZ` signal is high when executing the `HIGHZ` instruction. The data signal path for the boundary-scan register runs from the serial data in (`SDI`) signal to the serial data out (`SDO`) signal. The scan register begins at the `TDI` pin and ends at the `TDO` pin of the device.

Figure 13–4 shows the Stratix III device's user I/O boundary-scan cell.

Figure 13–4. Stratix III Device's User I/O BSC with IEEE Std. 1149.1 BST Circuitry



17. Stratix III Device Packaging Information

SIII51017-1.7

This chapter provides thermal resistance values and package information for Altera® Stratix® III devices, including:

- "Thermal Resistance" on page 17–2
- "Package Outlines" on page 17–2

Table 17–1 lists which Stratix III device, are available in FineLine BGA or Hybrid FineLine BGA packages.

Table 17–1. FineLine and Hybrid FineLine BGA Packages for Stratix III Devices

Device	Package	Pins
EP3SL50	FineLine BGA - Flip Chip (Option 1)	484
	FineLine BGA - Flip Chip (Option 1)	780
EP3SL70	FineLine BGA - Flip Chip (Option 1)	484
	FineLine BGA - Flip Chip (Option 1)	780
EP3SL110	FineLine BGA - Flip Chip (Option 1)	780
	FineLine BGA - Flip Chip (Option 1)	1152
EP3SL150	FineLine BGA - Flip Chip (Option 1)	780
	FineLine BGA - Flip Chip (Option 1)	1152
EP3SL200	Hybrid FineLine BGA - Flip Chip (Option 1)	780
	FineLine BGA - Flip Chip (Option 1)	1152
	FineLine BGA - Flip Chip (Option 1)	1517
EP3SL340	Hybrid FineLine BGA - Flip Chip (Option 1)	1152
	FineLine BGA - Flip Chip (Option 1)	1517
	FineLine BGA - Flip Chip (Option 1)	1760
EP3SE50	FineLine BGA - Flip Chip (Option 1)	484
	FineLine BGA - Flip Chip (Option 1)	780
EP3SE80	FineLine BGA - Flip Chip (Option 1)	780
	FineLine BGA - Flip Chip (Option 1)	1152
EP3SE110	FineLine BGA - Flip Chip (Option 1)	780
	FineLine BGA - Flip Chip (Option 1)	1152
EP3SE260	Hybrid FineLine BGA - Flip Chip (Option 1)	780
	FineLine BGA - Flip Chip (Option 1)	1152
	FineLine BGA - Flip Chip (Option 1)	1517