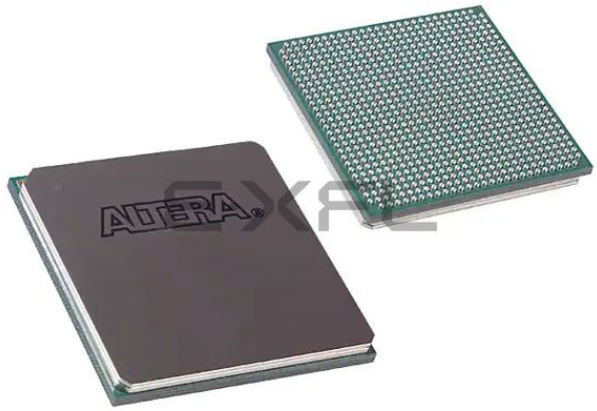

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4300
Number of Logic Elements/Cells	107500
Total RAM Bits	4992000
Number of I/O	488
Number of Gates	-
Voltage - Supply	0.86V ~ 1.15V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep3sl110f780c3n

Chapter 3. MultiTrack Interconnect in Stratix III Devices

Chapter 4. TriMatrix Embedded Memory Blocks in Stratix III Devices

Table 1–1 lists the Stratix III FPGA family features.

Table 1–1. FPGA Family Features for Stratix III Devices

	Device/ Feature	ALMs	LEs	M9K Blocks	M144K Blocks	MLAB Blocks	Total Embedded RAM Kbits	MLAB RAM Kbits *(1)*	Total RAM Kbits*(2)*	18×18-bit Multipliers (FIR Mode)	PLLs *(3)*
Stratix III Logic Family	EP3SL50	19K	47.5K	108	6	950	1,836	297	2,133	216	4
	EP3SL70	27K	67.5K	150	6	1,350	2,214	422	2,636	288	4
	EP3SL110	43K	107.5K	275	12	2,150	4,203	672	4,875	288	8
	EP3SL150	57K	142.5K	355	16	2,850	5,499	891	6,390	384	8
	EP3SL200	80K	200K	468	36	4,000	9,396	1,250	10,646	576	12
	EP3SL340	135K	337.5K	1,040	48	6,750	16,272	2,109	18,381	576	12
Stratix III Enhanced Family	EP3SE50	19K	47.5K	400	12	950	5,328	297	5,625	384	4
	EP3SE80	32K	80K	495	12	1,600	6,183	500	6,683	672	8
	EP3SE110	43K	107.5K	639	16	2,150	8,055	672	8,727	896	8
	EP3SE260	102K	255K	864	48	5,100	14,688	1,594	16,282	768	12

Notes to Table 1–1:

(1) MLAB ROM mode supports twice the number of MLAB RAM Kbits.

(2) For total ROM Kbits, use this equation to calculate:
Total ROM Kbits = Total Embedded RAM Kbits + [(# of MLAB blocks × 640)/1024]

(3) The availability of the PLLs shown in this column is based on the device with the largest package. Refer to the *Clock Networks and PLLs in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook* for the availability of the PLLs for each device.

The Stratix III logic family (*L*) offers balanced logic, memory, and multipliers to address a wide range of applications, while the enhanced family (*E*) offers more memory and multipliers per logic and is ideal for wireless, medical imaging, and military applications.

Stratix III devices are available in space-saving FineLine BGA (FBGA) packages (refer to Table 1–2 and Table 1–3).

Table 1–5. Speed Grades for Stratix III Devices (Part 2 of 2)

Device	Temperature Grade	484 -Pin FineLine BGA	780-Pin FineLine BGA	780-Pin Hybrid FineLine BGA	1152-Pin FineLine BGA	1152-Pin Hybrid FineLine BGA	1517-Pin FineLine BGA	1760-Pin FineLine BGA
EP3SE260	Commercial	—	—	–2, –3, –4, –4L	–2,– 3, –4, –4L	—	–2, –3, –4, –4L	—
	Industrial *(1)*	—	—	–3, –4, –4L	–3, –4, –4L	—	–3, –4,–4L	—

Note to Table 1–5:

(1) For EP3SL340, EP3SL200, and EP3SE260 devices, the industrial junction temperature range for –4L is 0–100°C, regardless of supply voltage.

Architecture Features

The following section describes the various features of the Stratix III family FPGAs.

Logic Array Blocks and Adaptive Logic Modules

The Logic Array Block (LAB) is composed of basic building blocks known as Adaptive Logic Modules (ALMs) that can be configured to implement logic, arithmetic, and register functions. Each LAB consists of ten ALMs, carry chains, shared arithmetic chains, LAB control signals, local interconnect, and register chain connection lines. ALMs are part of a unique, innovative logic structure that delivers faster performance, minimizes area, and reduces power consumption. ALMs expand the traditional 4-input look-up table architecture to 7 inputs, increasing performance by reducing LEs, logic levels, and associated routing. In addition, ALMs maximize DSP performance with dedicated functionality to efficiently implement adder trees and other complex arithmetic functions. The Quartus II Compiler places associated logic in an LAB or adjacent LABs, allowing the use of local, shared arithmetic chain, and register chain connections for performance and area efficiency.

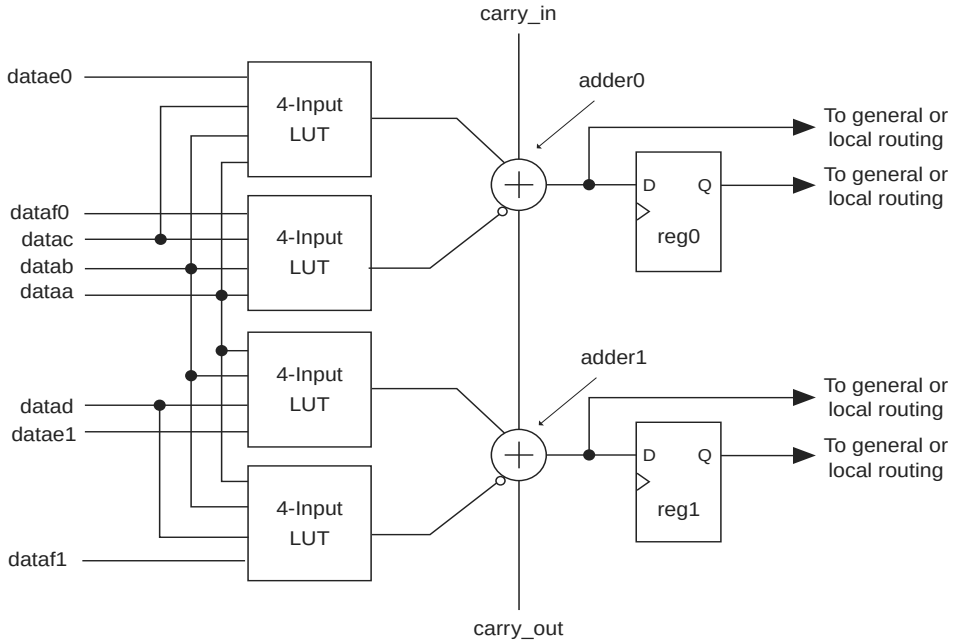
The Stratix III LAB has a new derivative called Memory LAB (or MLAB), which adds SRAM memory capability to the LAB. MLAB is a superset of the LAB and includes all LAB features. MLABs support a maximum of 320 bits of simple dual-port Static Random Access Memory (SRAM). Each ALM in an MLAB can be configured as a 16×2 block, resulting in a configuration of 16×20 simple dual port SRAM block. MLAB and LAB blocks always co-exist as pairs in all Stratix III families, allowing up to 50% of the logic (LABs) to be traded for memory (MLABs).

For more information about LABs and ALMs, refer to the *Logic Array Blocks and Adaptive Logic Modules in Stratix III Devices* chapter.

For more information about MLAB modes, features and design considerations, refer to the *TriMatrix Embedded Memory Blocks in Stratix III Devices* chapter.

The four LUTs share the `dataa` and `datab` inputs. As shown in Figure 2–11, the carry-in signal feeds to `adder0`, and the carry-out from `adder0` feeds to carry-in of `adder1`. The carry-out from `adder1` drives to `adder0` of the next ALM in the LAB. ALMs in arithmetic mode can drive out registered and/or unregistered versions of the adder outputs.

Figure 2–11. ALM in Arithmetic Mode



While operating in arithmetic mode, the ALM can support simultaneous use of the adder's carry output along with combinational logic outputs. In this operation, the adder output is ignored. This usage of the adder with the combinational logic output provides resource savings of up to 50% for functions that can use this ability. An example of such functionality is a conditional operation, such as the one shown in Figure 2–12.

Figure 3–9. Row I/O Block Connection to Interconnect

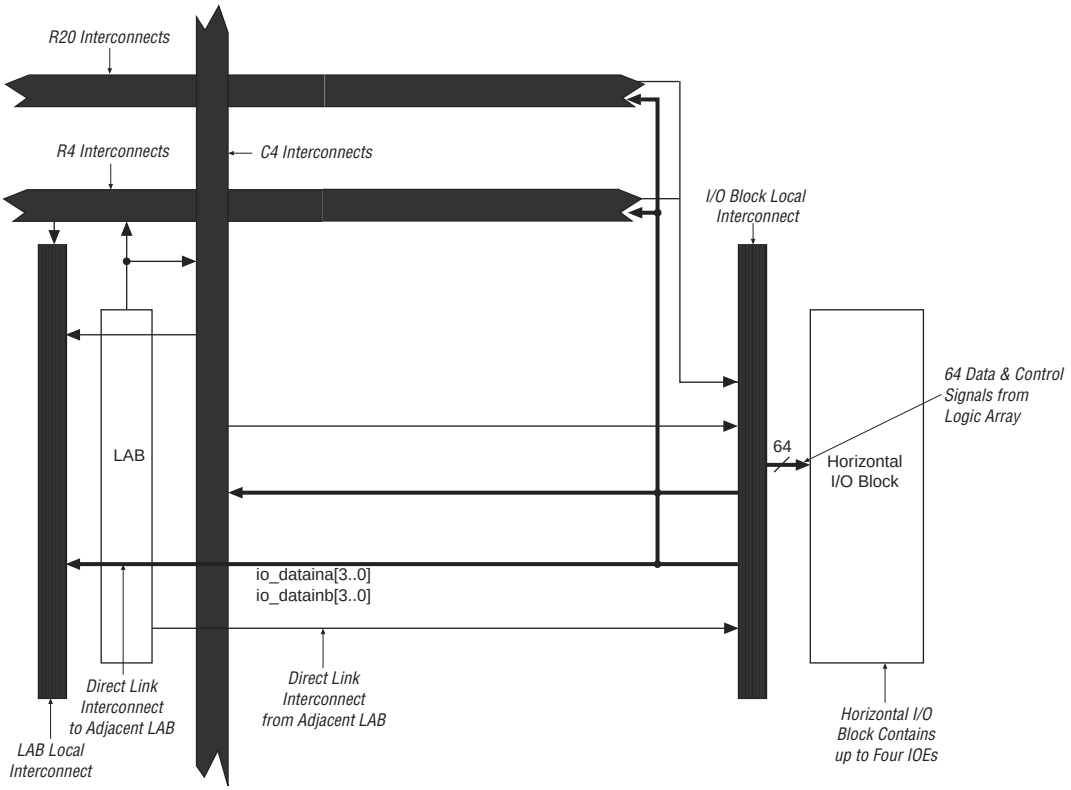


Table 5–7. Comparison of Round-to-Nearest-Integer and Round-to-Nearest-Even

Round-To-Nearest-Integer	Round-To-Nearest-Even
010111 ⇒0110	010111 ⇒0110
001101 ⇒0011	001101 ⇒0011
001010 ⇒0011	001010 ⇒0010
001110 ⇒0100	001110 ⇒0100
110111 ⇒1110	110111 ⇒1110
101101 ⇒1011	101101 ⇒1011
110110 ⇒1110	110110 ⇒1110
110010 ⇒1101	110010 ⇒1100

Two saturation modes are supported in Stratix III:

- Asymmetric saturation mode
- Symmetric saturation mode

You must select one of the two options at compile time.

In 2's complement format, the maximum negative number that can be represented is $-2^{(n-1)}$ while the maximum positive number is $2^{(n-1)}-1$. Symmetrical saturation will limit the maximum negative number to $-2^{(n-1)} + 1$. For example, for 32 bits:

- Asymmetric 32-bit saturation: Max = 0x7FFFFFFF, Min = 0x80000000
- Symmetric 32-bit saturation: Max = 0x7FFFFFFF, Min = 0x80000001

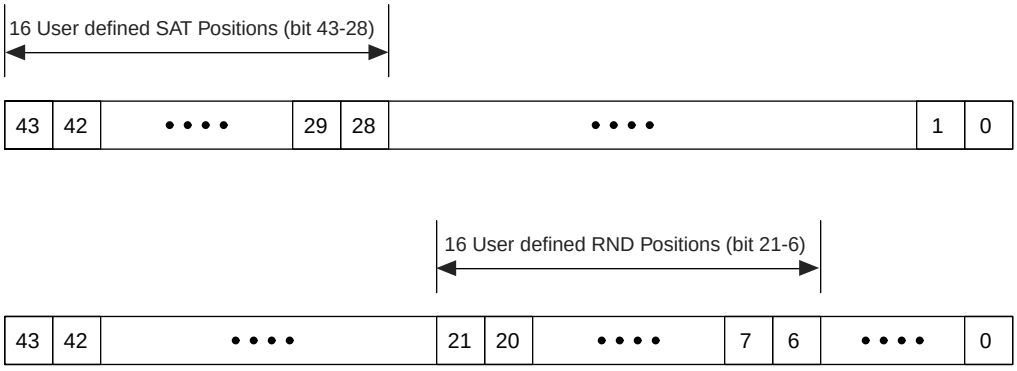
Table 5–8 lists how the saturation works. In this example, a 44-bit input is saturated to 36-bits.

Table 5–8. Examples of Saturation

44 to 36 Bits Saturation	Symmetric SAT Result	Asymmetric SAT Result
5926AC01342h	7FFFFFFFh	7FFFFFFFh
ADA38D2210h	800000001h	800000000h

Stratix III devices have up to 16 configurable bit positions out of the 44-bit bus ([43:0]) for the round and saturate logic unit providing higher flexibility. You must select the 16 configurable bit positions at compile time. These 16-bit positions are located at bits [21:6] for rounding and [43:28] for saturation, as shown in Figure 5–21.

Figure 5–21. Round and Saturation Locations



For symmetric saturation, the RND bit position is also used to determine where the LSP for the saturated data is located.

You can use the rounding and saturation function described above in regular supported multiplication operations as specified in Table 5–2. However, for accumulation type operations, the following convention is used.

The functionality of the round logic unit is in the format of:

Result = RND[S(A × B)], when used for an accumulation type of operation.

Likewise, the functionality of the saturation logic unit is in the format of:

Result = SAT[S(A × B)], when used for an accumulation type of operation.

If both the round and saturation logic units are used for an accumulation type of operation, the format is:

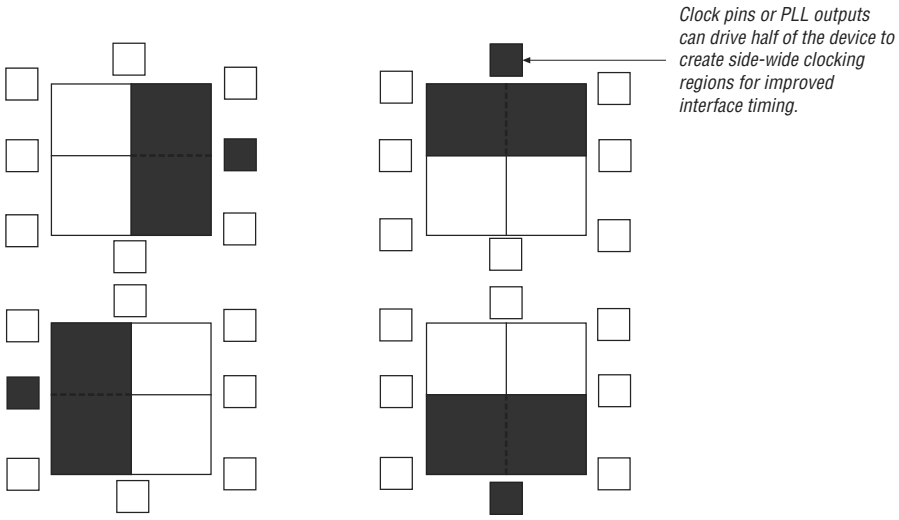
Result = SAT[RND[S(A × B)]]

In order to form the entire device clock region, a source (not necessarily a clock signal) drives a global clock network that can be routed through the entire device. This clock region has the maximum delay compared to other clock regions but allows the signal to reach every destination within the device. This is a good option for routing global reset/clear signals or routing clocks throughout the device.

In order to form a regional clock region, a source drives a single-quadrant of the device. This clock region provides the lowest skew within a quadrant and is a good option if all destinations are within a single device quadrant.

To form a dual-regional clock region, a single source (a clock pin or PLL output) generates a dual-regional clock by driving two regional clock networks (one from each quadrant). This technique allows destinations across two device quadrants to use the same low-skew clock. The routing of this signal on an entire side has approximately the same delay as in a regional clock region. Internal logic can also drive a dual-regional clock network. Corner PLL outputs only span one quadrant and hence cannot generate a dual-regional clock network. Figure 6–10 shows the dual-regional clock region.

Figure 6–10. Stratix III Dual-Regional Clock Region



Clock Network Sources

In Stratix III devices, clock input pins, PLL outputs, and internal logic can drive the global and regional clock networks. Refer to Table 6–2 to Table 6–6 for the connectivity between dedicated `CLK[0..15]` pins and the global and regional clock networks.

Dedicated Clock Inputs Pins

The `CLK` pins can either be differential clocks or single-ended clocks. Stratix III devices support 16 differential clock inputs or 32 single-ended clock inputs. You can also use the dedicated clock input pins `CLK[15..0]` for high fan-out control signals such as asynchronous clears, presets, and clock enables for protocol signals such as `TRDY` and `IRDY` for PCI through global or regional clock networks.

Table 6–3 lists the connectivity between the dedicated clock input pins and RCLKs in device Quadrant 1. A given clock input pin can drive two adjacent regional clock networks to create a dual-regional clock network.

Table 6–3. Clock Input Pin Connectivity to Regional Clock Networks (Quadrant 1)

Clock Resource	CLK (p/n Pins)															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RCLK0	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK1	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK2	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK3	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—
RCLK4	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK5	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK54	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓
RCLK55	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—
RCLK56	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—
RCLK57	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	—
RCLK58	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓
RCLK59	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—
RCLK60	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—
RCLK61	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	—
RCLK62	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓
RCLK63	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—

Table 6–4 lists the connectivity between the dedicated clock input pins and RCLKs in device Quadrant 2. A given clock input pin can drive two adjacent regional clock networks to create a dual-regional clock network.

Table 6–4. Clock Input Pin Connectivity to Regional Clock Networks (Quadrant 2) (Part 1 of 2)

Clock Resource	CLK (p/n Pins)															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RCLK38	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	—	—
RCLK39	—	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—
RCLK40	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—
RCLK41	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—
RCLK42	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	—	—
RCLK43	—	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—
RCLK44	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓
RCLK45	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—
RCLK46	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—
RCLK47	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	—
RCLK48	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓
RCLK49	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—

Source-Synchronous Mode for LVDS Compensation

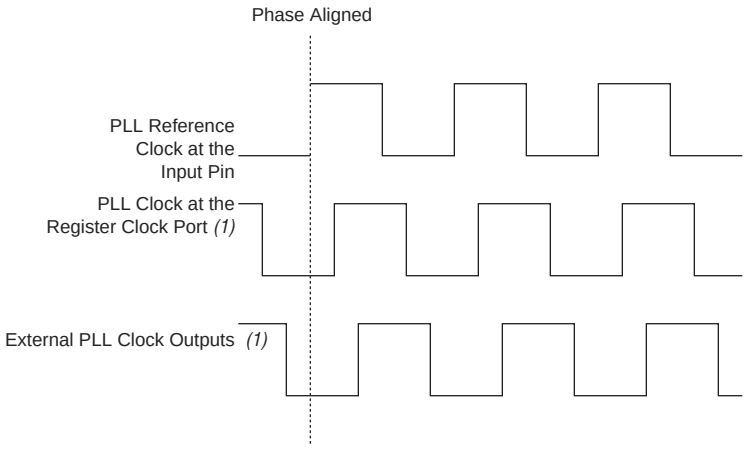
The goal of this mode is to maintain the same data and clock timing relationship seen at the pins at the internal SERDES capture register, except that the clock is inverted (180-degree phase shift). Thus, this mode ideally compensates for the delay of the LVDS clock network plus any difference in delay between these two paths:

- Data pin-to-SERDES capture register
- Clock input pin-to-SERDES capture register. In addition, the output counter needs to provide the 180-degree phase shift.

No-Compensation Mode

In the no-compensation mode, the PLL does not compensate for any clock networks. This mode provides better jitter performance because the clock feedback into the PFD passes through less circuitry. Both the PLL internal- and external-clock outputs are phase-shifted with respect to the PLL clock input. Figure 6–25 shows an example waveform of the PLL clocks' phase relationship in this mode.

Figure 6–25. Phase Relationship Between PLL Clocks in No Compensation Mode



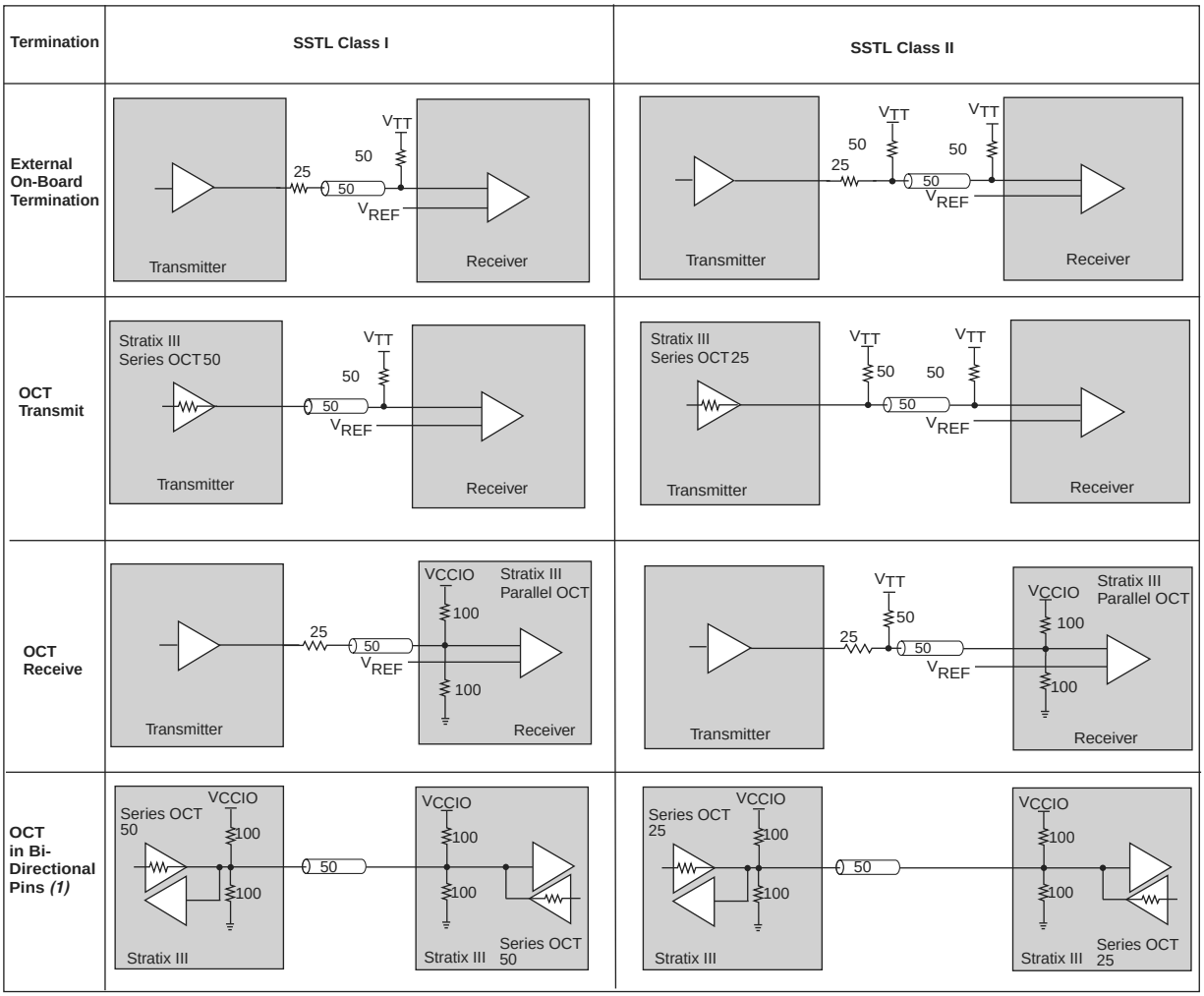
Note to Figure 6–25:

(1) The PLL clock outputs will lag the PLL input clocks, depending on routing delays.

Normal Mode

An internal clock in normal mode is phase-aligned to the input clock pin. The external clock-output pin has a phase delay relative to the clock input pin if connected in this mode. The Quartus II software timing analyzer reports any phase difference between the two. In normal mode, the delay introduced by the GCLK or RCLK network is fully compensated. Figure 6–26 shows an example waveform of the PLL clocks' phase relationship in this mode.

Figure 7–20. SSTL I/O Standard Termination for Stratix III Devices

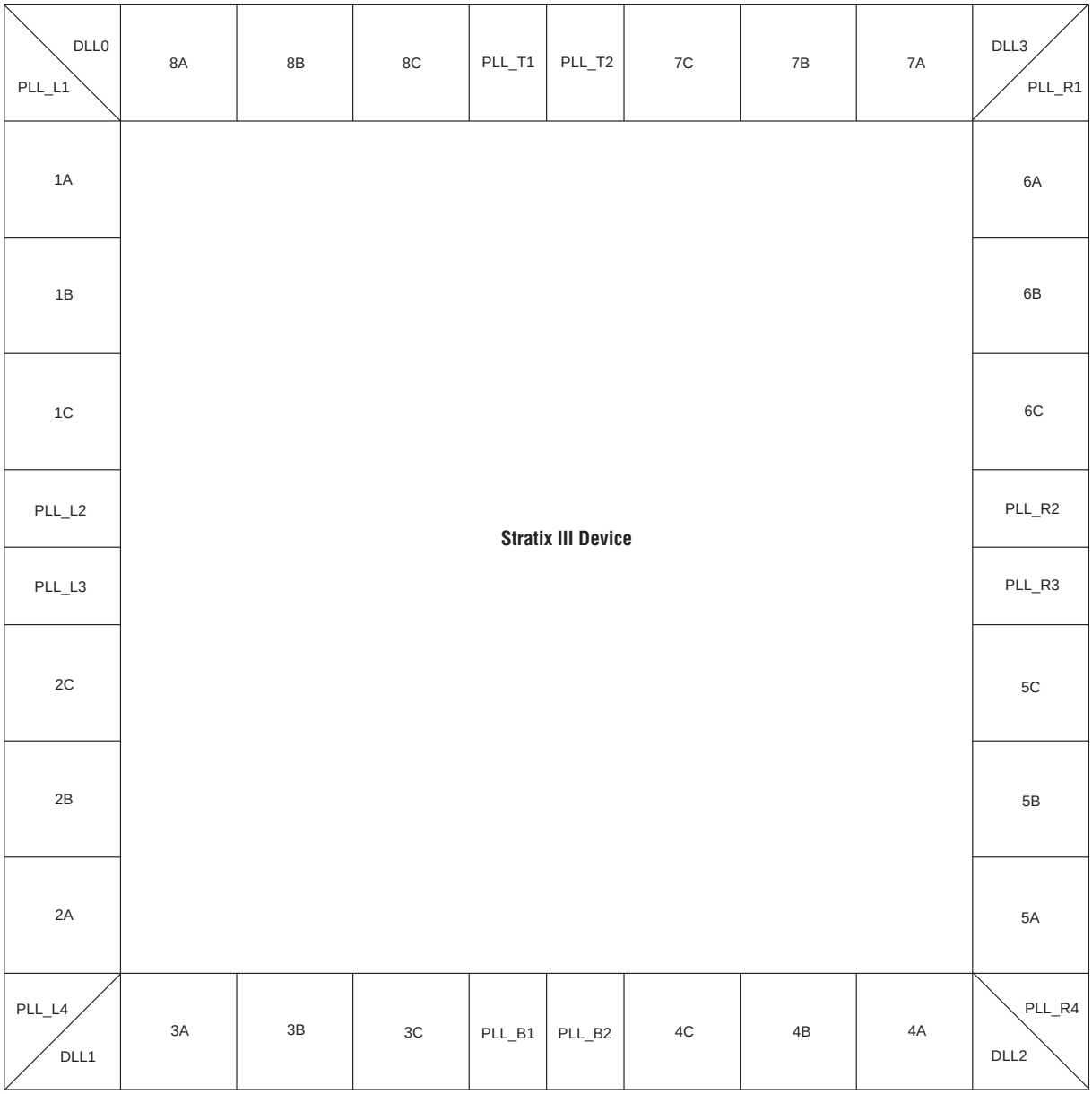


Note to Figure 7–20:

(1) In Stratix III devices, series and parallel OCT cannot be used simultaneously. For more information, refer to "Dynamic OCT" on page 7–25.

Figure 8–1 shows a package bottom view for Stratix III external memory support, showing the phase-locked loop (PLL), delay-locked loop (DLL), and I/O banks. The number of available I/O banks and PLLs depend on the device density.

Figure 8–1. Package Bottom View for Stratix III Devices *(Note 1), (2)*



Notes to Figure 8–1:

(1) The number of I/O banks and PLLs available depends on the device density.

(2) There is only one PLL in the center of each side of the device in EP3SL50, EP3SL70, and EP3SE50 devices.

vertical migration with the ×36 emulation implementation, check if migration is possible by enabling device migration in the Quartus II project. Table 8–4 shows the possible I/O sub-bank combinations to form two ×36 groups. On Stratix III devices that do not have ×36 groups. Other Stratix III devices in the 1517 - and 1760 - pin packages support this implementation as well.

☞ Splitting the read or write data bus over more than one device edge is not recommended.

Table 8–4. I/O Sub-Bank Combinations for Stratix III Devices that do not have ×36 Groups to form two ×36 Groups.

Package	Device	I/O Sub-Bank Combinations
780-pin FineLine BGA	EP3SL50, EP3SL70, EP3SE80, EP3SE110, EP3SL110, EP3SL150, EP3SL200, and EP3SE260	■ 1A and 2A ■ 5A and 6A ■ 3A and 4A ■ 7A and 8A
1152-pin FineLine BGA	EP3SE80, EP3SE110, EP3SL110, EP3SL150, EP3SL200, EP3SE260, and EP3SL340	■ 1A and 1C ■ 2A and 2C ■ 3A and 3B ■ 4A and 4B ■ 5A and 5C ■ 6A and 6C ■ 7A and 7B ■ 8A and 8B
1517-pin FineLine BGA	EP3SL200, EP3SE260, and EP3SL340	■ 1A and 1B ■ 2A and 2B or 1B and 1C ■ 2B and 2C *(2)* ■ 5A and 5B ■ 6A and 6B or 5B and 5C ■ 6B and 6C *(2)*
1760-pin FineLine BGA *(1)*	EP3SL340	■ 1A and 1B ■ 2A and 2B or 1B and 1C ■ 2B and 2C *(2)* ■ 5A and 5B ■ 6A and 6B or 5B and 5C ■ 6B and 6C *(2)*

Notes to Table 8–4:

(1) This device supports ×36 DQ/DQS groups on the top and bottom I/O banks natively.

(2) You can combine the ×16/×18 DQ/DQS groups from I/O banks 1A and 1C, 2A and 2C, 5A and 5C, 6A and 6C. However, this process is discouraged because of the size of the package. Similarly, crossing a bank number (for example combining groups from I/O banks 6C and 5C) is not supported in this package.

The output path is designed to route combinatorial or registered single data rate (SDR) outputs and full-rate or half-rate DDR outputs from the FPGA core. Half-rate data is converted to full-rate using the HDR block and is clocked by the half-rate clock from the PLL. Resynchronization registers are also clocked by the same 0° system clock, except in the DDR3 SDRAM interface where the leveling registers are clocked by the write-leveling clock.

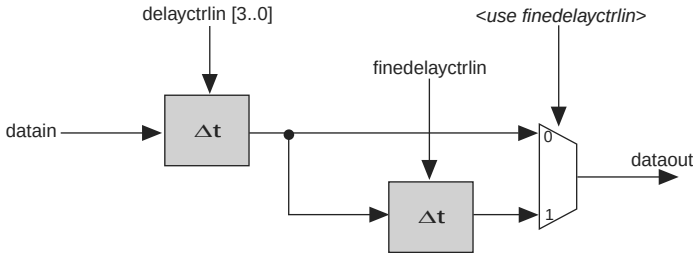
For more information about the write leveling delay chain, refer to "Leveling Circuitry" on page 8–31.

The output-enable path has structure similar to the output path. You can have a combinatorial or registered output in SDR applications and you can use half-rate or full-rate operation in DDR applications. You also have the resynchronization registers similar to the output path registers structure, ensuring that the output-enable path goes through the same delay and latency as the output path.

Delay Chain

Stratix III devices have run-time adjustable delay chains in the I/O blocks and the DQS logic blocks. You can control the delay chain setting through the I/O or the DQS configuration block output. Figure 8–22 shows the delay chain ports.

Figure 8–22. Delay Chain



Every I/O block contains the following:

- Two delay chains in series between the output registers and output buffer
- One delay chain between the input buffer and input register
- Two delay chains between the output enable and output buffer
- Two delay chains between the OCT R_T enable control register and output buffer

OCT

Stratix III devices feature dynamic calibrated OCT, in which series termination (OCT R_S) is turned on when driving signals and turned off when receiving signals, while the parallel termination (OCT R_T) is turned off when driving signals and turned on when receiving signals. This feature complements the DDR3/DDR2 SDRAM on-die termination (ODT), whereby memory termination is turned off when the memory is sending data and turned on when receiving data. You can also use OCT for other memory interfaces to improve signal integrity.

☞ You cannot use the programmable drive strength and programmable slew rate features when using OCT R_S.

To use dynamic calibrated OCT, you must use the R_{UP} and R_{DN} pins to calibrate the OCT calibration block. You can use one OCT calibration block to calibrate one type of termination with the same V_{CCIO} on the entire device. There are up to ten OCT calibration blocks to allow for different types of terminations throughout the device. For more information, refer to "Dynamic OCT Control" on page 8–33.

☞ You have the option to use the OCT R_S feature with or without calibration. However, the OCT R_T feature is only available with calibration.

You can also use the R_{UP} and R_{DN} pins as DQ pins. However, you cannot use the ×4 DQS/DQ groups where the R_{UP} and R_{DN} pins are located if you are planning to use dynamic calibrated OCT. The R_{UP} and R_{DN} pins are located in the first and last ×4 DQS/DQ group on each side of the device.

Use the OCT RT/RS setting for uni-directional read and write data; use a dynamic OCT setting for bi-directional data signals.

Programmable IOE Delay Chains

You can use programmable delay chains in the Stratix III I/O registers as deskewing circuitry. Each pin can have a different input delay from the pin to input register or a delay from the output register to the output pin to ensure that the bus has the same delay going into or out of the FPGA. This feature helps read and write time margins as it minimizes the uncertainties between signals in the bus.

☞ Deskewing circuitry and programmable IOE delay chains are the same circuit.

Programmable Output Buffer Delay

In addition to allowing output buffer duty cycle adjustment, the programmable output buffer delay chain allows you to adjust the delays between data bits in your output bus to introduce or compensate channel-to-channel skew. Incorporating skew to the output bus helps to minimize simultaneous switching events by enabling smaller parts of the bus to switch simultaneously, instead of the whole bus. This feature is particularly useful in DDR3 SDRAM interfaces where the memory system clock delay can be much larger than the data and data clock/strobe delay. Use this delay chain to add delay to the data and data clock/strobe to better match the memory system clock delay.

Table 8–13. Chapter Revision History (Part 2 of 2)

Date and Revision	Changes Made	Summary of Changes
November 2007, version 1.3	■ Updated Table 8–5. ■ Updated Figure 8–6.	Minor updates to content.
October 2007, version 1.2	■ Updated Table 8–1, Table 8–3, Table 8–4, Table 8–5. ■ Added Table 8–2. ■ Minor text edits. ■ Updated Figure 8–3, note 3 to Figure 8–4, note 3 to Figure 8–5, note 2 to Figure 8–6, added a note to Figure 8–7, added a note and updated Figure 8–10, notes to Figure 8–11, and updated Figure 8–12. ■ Added new material to “Memory Clock Pins” on page 8–21. ■ Added section “Referenced Documents”. ■ Added live links for references.	Minor updates to content.
May 2007, version 1.1	■ Updated Figure 8–5, Figure 8–8, Figure 8–14, Figure 8–18, Figure 8–19, Figure 8–20, and Figure 8–21. ■ Added new figure, Figure 8–17. ■ Added memory support information for -4L in Table 8–1, Table 8–8, Table 8–10, and Table 8–11. ■ Added new material to section “Phase Offset Control” on page 8–32.	Minor updates to content.
November 2006, version 1.0	Initial Release.	—

Figure 9–18. Corner and Center Left/Right PLLs Driving DPA-Enabled Differential I/Os in the Same Bank

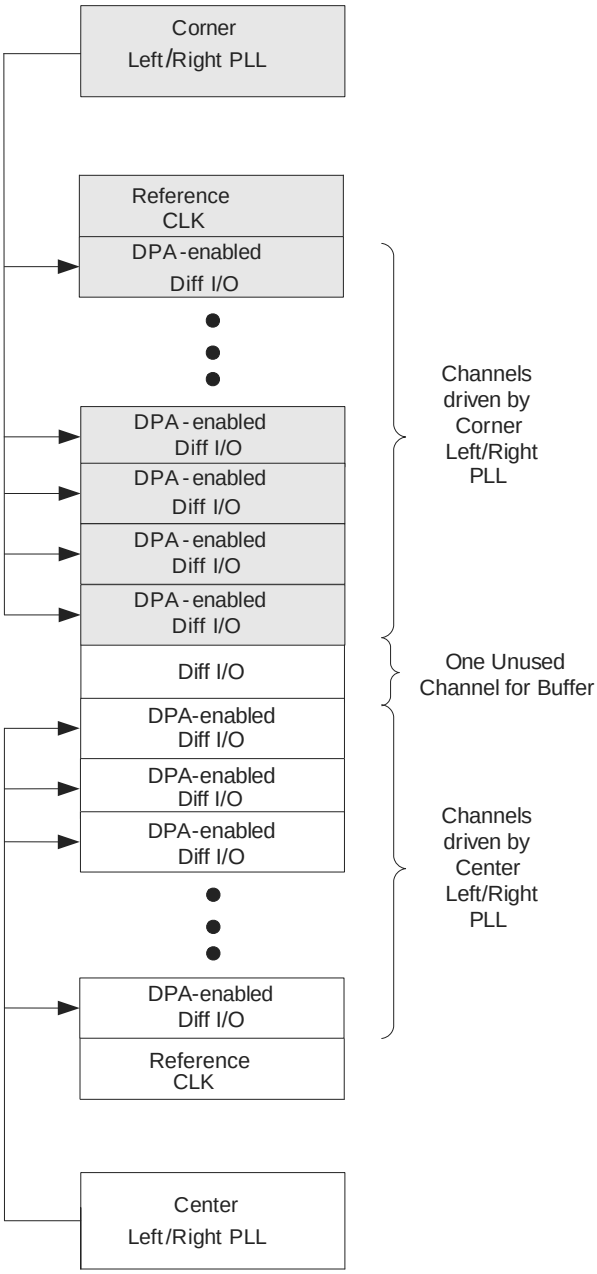


Table 11–13. Stratix III Configuration Pin Summary *(Note 1)* (Part 2 of 2)

Description	Input/Output	Dedicated	Powered By	Configuration Mode
MSEL[2..0]	Input	Yes	V_{CCPGM}	All modes

Notes to Table 11–13:

(1) The total number of pins is 30. The total number of dedicated pins is 19.

(2) The JTAG output pin TDO and all JTAG input pins are powered by the 2.5 V/3.0 V/3.3-V V_{CCPD} power supply of I/O bank 1A.

(3) These dual purpose pins are powered by V_{CCPGM} during configuration, then are powered by V_{CCIO} while in user mode.This applies for all configuration modes.

Table 11–14 describes the dedicated configuration pins, which are required to be connected properly on your board for successful configuration. Some of these pins may not be required for your configuration schemes.

Table 11–14. Dedicated Configuration Pins on the Stratix III Device (Part 1 of 5)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
VCCPGM	N/A	All	Power	Dedicated power pin. Use this pin to power all dedicated configuration inputs, dedicated configuration outputs, dedicated configuration bi-direction pins, and some of the dual functional pins that are used for configuration. You must connect this pin to 1.8-V, 2.5-V, 3.0-V, or 3.3-V. V_{CCPGM} must ramp-up from 0-V to 3.3-V within 100 ms. If V_{CCPGM} is not ramped up within this specified time, your Stratix III device will not configure successfully. If your system does not allow for a VCCPGM ramp-up time of 100 ms or less, you must hold nCONFIG low until all power supplies are stable.
VCCPD	N/A	All	Power	Dedicated power pin. Use this pin to power the I/O pre-drivers, the JTAG input and output pins, and the design security circuitry. You must connect this pin to 2.5-V, 3.0-V, or 3.3-V depending on the I/O standards selected. For 3.3-V I/O standards, VCCPD=3.3-V, for 3.0-V I/O standards, V_{CCPD} = 3.0 V, for 2.5-V or below I/O standards, V_{CCPD} = 2.5 V. V_{CCPD} must ramp-up from 0-V to 2.5-V / 3.0-V/3.3-V within 100 ms. If V_{CCPD} is not ramped up within this specified time, your Stratix III device will not configure successfully. If your system does not allow for a V_{CCPD} ramp-up time of 100 ms or less, you must hold nCONFIG low until all power supplies are stable.
PORSEL	N/A	All	Input	Dedicated input which selects either a POR time of 12 ms or 100 ms. A logic high (1.8 V, 2.5 V, 3.0 V, 3.3 V) selects a POR time of approximately 12 ms and a logic low selects a POR time of approximately 100 ms. The PORSEL input buffer is powered by VCCPGM and has an internal 5-kΩ pull-down resistor that is always active. You should tie the PORSEL pin directly to VCCPGM or GND.

12. Remote System Upgrades with Stratix III Devices

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This chapter describes the functionality and implementation of the dedicated remote system upgrade circuitry. It also defines several concepts related to remote system upgrade, including factory configuration, application configuration, remote update mode, and user watchdog timer. Additionally, this chapter provides design guidelines for implementing remote system upgrades with the supported configuration schemes.

System designers sometimes face challenges such as shortened design cycles, evolving standards, and system deployments in remote locations. Stratix® III devices help overcome these challenges with their inherent re-programmability and dedicated circuitry to perform remote system upgrades. Remote system upgrades help deliver feature enhancements and bug fixes without costly recalls, reduce time-to-market, and extend product life.

Stratix III devices feature dedicated remote system upgrade circuitry. Soft logic (either the Nios® II embedded processor or user logic) implemented in a Stratix III device can download a new configuration image from a remote location, store it in configuration memory, and direct the dedicated remote system upgrade circuitry to initiate a reconfiguration cycle. The dedicated circuitry performs error detection during and after the configuration process, recovers from any error condition by reverting back to a safe configuration image, and provides error status information. This dedicated remote system upgrade circuitry is unique to the Stratix series and helps to avoid system downtime.

Remote system upgrade is supported in fast active serial (FAS) Stratix III configuration schemes. You can also implement remote system upgrade in conjunction with advanced Stratix III features such as real-time decompression of configuration data and design security using the advanced encryption standard (AES) for secure and efficient field upgrades.

Functional Description

The dedicated remote system upgrade circuitry in Stratix III devices manage remote configuration and provides error detection, recovery, and status information. User logic or a Nios II processor implemented in the Stratix III device logic array provides access to the remote configuration data source and an interface to the system's configuration memory.

Stratix III devices have remote system upgrade processes that involves the following steps:

1. A Nios II processor (or user logic) implemented in the Stratix III device logic array receives new configuration data from a remote location. The connection to the remote source uses a communication protocol such as the transmission control protocol/Internet protocol (TCP/IP), peripheral component interconnect (PCI), user datagram protocol (UDP), universal asynchronous receiver/transmitter (UART), or a proprietary interface.
2. The Nios II processor (or user logic) stores this new configuration data in non-volatile configuration memory.