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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	5700
Number of Logic Elements/Cells	142500
Total RAM Bits	6543360
Number of I/O	744
Number of Gates	-
Voltage - Supply	0.86V ~ 1.15V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep3sl150f1152c2n

MultiTrack Interconnect

In the Stratix III architecture, connections between ALMs, TriMatrix memory, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive technology. The MultiTrack interconnect consists of continuous, performance-optimized row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities. The MultiTrack interconnect provides 1-hop connection to 34 adjacent LABs, 2-hop connections to 96 adjacent LABs and 3-hop connections to 160 adjacent LABs.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement in the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the reoptimization cycles that typically follow design changes and additions. The Quartus II Compiler also automatically places critical design paths on faster interconnects to improve design performance.

For more information, refer to the *MultiTrack Interconnect in Stratix III Devices* chapter.

TriMatrix Embedded Memory Blocks

TriMatrix embedded memory blocks provide three different sizes of embedded SRAM to efficiently address the needs of Stratix III FPGA designs. TriMatrix memory includes the following blocks:

- 320-bit MLAB blocks optimized to implement filter delay lines, small FIFO buffers, and shift registers
- 9-Kbit M9K blocks that can be used for general purpose memory applications
- 144-Kbit M144K blocks that are ideal for processor code storage, packet and video frame buffering

Each embedded memory block can be independently configured to be a single- or dual-port RAM, ROM, or shift register via the Quartus II MegaWizard™ Plug-In Manager. Multiple blocks of the same type can also be stitched together to produce larger memories with minimal timing penalty. TriMatrix memory provides up to 16,272 Kbits of embedded SRAM at up to 600 MHz operation.

For more information about TriMatrix memory blocks, modes, features, and design considerations, refer to the *TriMatrix Embedded Memory Blocks in Stratix III Devices* chapter.

DSP Blocks

Stratix III devices have dedicated high-performance digital signal processing (DSP) blocks optimized for DSP applications requiring high data throughput. Stratix III devices provide you with the ability to implement various high-performance DSP functions easily. Complex systems such as WiMAX, 3GPP WCDMA, CDMA2000, voice over Internet Protocol (VoIP), H.264 video compression, and high-definition television (HDTV) require high-performance DSP blocks to process data. These system designs typically use DSP blocks to implement finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, and discrete cosine transform (DCT) functions.

f For more information, refer to the Clock Networks and PLLs in Stratix III Devices chapter.

I/O Banks and I/O Structure

Stratix III devices contain up to 24 modular I/O banks, each of which contains 24, 32, 36, 40, or 48 I/Os. This modular bank structure improves pin efficiency and eases device migration. The I/O banks contain circuitry to support external memory interfaces at speeds up to 533 MHz and high-speed differential I/O interfaces meeting up to 1.6 Gbps performance. It also supports high-speed differential inputs and outputs running at speeds up to 800 MHz.

Stratix III devices support a wide range of industry I/O standards, including single-ended, voltage referenced single-ended, and differential I/O standards. The Stratix III I/O supports programmable bus hold, programmable pull-up resistor, programmable slew rate, programmable drive strength, programmable output delay control, and open-drain output. Stratix III devices also support on-chip series (R_S) and on-chip parallel (R_T) termination with auto calibration for single-ended I/O standards and on-chip differential termination (R_D) for LVDS I/O standards on Left/Right I/O banks. Dynamic OCT is also supported on bi-directional I/O pins in all I/O banks.

f For more information, refer to the Stratix III Device I/O Features chapter.

External Memory Interfaces

The Stratix III I/O structure has been completely redesigned to provide flexibility and enable high-performance support for existing and emerging external memory standards such as DDR, DDR2, DDR3, QDR II, QDR II+, and RLDRAM II at frequencies of up to 533 MHz.

Packed with features such as dynamic on-chip termination, trace mismatch compensation, read/write leveling, half-rate registers, and 4-to 36-bit programmable DQ group widths, Stratix III I/Os supply the built-in functionality required for rapid and robust implementation of external memory interfaces. Double data-rate support is found on all sides of the Stratix III device. Stratix III devices provide an efficient architecture to quickly and easily fit wide external memory interfaces exactly where you want them.

A self-calibrating soft IP core (ALTMEMPHY), optimized to take advantage of the Stratix III device I/O, along with the Quartus II timing analysis tool (TimeQuest), provide the total solution for the highest reliable frequency of operation across process voltage and temperature.

f For more information about external memory interfaces, refer to the External Memory Interfaces in Stratix III Devices chapter.

High-Speed Differential I/O Interfaces with DPA

Stratix III devices contain dedicated circuitry for supporting differential standards at speeds up to 1.6 Gbps. The high-speed differential I/O circuitry supports the following high-speed I/O interconnect standards and applications: Utopia IV, SPI-4.2, SFI-4, 10 Gigabit Ethernet XSBI, Rapid I/O, and NPSI. Stratix III devices support 2×,

Figure 4 3 shows an address clock enable block diagram. The address clock enable is referred to by the port name addressstall.

Figure 4–3. Stratix III Address Clock Enable Block Diagram

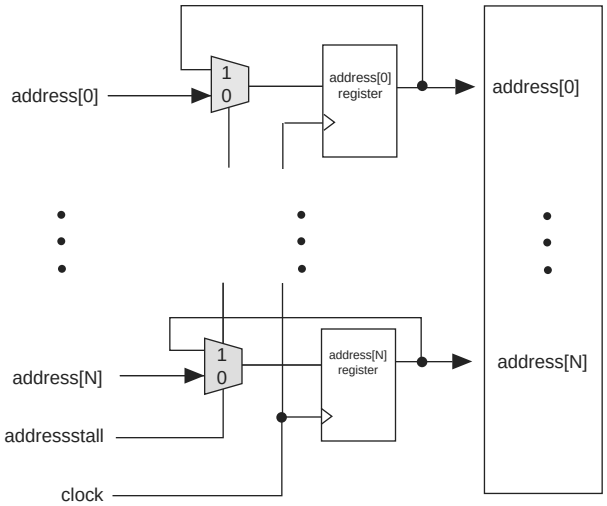


Figure 4 4 shows the address clock enable waveform during the read cycle.

Figure 4–4. Stratix III Address Clock Enable during Read Cycle Waveform

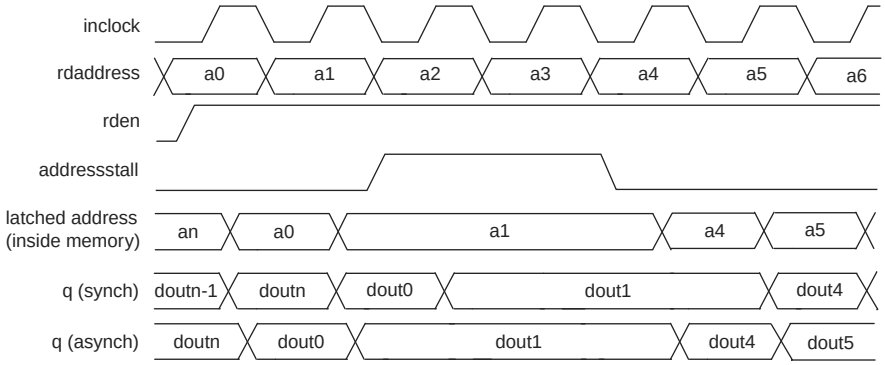
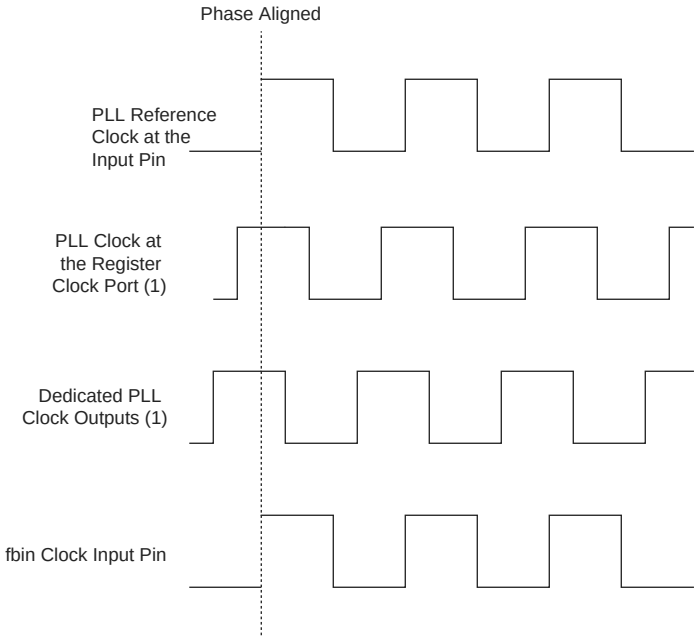


Figure 6 30 shows an example waveform of the phase relationship between PLL clocks in EFB mode.

Figure 6–30. Phase Relationship Between PLL Clocks in External-Feedback Mode



Note toFigure 6–30:

(1) The PLL clock outputs can lead or lag the fbin clock input.

Clock Multiplication and Division

Each Stratix III PLL provides clock synthesis for PLL output ports using m/(n* post-scale counter) scaling factors. The input clock is divided by a pre-scale factor, n, and is then multiplied by the m feedback factor. The control loop drives the VCO to match f_{in} (m/ n). Each output port has a unique post-scale counter that divides down the high-frequency VCO. For multiple PLL outputs with different frequencies, the VCO is set to the least common multiple of the output frequencies that meets its frequency specifications. For example, if output frequencies required from one PLL are 33 and 66 MHz, then the Quartus II software sets the VCO to 660 MHz (the least common multiple of 33 and 66 MHz within the VCO range). Then the post-scale counters scale down the VCO frequency for each output port.

Each PLL has one pre-scale counter, n, and one multiply counter,m, with a range of 1 to 512 for both m and n. The n counter does not use duty-cycle control because the only purpose of this counter is to calculate frequency division. There are seven generic post-scale counters per Left/Right PLL and ten post-scale counters per Top/Bottom PLL that can feed GCLKs, RCLKs, or external clock outputs. These post-scale counters range from 1 to 512 with a 50% duty cycle setting. The high- and low-count values for each counter range from 1 to 256. The sum of the high- and low-count values chosen for a design selects the divide value for a given counter.

The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered into the ALTPLL megafunction.

An optional INIT_DONE pin is available, which signals the end of initialization and the start of user-mode with a low-to-high transition. The Enable INIT_DONE Output option is available in the Quartus II software on the General tab of the Device and Pin Options dialog box. If you use the INIT_DONE pin, it will be high due to an external 10-k pull-up resistor when nCONFIG is low and during the beginning of configuration. When the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin will go low. When initialization is complete, the INIT_DONE pin will be released and pulled high. The MAX II device must be able to detect this low-to-high transition, which signals the device has entered user mode. When initialization is complete, the device enters user mode. In user mode, the user I/O pins will no longer have weak pull-up resistors and will function as assigned in your design.

To ensure DCLK and DATA0 are not left floating at the end of configuration, the MAX II device must drive them either high or low, whichever is convenient on your board. The DATA[0] pin is available as a user I/O pin after configuration. When you choose the PS scheme as a default in the Quartus II software, this I/O pin is tri-stated in user mode and should be driven by the MAX II device. To change this default option in the Quartus II software, click the Dual-Purpose Pins tab of the Device and Pin Options dialog box.

The configuration clock (DCLK) speed must be below the specified frequency to ensure correct configuration. No maximum DCLK period exists, which means you can pause configuration by halting DCLK for an indefinite amount of time.

If an error occurs during configuration, the device drives its nSTATUS pin low, resetting itself internally. The low signal on the nSTATUS pin also alerts the MAX II device that there is an error. If the Auto-restart configuration after error option (available in the Quartus II software on the General tab of the Device and Pin Options dialog box) is turned on, the Stratix III device releases nSTATUS after a reset time-out period (maximum of 100 µs). After nSTATUS is released and pulled high by a pull-up resistor, the MAX II device can attempt to reconfigure the target device without needing to pulse nCONFIG low. If this option is turned off, the MAX II device must generate a low-to-high transition (with a low pulse of at least 2 µs) on nCONFIG to restart the configuration process.

1 If you have enabled the Auto-restart configuration after error option, the nSTATUS pin transitions from high to low and back again to high when a configuration error is detected. This appears as a low pulse at the nSTATUS pin with a minimum pulse width of 10 µs to a maximum pulse width of 500 µs, as defined in the t_{STATUS} specification.

The MAX II device can also monitor the CONF_DONE and INIT_DONE pins to ensure successful configuration. The CONF_DONE pin must be monitored by the MAX II device to detect errors and determine when programming completes. If all configuration data is sent, but CONF_DONE or INIT_DONE have not gone high, the MAX II device must reconfigure the target device.

1 If you use the optional CLKUSR pin and nCONFIG is pulled low to restart configuration during device initialization, you must ensure that CLKUSR continues toggling during the time nSTATUS is low (maximum of 100 µs).

Recovering From CRC Errors

The system that contains the Stratix III device must control the device reconfiguration. After detecting an error on the CRC_ERROR pin, strobing the nCONFIG signal low directs the system to perform the reconfiguration at a time when it is safe for the system to reconfigure the device.

When the data bit is rewritten with the correct value by reconfiguring the device, the device functions correctly.

While soft errors are uncommon in Altera devices, certain high-reliability applications may require a design to account for these errors.

Chapter Revision History

Table 15 8 lists the revision history for this chapter.

Table 15 8. Chapter Revision History

Date	Version	Changes Made
March 2010	1.7	Updated for the Quartus II software version 9.1 SP2 release: Updated Table 15–6 Minor text edits.
May 2009	1.6	Updated “User Mode Error Detection” and “CRC_ERROR Pin” sections.
February 2009	1.5	Updated “Error Detection Timing” section. Removed “Referenced Documents”, Critical Error Detection”, and “CRITICAL ERROR Pin” sections.
October 2008	1.4	Updated “Introduction” and “Referenced Documents” sections. Updated New Document Format.
May 2008	1.3	Updated “Configuration Error Detection”, “User Mode Error Detection”, and “Error Detection Timing” sections. Updated Table 15–3, Table 15–6, and Table 15–7. Updated Figure 15–2 and Figure 15–3.
October 2007	1.2	Minor edits to Table 15–3. Added new section “Referenced Documents”. Added live links for references.
May 2007	1.1	Minor edits to page 2, 3, 4, and 14. Updated Table 15–5.
November 2006	1.0	Initial Release.