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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	5700
Number of Logic Elements/Cells	142500
Total RAM Bits	6543360
Number of I/O	744
Number of Gates	-
Voltage - Supply	0.86V ~ 1.15V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep3sl150f1152c4ln

Figure 4–3 shows an address clock enable block diagram. The address clock enable is referred to by the port name `addressstall`.

Figure 4–3. Stratix III Address Clock Enable Block Diagram

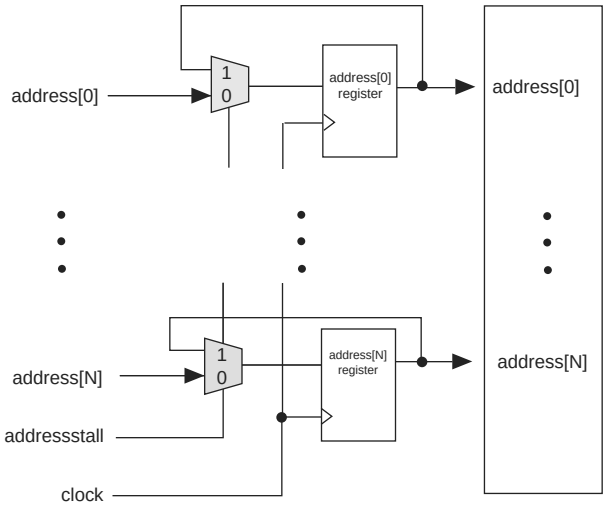


Figure 4–4 shows the address clock enable waveform during the read cycle.

Figure 4–4. Stratix III Address Clock Enable during Read Cycle Waveform

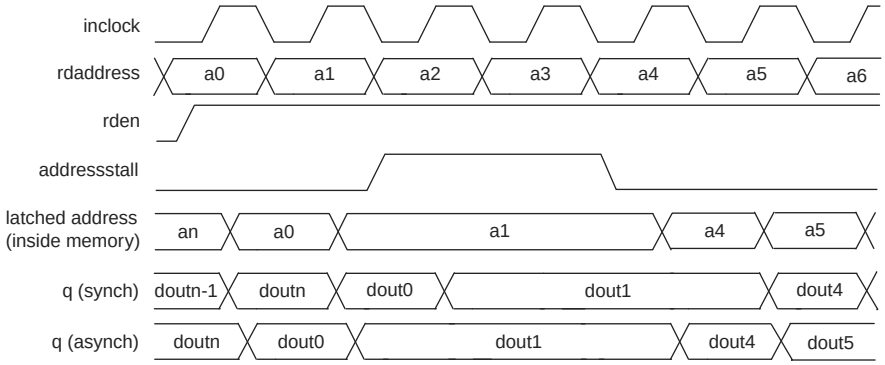
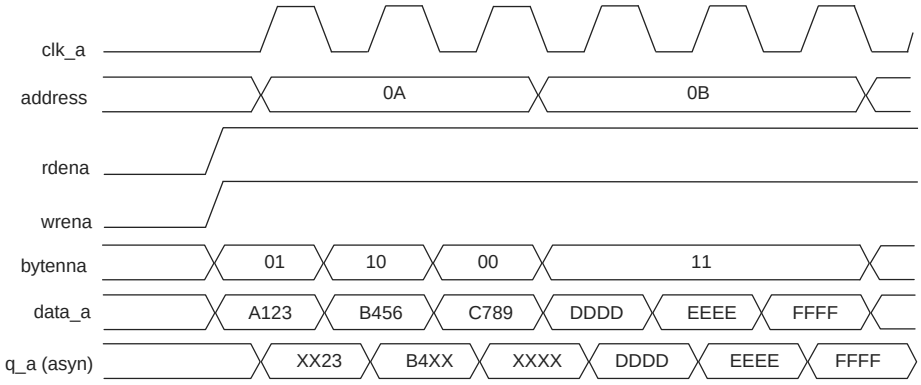


Figure 4–19 shows the sample functional waveforms of same-port read-during-write behavior with new data.

Figure 4–19. Same Port Read-During-Write: New Data Mode *(Note 1)*

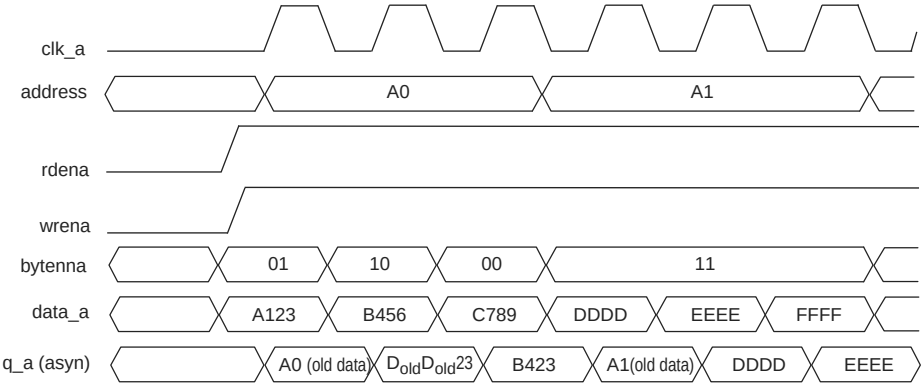


Note to Figure 4–19:

(1) "X" can be a don't care value or current data at that location, depending on the setting chosen in the Quartus II software.

Figure 4–20 shows the sample functional waveforms of same-port read-during-write behavior with old data mode.

Figure 4–20. Same Port Read-During-Write: Old Data Mode *(Note 1)*



Note to Figure 4–20:

(1) D_{old} is the old data bit at address A0, A0 (old data) is the old data at address A0, and A1 (old data) is the old data at address A1.

Mixed-Port Read-During-Write Mode

This mode applies to a RAM in simple or true dual-port mode which has one port reading and the other port writing to the same address location with the same clock.

In this mode you also have two output choices: old data or don't care. In old data mode, a read-during-write operation to different ports causes the RAM outputs to reflect the old data at that address location. In don't care mode, the same operation results in a "don't care" or "unknown" value on the RAM outputs.

Each Half Block has its own `signa` and `signb` signal. Therefore, all of the `data A` inputs feeding the same DSP Half Block must have the same sign representation. Similarly, all of the `data B` inputs feeding the same DSP Half Block must have the same sign representation. The multiplier offers full precision regardless of the sign representation in all operational modes except for full precision 18 x 18 loopback and Two-Multiplier Adder modes. Refer to "Two-Multiplier Adder Sum Mode" on page 5–21 for details.

☞ When the `signa` and `signb` signals are unused, the Quartus II software sets the multiplier to perform unsigned multiplication by default.

The outputs of the multipliers are the only outputs that can feed into the first-stage adder, as shown in Figure 5–6. There are four first-stage adders in a DSP block (two adders per half DSP block). The first-stage adder block has the ability to perform addition and subtraction. The control signal for addition or subtraction is static and has to be configured upon compile time. The first-stage adders are used by the sum modes to compute the sum of two multipliers, 18 × 18-complex multipliers, and to perform the first stage of a 36 × 36 multiply and shift operation.

Depending on your specifications, the output of the first-stage adder has the option to feed into the pipeline registers, second-stage adder, round and saturation unit, or the output registers.

Pipeline Register Stage

The output from the first-stage adder can either feed or bypass the pipeline registers, as shown in Figure 5–6. Pipeline registers increase the DSP block's maximum performance (at the expense of extra cycles of latency), especially when using the subsequent DSP block stages. Pipeline registers split up the long signal path between the input-registers/multiplier/first-stage adder and the second-stage adder/round-and-saturation/output-registers, creating two shorter paths.

Second-Stage Adder

There are four individual 44-bit second-stage adders per DSP block (2 adders per half DSP block). You can configure the second-stage adders as follows:

- The final stage of a 36-bit multiplier
- A sum of four (18 × 18)
- An accumulator (44-bits maximum)
- A chained output summation (44-bits maximum)

☞ The chained-output adder can be used at the same time as a second-level adder in chained output summation mode.

☞ The output of the second-stage adder has the option to go into the round and saturation logic unit or the output register.

☞ You cannot use the second-stage adder independently from the multiplier and first-stage adder.

18 × 18 Complex Multiply

You can configure the DSP block when used in Two-Multiplier Adder mode to implement complex multipliers using the two-multiplier adder mode. A single half DSP block can implement one 18-bit complex multiplier.

A complex multiplication can be written as shown in Equation 5–4.

Equation 5–4. Complex Multiplication Equation

$$(a + jb) \times (c + jd) = ((a \times c) - (b \times d)) + j((a \times d) + (b \times c))$$

To implement this complex multiplication within the DSP block, the real part ((a × c) – (b × d)) is implemented using two multipliers feeding one subtractor block while the imaginary part ((a × d) + (b × c)) is implemented using another two multipliers feeding an adder block. Figure 5–16 shows an 18-bit complex multiplication. This mode automatically assumes all inputs are using signed numbers.

Figure 5–16. Complex Multiplier Using Two-Multiplier Adder Mode

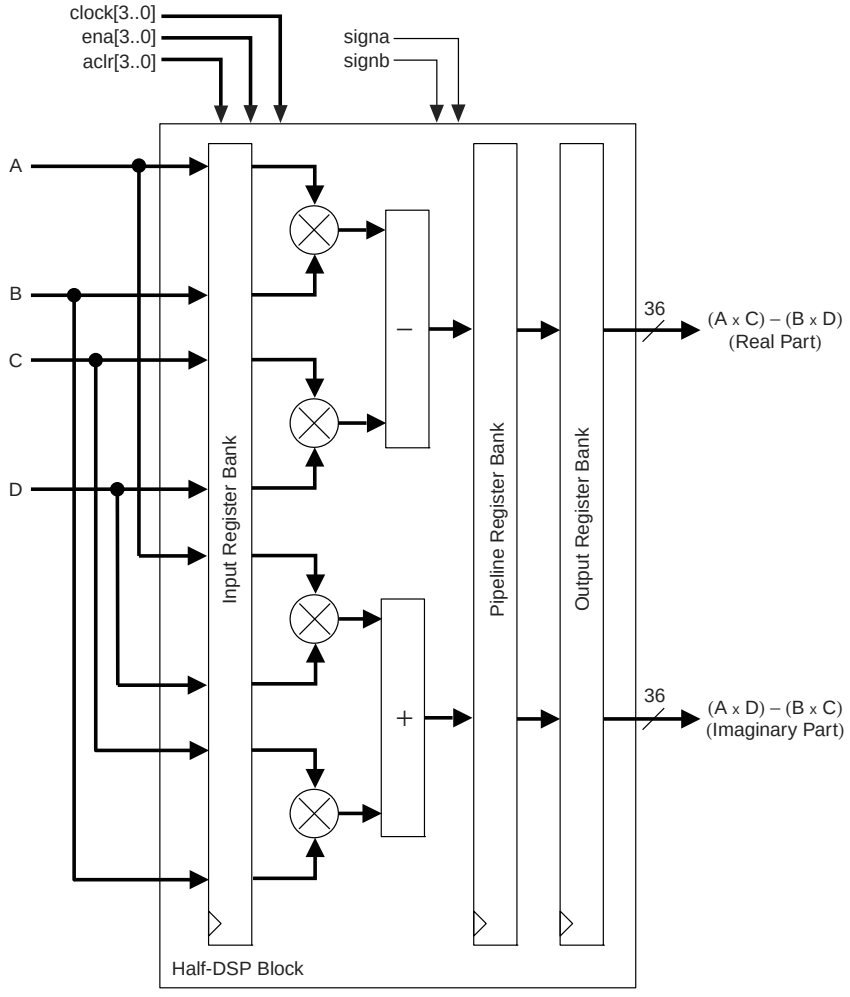
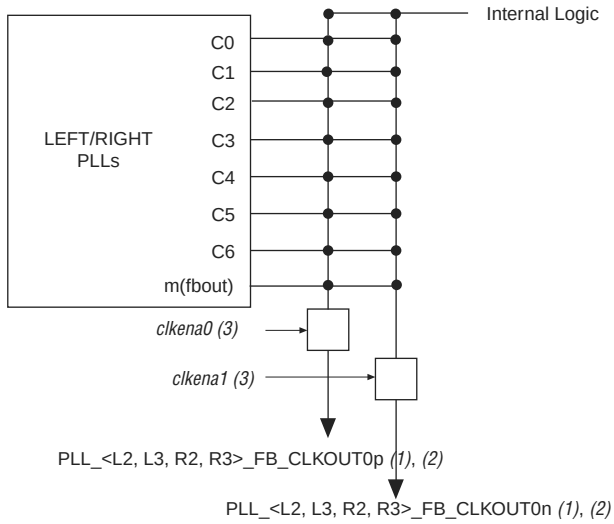


Figure 6–21. External Clock Outputs for Left/Right PLLs



Notes to Figure 6–21:

(1) These clock output pins can be fed by any one of the `C[6..0]`, m counters.

(2) The `CLKOUT0p` and `CLKOUT0n` pins are dual-purpose I/O pins that can be used as two single-ended outputs or one single-ended output and one external feedback input pin.

(3) These external clock enable signals are available only when using the ALTCLKCTRL megafunction.

Each pin of a single-ended output pair can either be in-phase or 180-degrees out-of-phase. The Quartus II software places the NOT gate in the design into the IOE to implement 180-degrees phase with respect to the other pin in the pair. The clock output pin pairs support the same I/O standards as standard output pins (in the top and bottom banks) as well as LVDS, LVPECL, differential HSTL, and differential SSTL.

To determine which I/O standards are supported by the PLL clock input and output pins, refer to the *Stratix III Device I/O Features* chapter.

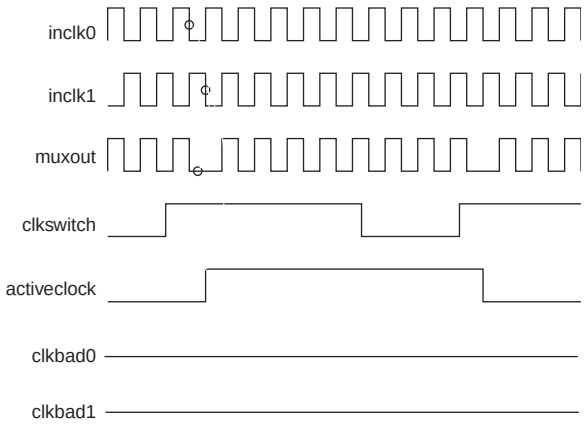
Stratix III PLLs can also drive out to any regular I/O pin through the global or regional clock network. You can use the external clock output pins as user I/O pins if external PLL clocking is not needed.

Manual Override

In the automatic switchover with manual override mode, you can use the clkswitch input for user- or system-controlled switch conditions. You can use this mode for same-frequency switchover or to switch between inputs of different frequencies. For example, if inclk0 is 66 MHz and inclk1 is 200 MHz, you must control the switchover using clkswitch because the automatic clock-sense circuitry cannot monitor clock input (inclk0, inclk1) frequencies with a frequency difference of more than 100% (2×). This feature is useful when the clock sources originate from multiple cards on the backplane, requiring a system-controlled switchover between the frequencies of operation. You should choose the backup clock frequency and set the m, n, c, and k counters accordingly so the VCO operates within the recommended operating frequency range of 600 to 1,300 MHz. The ALTPLL MegaWizard Plug-in Manager notifies users if a given combination of inclk0 and inclk1 frequencies cannot meet this requirement. In the Quartus II software, the VCO value reported is divided by the post scale counter (K).

Figure 6–34 shows an example of a waveform illustrating the switchover feature when controlled by clkswitch. In this case, both clock sources are functional and inclk0 is selected as the reference clock. clkswitch goes high, which starts the switchover sequence. On the falling edge of inclk0, the counter's reference clock, muxout, is gated off to prevent any clock glitching. On the falling edge of inclk1, the reference clock multiplexer switches from inclk0 to inclk1 as the PLL reference, and the activeclock signal changes to indicate which clock is currently feeding the PLL.

Figure 6–34. Clock Switchover Using the clkswitch (Manual) Control *(Note 1)*



Note to Figure 6–34:

(1) Both inclk0 and inclk1 must be running when the clkswitch signal goes high to initiate a manual clock switchover event.

In this mode, the activeclock signal mirrors the clkswitch signal. As both clocks are still functional during the manual switch, neither clkbad signal goes high. Since the switchover circuit is positive-edge sensitive, the falling edge of the clkswitch signal does not cause the circuit to switch back from inclk1 to inclk0. When the clkswitch signal goes high again, the process repeats. clkswitch and automatic switch only work if the clock being switched to is available. If the clock is not available, the state machine waits until the clock is available.

PLL Cascading and Clock Network Guidelines

When cascading PLLs in Stratix III devices, the source (upstream) PLL must have a low-bandwidth setting while the destination (downstream) PLL must have a high-bandwidth setting. There must be no overlap of the bandwidth ranges of the two PLLs.

To ensure that the memory interface's PLL is configured correctly in the external memory interface design, the following settings are required:

- The PLL used to generate the memory output clock signals and write data/clock signals must be set to **No compensation** mode to minimize output clock jitter.
- The reference input clock signal to the PLL must be driven by the dedicated clock input pin located adjacent to the PLL, or from the clock output signal from the adjacent PLL. To minimize output clock jitter, the reference input clock pin must not be routed through the core using global or regional clock networks. If reference clock is cascaded from another PLL, that upstream PLL must be configured in **No compensation** mode and **Low bandwidth** mode.

Spread-Spectrum Tracking

Stratix III devices can accept a spread-spectrum input with typical modulation frequencies. However, the device cannot automatically detect that the input is a spread-spectrum signal. Instead, the input signal looks like deterministic jitter at the input of PLL. Stratix III PLLs can track a spread-spectrum input clock as long as it is within the input-jitter tolerance specifications and the modulation frequency of the input clock is below the PLL bandwidth which is specified in the fitter report. Stratix III devices cannot internally generate spread-spectrum clocks.

PLL Specifications

For information about PLL timing specifications, refer to the *DC and Switching Characteristics of Stratix III Devices* chapter.

Section II. I/O Interfaces

This section provides information on Stratix® III device I/O features, external memory interfaces, and high-speed differential interfaces with DPA. This section includes the following chapters:

- Chapter 7, Stratix III Device I/O Features
- Chapter 8, External Memory Interfaces in Stratix III Devices
- Chapter 9, High-Speed Differential I/O Interfaces and DPA in Stratix III Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

Table 7–2. I/O Standards and Voltage Levels for Stratix III Devices *(Note 1)*, *(3)* (Part 3 of 3)

I/O Standard	Standard Support	V_{CCIO} (V)				V_{CCPD} (V) (Pre-Driver Voltage)	V_{REF} (V) (Input Ref Voltage)	V_{TT} (V) (Board Termination Voltage)
		Input Operation		Output Operation				
		Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks			
LVPECL	—	*(4)*	*(4)*	—	—	2.5	—	—

Notes to Table 7–2:

(1) V_{CCPD} is either 2.5 V, 3.0 V, or 3.3 V. For V_{CCIO} = 3.3 V, V_{CCPD}=3.3 V. For V_{CCIO} = 3.0 V, V_{CCPD} = 3.0 V. For V_{CCIO} = 2.5 V or less, V_{CCPD} = 2.5 V.

(2) Single-ended HSTL/SSTL, differential SSTL/HSTL, and LVDS input buffers are powered by V_{CCPD}.

(3) $V_{CCCLKIN}$ powers the Column I/O bank dedicated clock input pins when configured as differential inputs. Clock input pins on the Column I/O banks use V_{CCIO} when configured as single-ended inputs.

(4) Column and row I/O banks support LVPECL I/O standards for input operation only on dedicated clock input pins. Clock inputs on column I/O are powered by $V_{CCCLKIN}$ when configured as differential clock input. Differential clock inputs in row I/O are powered by V_{CCPD}.

(5) Row I/O banks support LVDS outputs using a dedicated output buffer. Column and row I/O banks support emulated LVDS outputs using two single-ended output buffers and external one-resistor (LVDS_E_1R) and a three-resistor (LVDS_E_3R) network.

(6) Row I/O banks support RSDS and mini-LVDS I/O standards using a true LVDS output buffer without a resistor network.

(7) Column and row I/O banks support emulated-RSDS and mini-LVDS I/O standards using two single-ended output buffers with one-resistor (RSDS_E_1R and mini-LVDS_E_1R) and three-resistor (RSDS_E_3R and mini-LVDS_E_3R) networks.

(8) The emulated differential output standard that supports the tri-state feature includes: LVDS_E_1R, LVDS_E_3R, RSDS_E_1R, RSDS_E_3R, Mini_LVDS_E_1R, and Mini_LVDS_E_3R.

For detailed electrical characteristics of each I/O standard, refer to the *DC and Switching Characteristics of Stratix III Devices* chapter.

Stratix III I/O Banks

Stratix III devices contain up to 24 I/O banks, as shown in Figure 7–1. The row I/O banks contain true differential input and output buffers and dedicated circuitry to support differential standards at speeds up to 1.6 Gbps.

Every I/O bank in Stratix III devices can support high-performance external memory interfaces with dedicated circuitry. The I/O pins are organized in pairs to support differential standards. Each I/O pin pair can support both differential input and output buffers. The only exceptions are the `CLK[1, 3, 8, 10][p, n]`, `PLL_L[1, 4]_CLK[p, n]`, and `PLL_R[1, 4]_CLK[p, n]` pins, which support differential or single-ended input operations, these pins do not support output operations.

Pins that do not support output operations do not support the programmable current strength, programmable slew rate, programmable pull-up, bus hold, open-drain, or on-chip series termination (OCT R_S) options.

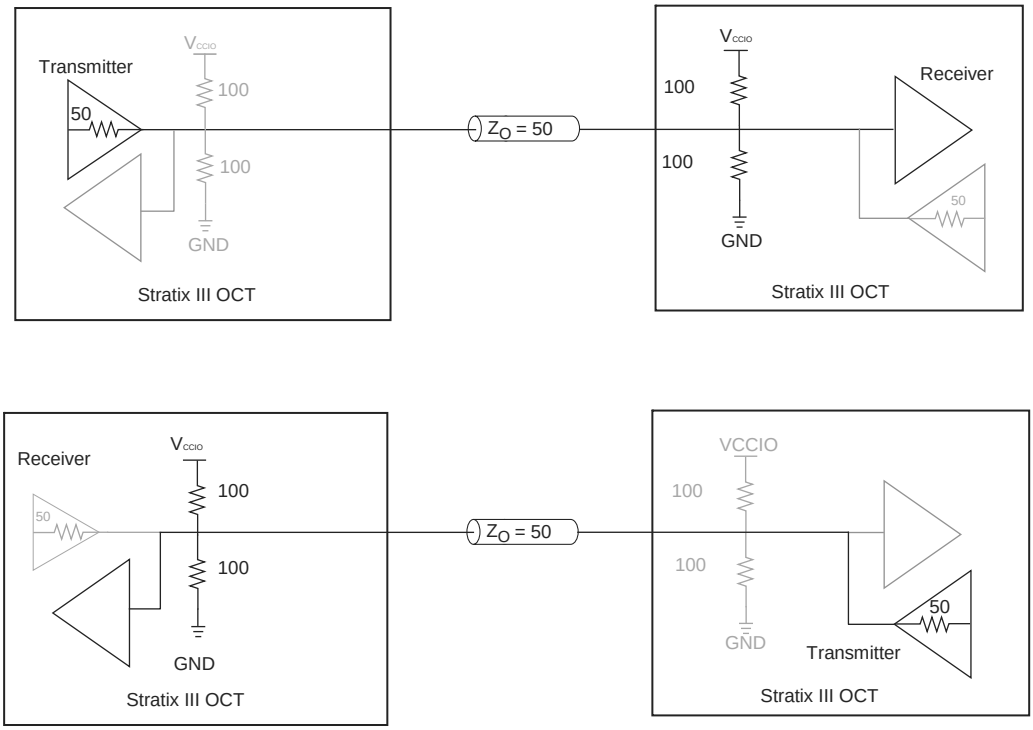
For the number of channels available for the LVDS I/O standard, refer to the *High-Speed Differential I/O Interface with DPA in Stratix III Devices* chapter.

Dynamic OCT

Stratix III devices support on-off dynamic series and parallel termination for a bi-directional I/O in all I/O banks. Figure 7–11 shows the termination schemes supported in the Stratix III device. Dynamic parallel termination is enabled only when the bi-directional I/O acts as a receiver and is disabled when it acts as a driver. Similarly, dynamic series termination is enabled only when the bi-directional I/O acts as a driver and is disabled when it acts as a receiver. This feature is useful for terminating any high-performance bi-directional path because the signal integrity is optimized depending on the direction of the data.

You should connect a bi-directional pin that uses both 25-Ω or 50-Ω series termination and 50-Ω input termination to a calibration block that has a 50-Ω external resistor connected to its RUP and RDN pins. The 25-Ω series termination on the bi-directional pin is achieved through internal divide by two circuits.

Figure 7–11. Dynamic Parallel OCT in Stratix III Devices



For more information about tolerance specifications for OCT with calibration, refer to the *DC and Switching Characteristics of Stratix III Devices* chapter.

Chapter Revision History

Table 7–13 lists the revision history for this chapter.

Table 7–13. Chapter Revision History (Part 1 of 2)

Date and Revision	Version	Changes Made
July 2010	1.9	■ Updated Figure 7–25, Figure 7–26, and Figure 7–28. ■ Updated Equation 7–1 and Equation 7–2.
March 2010	1.8	Updated for the Quartus II software version 9.1 SP2 release: ■ Updated "Programmable Pull-Up Resistor" section. ■ Updated Figure 7–2, Figure 7–3, Figure 7–4, Figure 7–5, Figure 7–6. ■ Updated Table 7–2, Table 7–3, and Table 7–7. ■ Added reference before Table 7–11. ■ Removed "Conclusion" section. ■ Minor text edit.
May 2009	1.7	■ Updated "Expanded On-Chip Series Termination with Calibration" and "Mixing Voltage-Referenced and Non-Voltage-Referenced Standards" sections. ■ Added "Left Shift Series Termination Control" section. ■ Updated Table 7–8 and Table 7–9. ■ Updated Figure 7–24.
February 2009	1.6	■ Updated Table 7–3, Table 7–7, Table 7–8, and Table 7–11. ■ Updated Figure 7–2, Figure 7–3, Figure 7–4, Figure 7–5, and Figure 7–6. ■ Updated "LVDS Input On-Chip Termination (R_D)" section. ■ Removed "Referenced Documents" section.
October 2008	1.5	Text, Table, and Figure updates: ■ Updated Table 7–2, Table 7–4, Table 7–7, and Table 7–10. ■ Updated notes for Table 7–2. ■ Updated notes for Figure 7–3, Figure 7–4, Figure 7–5, Figure 7–6, and Figure 7–7. ■ Updated "Stratix III I/O Banks", "Modular I/O Banks", "High-Speed Differential I/O with DPA Support", "Dynamic On-Chip Termination", "LVDS Input On-Chip Termination (RD)", "Serial Data Transfer", "LVDS", "RSDS", "mini-LVDS", "Voltage-Referenced Standards", "Stratix III I/O Banks", "MultiVolt I/O Interface", and "On-Chip Parallel Termination with Calibration" sections. ■ Updated Figure 7–1. ■ Added Table 7–3. ■ Updated New Document Format.

When using the Altera memory controller MegaCore® functions, the PHY is instantiated for you.

The ALTMEMPHY megafunction and the Altera memory controller MegaCore functions can run at half the frequency of the I/O interface of the memory devices to allow better timing management in high-speed memory interfaces. Stratix III devices have built-in registers to convert data from full-rate (I/O frequency) to half-rate (controller frequency) and vice versa. You can bypass these registers if your memory controller is not running at half the rate of the I/O frequency.

DQS Phase-Shift Circuitry

Stratix III phase-shift circuitry provides phase shift to the DQS and CQn pins on read transactions, when the DQS/CQ and CQn pins are acting as input clocks or strobes to the FPGA. DQS phase-shift circuitry consists of DLLs that are shared between multiple DQS pins and the phase-offset module to further fine-tune the DQS phase shift for different sides of the device. Figure 8–10 shows how the DQS phase-shift circuitry is connected to the DQS/CQ and CQn pins in the device.

Table 8–9. DLL Reference Clock Input for EP3SL200, EP3SE260 and EP3SL340 Devices *(Note 1)*, *(2)*

DLL	CLKIN (Top/Bottom)	CLKIN (Left/Right)	PLL (Top/Bottom)	PLL (Left/Right)
DLL0	CLK12P CLK13P CLK14P CLK15P	CLK0P CLK1P CLK2P CLK3P	PLL_T1	PLL_L1 PLL_L2
DLL1	CLK4P CLK5P CLK6P CLK7P	CLK0P CLK1P CLK2P CLK3P	PLL_B1	PLL_L3 PLL_L4
DLL2	CLK4P CLK5P CLK6P CLK7P	CLK8P CLK9P CLK10P CLK11P	PLL_B2	PLL_R3 PLL_R4
DLL3	CLK12P CLK13P CLK14P CLK15P	CLK8P CLK9P CLK10P CLK11P	PLL_T2	PLL_R1 PLL_R2

Notes to Table 8–9:

(1) PLLs L1, L3, L4, B2, R1, R3, R4, and T2 are not available for the EP3SL200 H780 package.

(2) PLLs L1, L4, R1 and R4 are not available for the EP3SL200 F1152 package.

Figure 8–12 shows a simple block diagram of the DLL. The input reference clock goes into the DLL to a chain of up to 16 delay elements. The phase comparator compares the signal coming out of the end of the delay chain block to the input reference clock. The phase comparator then issues the upndn signal to the Gray-code counter. This signal increments or decrements a 6-bit delay setting (DQS delay settings) that increases or decreases the delay through the delay element chain to bring the input reference clock and the signals coming out of the delay element chain in phase.

The POR circuit does not monitor the power supplies listed in Table 10–3.

Table 10–3. Power Supplies That Are Not Monitored by the POR Circuitry

Voltage Supply	Description	Setting (V)
V_{CCIO}	I/O power supply	1.2, 1.5, 1.8, 2.5, 3.0, 3.3
V_{CCA_PLL}	PLL analog global power supply	2.5
V_{CCD_PLL}	PLL digital power supply	1.1
V_{CC_CLKIN}	PLL differential clock input power supply (top and bottom I/O banks only)	2.5
V_{CCBAT}	Battery back-up power supply for design security volatile key storage	1.0 – 3.3 *(1)*

Note to Table 10–3:

(1) The nominal voltage for V_{CCBAT} is 3.0-V.

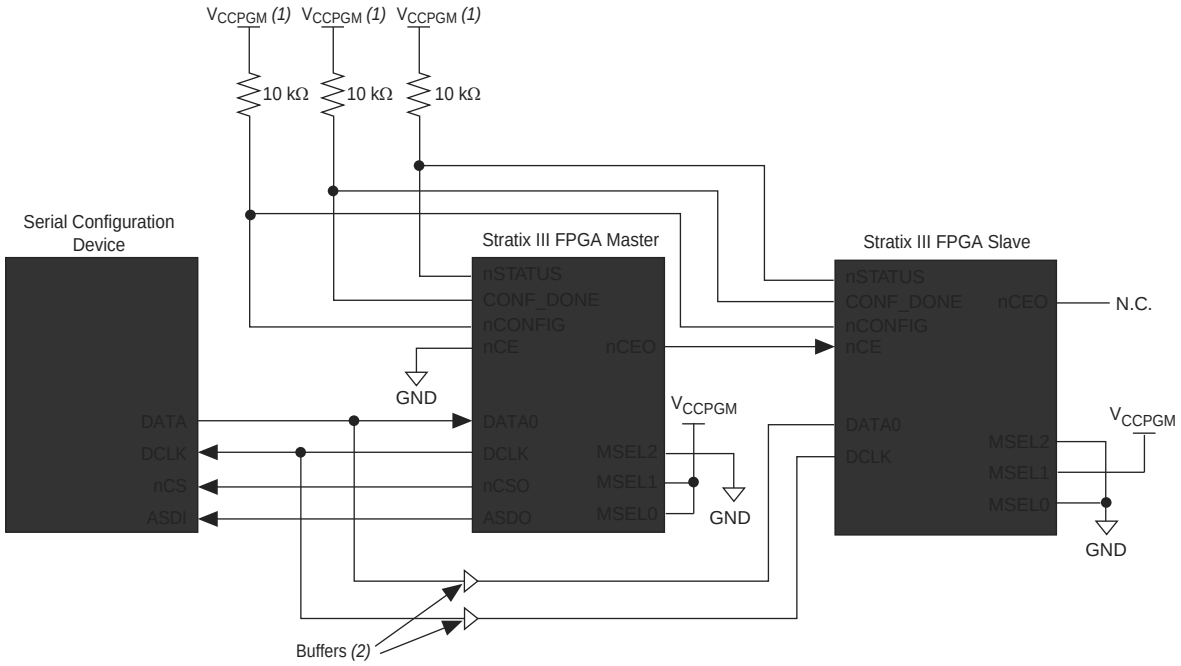
During power up, all power supplies listed in Table 10–2 and Table 10–3 are required to monotonically reach their full-rail values within t_{RAMP}.

The POR specification is designed to ensure that all the circuits in the Stratix III device are at certain known states during power up.

The POR signal pulse width is programmable using the PORSEL input pin. When PORSEL is set to low, the POR signal pulse width is set to 100 ms. A POR pulse width of 100 ms allows serial flash devices with 65 ms to 100 ms internal POR delay to be powered up and ready to receive the nSTATUS signal from Stratix III. When the PORSEL is set to high, the POR signal pulse width is set to 12 ms. A POR pulse width of 12 ms allows time for power supplies to ramp-up to full rail.

For more information about the POR specification, refer to the *DC and Switching Characteristics* chapter.

Figure 11–9. Multi-Device Fast AS Configuration



Notes to Figure 11–9:

(1) Connect the pull-up resistors to V_{CCPGM} at 3.3-V supply.

(2) Connect the repeater buffers between the Stratix III master and slave device(s) for DATA[0] and DCLK. This prevents any potential signal integrity and clock skew problems.

As shown in Figure 11–9, the nSTATUS and CONF_DONE pins on all target devices are connected with external pull-up resistors. These pins are open-drain bi-directional pins on the devices. When the first device asserts nCEO (after receiving all of its configuration data), it releases its CONF_DONE pin. The subsequent devices in the chain keep this shared CONF_DONE line low until they have received their configuration data. When all target devices in the chain have received their configuration data and released CONF_DONE, the pull-up resistor drives a high level on this line and all devices simultaneously enter initialization mode.

If an error occurs at any point during configuration, the nSTATUS line is driven low by the failing device. If you enable the **Auto-restart configuration after error** option, reconfiguration of the entire chain begins after a reset time-out period (maximum of 100 µs). If the **Auto-restart configuration after error** option is turned off, the external system must monitor nSTATUS for errors and then pulse nCONFIG low to restart configuration. The external system can pulse nCONFIG if it is under system control rather than tied to V_{CCPGM}.

☞ If you have enabled the **Auto-restart configuration after error** option, the nSTATUS pin transitions from high to low and back again to high when a configuration error is detected. This appears as a low pulse at the nSTATUS pin with a minimum pulse width of 10 µs to a maximum pulse width of 500 µs, as defined in the t_{STATUS} specification.

☞ While you can cascade Stratix III devices, you cannot cascade or chain together serial configuration devices.

For more information about programming serial configuration devices and fast AS Configuration Timing, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS16, EPCS64, and EPCS128) Data Sheet* in the *Configuration Handbook*.

Passive Serial Configuration

You can program PS configuration of Stratix III devices using an intelligent host, such as a MAX II device or microprocessor with flash memory, or a download cable. In the PS scheme, an external host (a MAX II device, embedded processor, or host PC) controls configuration. Configuration data is clocked into the target Stratix III device by using the DATA0 pin at each rising edge of DCLK.

The Stratix III decompression and design security features are fully available when configuring your Stratix III device using PS mode.

Table 11–9 lists the MSEL pin settings when using the PS configuration scheme.

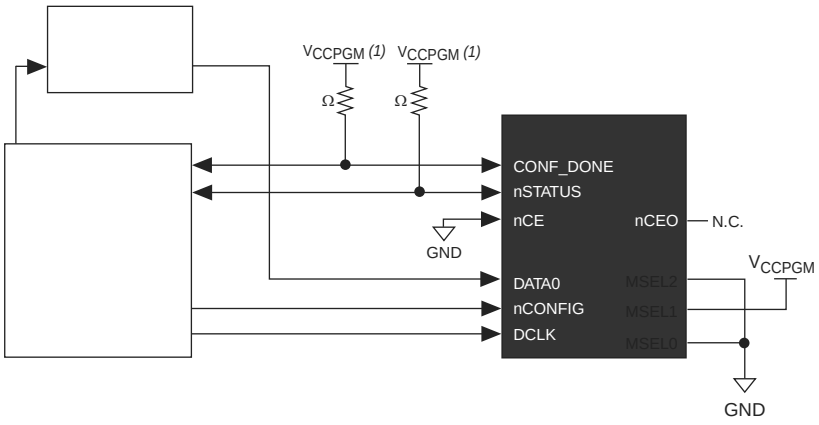
Table 11–9. Stratix III MSEL Pin Settings for PS Configuration Scheme

Configuration Scheme	MSEL2	MSEL1	MSEL0
PS	0	1	0

PS Configuration Using a MAX II Device as an External Host

In this configuration scheme, you can use a MAX II device as an intelligent host that controls the transfer of configuration data from a storage device, such as flash memory, to the target Stratix III device. You can store configuration data in **.rbf**, **.hex**, or **.ttf** format. Figure 11–13 shows the configuration interface connections between a Stratix III device and a MAX II device for single device configuration.

Figure 11–13. Single Device PS Configuration Using an External Host



Note to Figure 11–13:

(1) Connect the resistor to a supply that provides an acceptable input signal for the Stratix III device. V_{CCPGM} must be high enough to meet the V_{IH} specification of the I/O on the external host. It is recommended to power up all configuration systems' I/O with V_{CCPGM}.

Stratix III devices have dedicated JTAG pins that always function as JTAG pins. Not only can you perform JTAG testing on Stratix III devices before and after, but also during configuration. While other device families do not support JTAG testing during configuration, Stratix III devices support the bypass, id code, and sample instructions during configuration without interrupting configuration. All other JTAG instructions may only be issued by first interrupting configuration and reprogramming I/O pins using the CONFIG_IO instruction.

The CONFIG_IO instruction allows I/O buffers to be configured by using the JTAG port and when issued, interrupts configuration. This instruction allows you to perform board-level testing prior to configuring the Stratix III device or waiting for a configuration device to complete configuration. When configuration has been interrupted and JTAG testing is complete, you must reconfigure the part by using JTAG (PULSE_CONFIG instruction) or by pulsing nCONFIG low.

The chip-wide reset (DEV_CLRn) and chip-wide output enable (DEV_OE) pins on Stratix III devices do not affect JTAG boundary-scan or programming operations. Toggling these pins does not affect JTAG operations (other than the usual boundary-scan operation).

When designing a board for JTAG configuration of Stratix III devices, consider the dedicated configuration pins. Table 11–12 lists how these pins should be connected during JTAG configuration.

Table 11–12. Dedicated Configuration Pin Connections During JTAG Configuration

Signal	Description
nCE	On all Stratix III devices in the chain, nCE should be driven low by connecting it to ground, pulling it low by using a resistor, or driving it by some control circuitry. For devices that are also in multi-device FPP, AS, or PS configuration chains, the nCE pins should be connected to GND during JTAG configuration or JTAG configured in the same order as the configuration chain.
nCEO	On all Stratix III devices in the chain, you can leave nCEO floating or connected to the nCE of the next device.
MSEL	These pins must not be left floating. These pins support whichever non-JTAG configuration is used in production. If you only use JTAG configuration, tie these pins to ground.
nCONFIG	Driven high by connecting to V_{CCPGM}, pull up by using a resistor, or driven high by some control circuitry.
nSTATUS	Pull to V_{CCPGM} by using a 10-kΩ resistor. When configuring multiple devices in the same JTAG chain, each nSTATUS pin should be pulled up to V_{CCPGM} individually.
CONF_DONE	Pull to V_{CCPGM} by using a 10-kΩ resistor. When configuring multiple devices in the same JTAG chain, each CONF_DONE pin should be pulled up to V_{CCPGM} individually. CONF_DONE going high at the end of JTAG configuration indicates successful configuration.
DCLK	Should not be left floating. Drive low or high, whichever is more convenient on your board.

When programming a JTAG device chain, one JTAG-compatible header is connected to several devices. The number of devices in the JTAG chain is limited only by the drive capability of the download cable. When four or more devices are connected in a JTAG chain, Altera recommends buffering the TCK, TDI, and TMS pins with an on-board buffer.

JTAG-chain device programming is ideal when the system contains multiple devices, or when testing your system using JTAG BST circuitry. Figure 11–20 shows multi-device JTAG configuration.

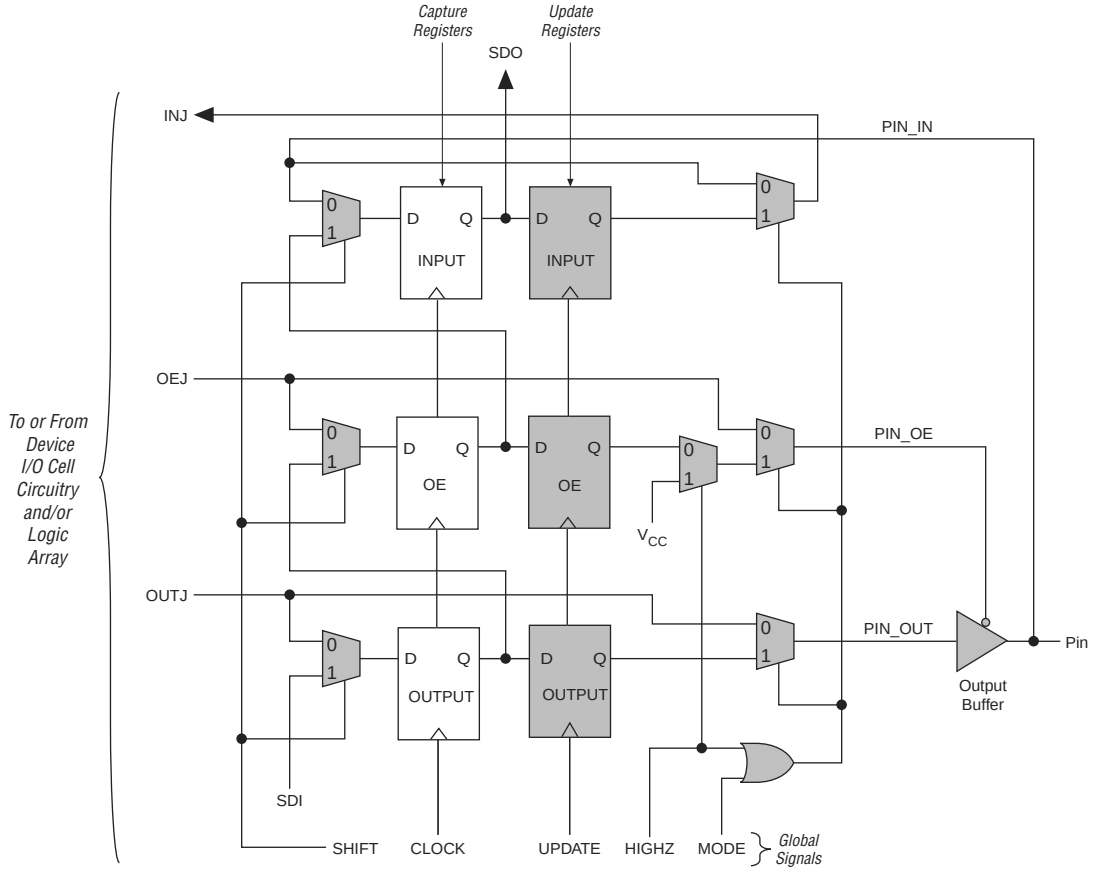
Boundary-Scan Cells of a Stratix III Device I/O Pin

The Stratix III device three-bit boundary-scan cell (BSC) consists of a set of capture registers and a set of update registers. The capture registers can connect to internal device data through the `OUTJ`, `OEJ`, and `PIN_IN` signals, while the update registers connect to external data through the `PIN_OUT` and `PIN_OE` signals.

The global control signals for the IEEE Std. 1149.1 BST registers (such as `shift`, `clock`, and `update`) are generated internally by the TAP controller. The `MODE` signal is generated by a decode of the instruction register. The `HIGHZ` signal is high when executing the `HIGHZ` instruction. The data signal path for the boundary-scan register runs from the serial data in (`SDI`) signal to the serial data out (`SDO`) signal. The scan register begins at the `TDI` pin and ends at the `TDO` pin of the device.

Figure 13–4 shows the Stratix III device's user I/O boundary-scan cell.

Figure 13–4. Stratix III Device's User I/O BSC with IEEE Std. 1149.1 BST Circuitry



During the SHIFT_IR state, an instruction code is entered by shifting data on the TDI pin on the rising edge of TCK. The last bit of the instruction code is clocked at the same time that the next state, EXIT1_IR, is activated. Set TMS high to activate the EXIT1_IR state. After the EXIT1_IR state is activated, TDO becomes tri-stated again. TDO is always tri-stated except in the SHIFT_IR and SHIFT_DR states. After an instruction code is entered correctly, the TAP controller advances to serially shift test data in one of three modes.

The three serially shift test data instruction modes are discussed in the following sections:

- "SAMPLE/PRELOAD Instruction Mode" on page 13–11
- "EXTEST Instruction Mode" on page 13–13
- "BYPASS Instruction Mode" on page 13–15

Recovering From CRC Errors

The system that contains the Stratix III device must control the device reconfiguration. After detecting an error on the CRC_ERROR pin, strobing the nCONFIG signal low directs the system to perform the reconfiguration at a time when it is safe for the system to reconfigure the device.

When the data bit is rewritten with the correct value by reconfiguring the device, the device functions correctly.

While soft errors are uncommon in Altera devices, certain high-reliability applications may require a design to account for these errors.

Chapter Revision History

Table 15–8 lists the revision history for this chapter.

Table 15–8. Chapter Revision History

Date	Version	Changes Made
March 2010	1.7	Updated for the Quartus II software version 9.1 SP2 release: ■ Updated Table 15–6. ■ Minor text edits.
May 2009	1.6	Updated "User Mode Error Detection" and "CRC_ERROR Pin" sections.
February 2009	1.5	■ Updated "Error Detection Timing" section. ■ Removed "Referenced Documents", Critical Error Detection", and "CRITICAL ERROR Pin" sections.
October 2008	1.4	■ Updated "Introduction" and "Referenced Documents" sections. ■ Updated New Document Format.
May 2008	1.3	■ Updated "Configuration Error Detection", "User Mode Error Detection", and "Error Detection Timing" sections. ■ Updated Table 15–3, Table 15–6, and Table 15–7. ■ Updated Figure 15–2 and Figure 15–3.
October 2007	1.2	■ Minor edits to Table 15–3. ■ Added new section "Referenced Documents". ■ Added live links for references.
May 2007	1.1	■ Minor edits to page 2, 3, 4, and 14. ■ Updated Table 15–5.
November 2006	1.0	Initial Release.