Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

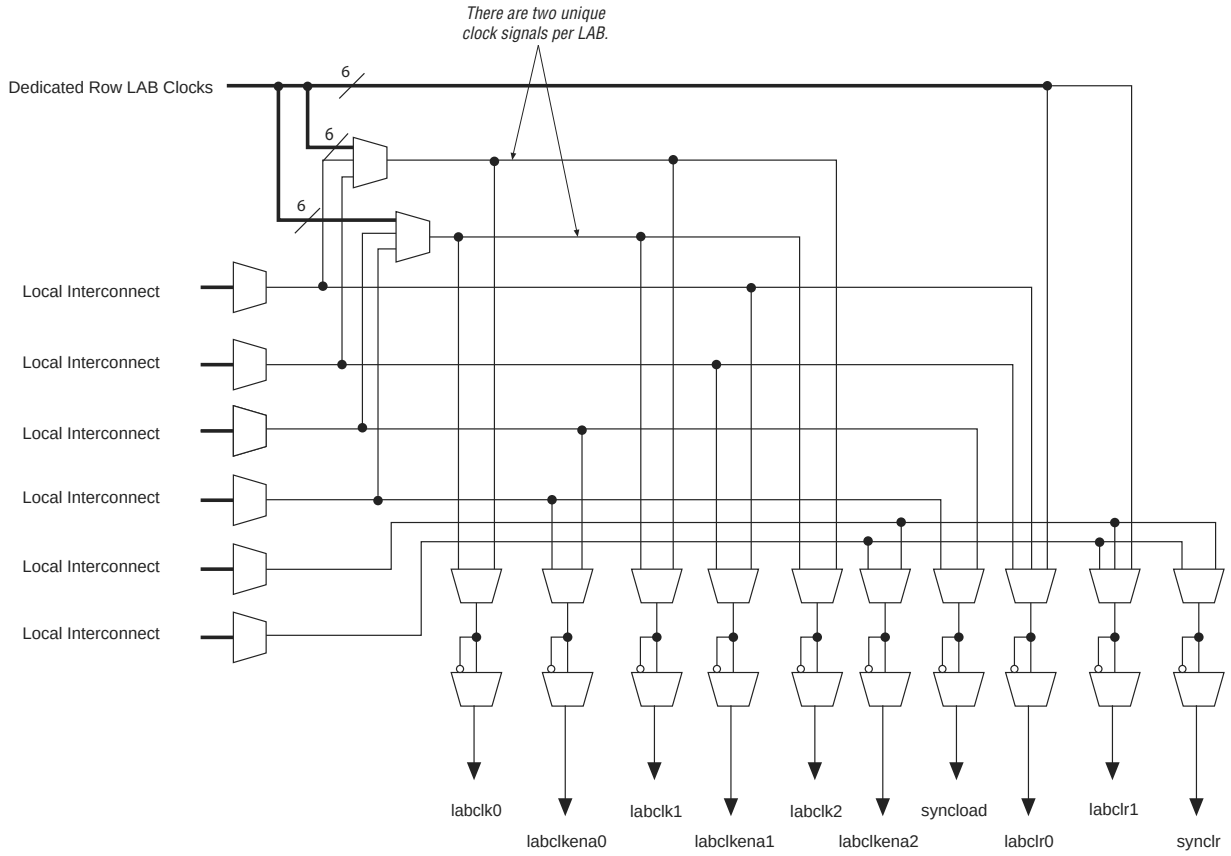
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	5700
Number of Logic Elements/Cells	142500
Total RAM Bits	6543360
Number of I/O	744
Number of Gates	-
Voltage - Supply	0.86V ~ 1.15V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep3sl150f1152c4n

- Selectable Core Voltage, available in low-voltage devices (L ordering code suffix), enables selection of lowest power or highest performance operation
- Up to 16 global clocks, 88 regional clocks, and 116 peripheral clocks per device
- Up to 12 phase-locked loops (PLLs) per device that support PLL reconfiguration, clock switchover, programmable bandwidth, clock synthesis, and dynamic phase shifting
- Memory interface support with dedicated DQS logic on all I/O banks
- Support for high-speed external memory interfaces including DDR, DDR2, DDR3 SDRAM, RLDRAM II, QDR II, and QDR II+ SRAM on up to 24 modular I/O banks
- Up to 1,104 user I/O pins arranged in 24 modular I/O banks that support a wide range of industry I/O standards
- Dynamic On-Chip Termination (OCT) with auto calibration support on all I/O banks
- High-speed differential I/O support with serializer/deserializer (SERDES) and dynamic phase alignment (DPA) circuitry for 1.6 Gbps performance
- Support for high-speed networking and communications bus standards including SPI-4.2, SFI-4, SGMII, Utopia IV, 10 Gigabit Ethernet XSBI, Rapid I/O, and NPSI
- The only high-density, high-performance FPGA with support for 256-bit AES volatile and non-volatile security key to protect designs
- Robust on-chip hot socketing and power sequencing support
- Integrated cyclical redundancy check (CRC) for configuration memory error detection with critical error determination for high availability systems support
- Built-in error correction coding (ECC) circuitry to detect and correct data errors in M144K TriMatrix memory blocks
- Nios® II embedded processor support
- Support for multiple intellectual property megafunctions from Altera® MegaCore® functions and Altera Megafunction Partners Program (AMPP℠)

Figure 2–4. LAB-Wide Control Signals

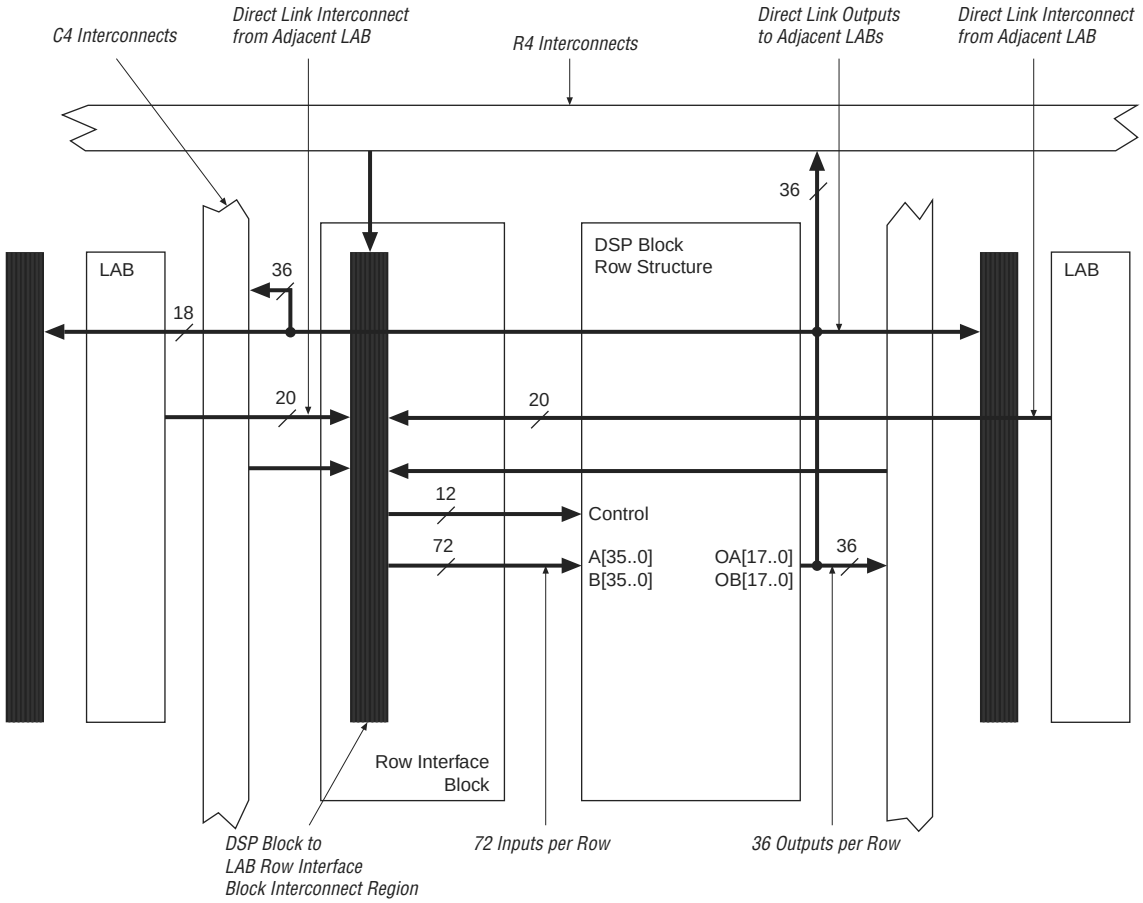


Adaptive Logic Modules

The basic building block of logic in the Stratix III architecture, the adaptive logic module (ALM), provides advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two combinational adaptive LUTs (ALUTs) and two registers. With up to eight inputs to the two combinational ALUTs, one ALM can implement various combinations of two functions. This adaptability allows an ALM to be completely backward-compatible with four-input LUT architectures. One ALM can also implement any function of up to six inputs and certain seven-input functions.

In addition to the adaptive LUT-based resources, each ALM contains two programmable registers, two dedicated full adders, a carry chain, a shared arithmetic chain, and a register chain. Through these dedicated resources, an ALM can efficiently implement various arithmetic functions and shift registers. Each ALM drives all types of interconnects: local, row, column, carry chain, shared arithmetic chain, register chain, and direct link interconnects. Figure 2–5 shows a high-level block diagram of the Stratix III ALM while Figure 2–6 shows a detailed view of all the connections in an ALM.

Figure 3–8. Detailed View, DSP Block Interface to Interconnect



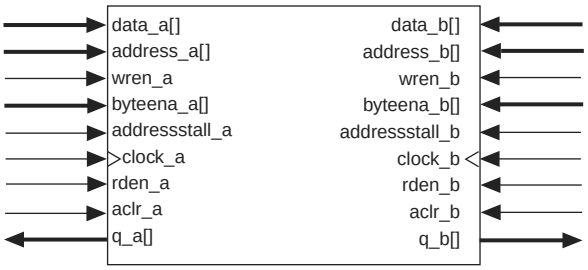
I/O Block Connections to Interconnect

The IOEs are located in I/O blocks around the periphery of the Stratix III device. There are up to four IOEs per row I/O block and four IOEs per column I/O block. The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects. Figure 3–9 shows how a row I/O block connects to the logic array. Figure 3–10 shows how a column I/O block connects to the logic array.

True Dual-Port Mode

Stratix III M9K and M144K blocks support true dual-port mode. Sometimes called bi-directional dual-port, this mode allows you to perform any combination of two port operations: two reads, two writes, or one read and one write at two different clock frequencies. Figure 4–15 shows the true dual-port RAM configuration.

Figure 4–15. Stratix III True Dual-Port Memory *(Note 1)*



Note to Figure 4–15:

(1) True dual-port memory supports input/output clock mode in addition to the independent clock mode shown.

The widest bit configuration of the M9K and M144K blocks in true dual-port mode is as follows:

- 512 × 16-bit (×18-bit with parity) (M9K)
- 4K × 32-bit (×36-bit with parity) (M144K)

Wider configurations are unavailable because the number of output drivers is equivalent to the maximum bit width of the respective memory block. Because true dual-port RAM has outputs on two ports, its maximum width equals half of the total number of output drivers. Table 4–7 lists the possible M9K block mixed-port width configurations in true dual-port mode.

Table 4–7. Stratix III M9K Block Mixed-Width Configuration (True Dual-Port Mode)

Read Port	Write Port						
	8K×1	4K×2	2K×4	1K×8	512×16	1K×9	512×18
8K×1	✓	✓	✓	✓	✓	—	—
4K×2	✓	✓	✓	✓	✓	—	—
2K×4	✓	✓	✓	✓	✓	—	—
1K×8	✓	✓	✓	✓	✓	—	—
512×16	✓	✓	✓	✓	✓	—	—
1K×9	—	—	—	—	—	✓	✓
512×18	—	—	—	—	—	✓	✓

Operational Modes Overview

Each Stratix III DSP block can be used in one of five basic operational modes. Table 5–2 lists the five basic operational modes and the number of multipliers that can be implemented within a single DSP block, depending on the mode.

Table 5–2. Stratix III DSP Block Operation Modes

Mode	Multiplier in Width	# of Mults	# per Block	Signed or Unsigned	RND, SAT	In Shift Register	Chainout Adder	1st Stage Add/Sub	2nd Stage Add/Acc
Independent Multiplier	9-bits	1	8	Both	No	No	No	—	—
	12-bits	1	6	Both	No	No	No	—	—
	18-bits	1	4	Both	Yes	Yes	No	—	—
	36-bits	1	2	Both	No	No	No	—	—
	Double	1	2	Both	No	No	No	—	—
Two-Multiplier Adder *(1)*	18-bits	2	4	Signed *(4)*	Yes	No	No	Both	—
Four-Multiplier Adder	18-bits	4	2	Both	Yes	Yes	Yes	Both	Add Only
High Precision Multiplier Adder	18 × 36-bits	2	2	Both	No	No	No	—	Add Only
Multiply Accumulate	18-bits	4	2	Both	Yes	Yes	Yes	Both	Both
Shift *(2)*	36-bits *(3)*	1	2	Both	No	No	—	—	—

Notes to Table 5–2:

(1) This mode also supports the loopback mode. In loopback mode, the number of loopback multipliers per DSP block is two and the remaining multipliers can be used in regular Two-Multiplier Adder mode.

(2) The dynamic shift mode supports arithmetic shift left, arithmetic shift right, logical shift left, logical shift right, and rotation operation.

(3) The dynamic shift mode operates on a 32-bit input vector but the multiplier width is configured as 36-bits.

(4) Unsigned value is also supported but you must make sure that the result can be contained within 36-bits.

The DSP block consists of two identical halves (top-half and bottom-half). Each half has four 18 × 18 multipliers.

The Quartus® II software includes megafunctions used to control the mode of operation of the multipliers. After making the appropriate parameter settings using the megafunction's MegaWizard™ Plug-In Manager, the Quartus II software automatically configures the DSP block.

Stratix III DSP blocks can operate in different modes simultaneously. Each half-block is fully independent except for the sharing of the four `clock`, `ena`, and `aclr` signals. For example, you can break down a single DSP block to operate a 9 × 9 multiplier in one Half-Block and an 18 × 18 two-multiplier adder in the other Half-Block. This increases DSP block resource efficiency and allows you to implement more multipliers within a Stratix III device. The Quartus II software automatically places multipliers that can share the same DSP block resources within the same block.

Figure 5–14. Two-Multiplier Adder Mode for Half-DSP Block

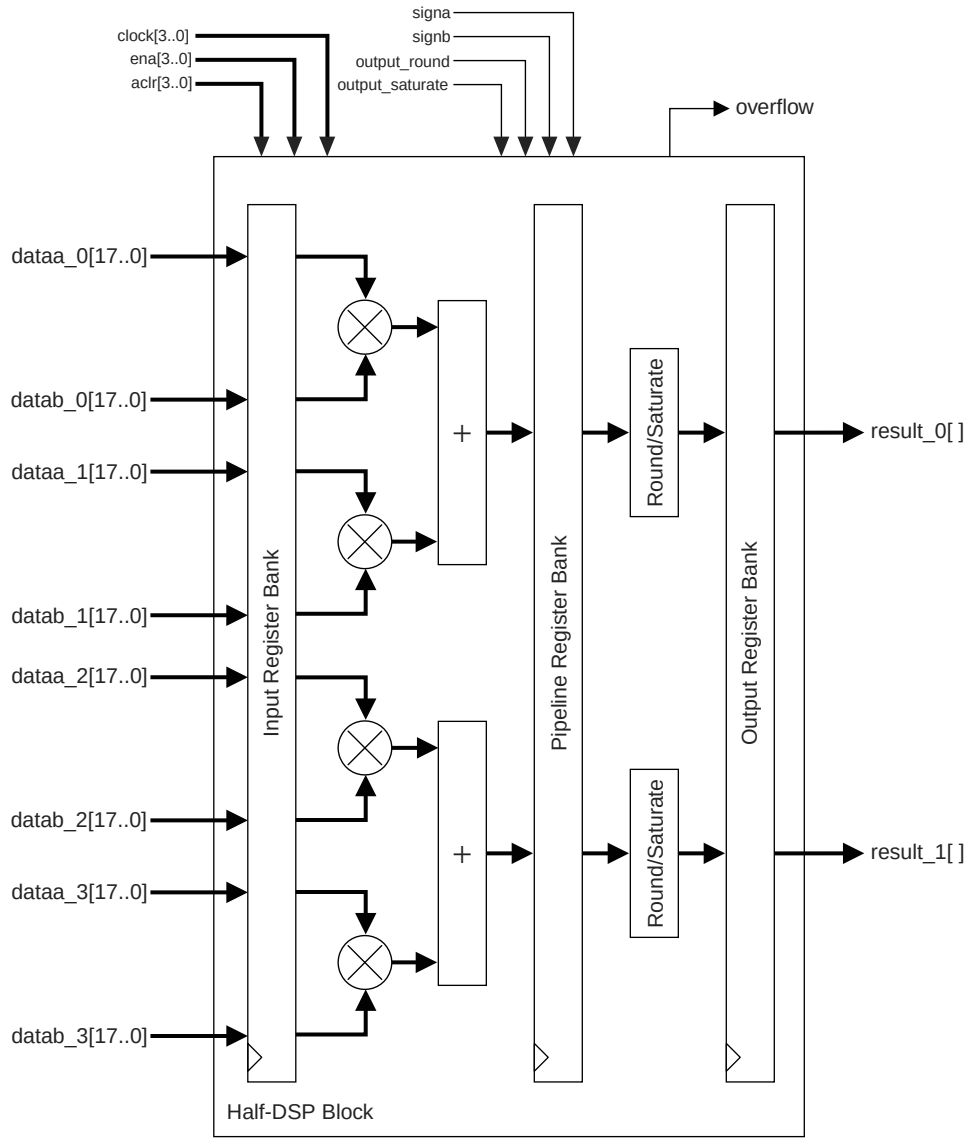


Table 6–7. Stratix III Device PLLs and PLL Clock Pin Drivers (Part 2 of 2) *(Note 1)*

Dedicated Clock Input Pin (CLKp/n pins)	PLL Number											
	L1	L2	L3	L4	B1	B2	R1	R2	R3	R4	T1	T2
CLK13	—	—	—	—	—	—	—	—	—	—	✓	✓
CLK14	—	—	—	—	—	—	—	—	—	—	✓	✓
CLK15	—	—	—	—	—	—	—	—	—	—	✓	✓
PLL_L1_CLKp *(2)*	✓	—	—	—	—	—	—	—	—	—	—	—
PLL_L1_CLKn *(2),(3)*	✓	—	—	—	—	—	—	—	—	—	—	—
PLL_L4_CLKp *(2)*	—	—	—	✓	—	—	—	—	—	—	—	—
PLL_L4_CLKn *(2),(3)*	—	—	—	✓	—	—	—	—	—	—	—	—
PLL_R1_CLKp *(2)*	—	—	—	—	—	—	✓	—	—	—	—	—
PLL_R1_CLKn *(2),(3)*	—	—	—	—	—	—	✓	—	—	—	—	—
PLL_R4_CLKp *(2)*	—	—	—	—	—	—	—	—	—	✓	—	—
PLL_R4_CLKn *(2),(3)*	—	—	—	—	—	—	—	—	—	✓	—	—

Notes to Table 6–7:

(1) For compensated PLLs input, only the dedicated CLK pins in the same I/O bank as the PLL used are compensated inputs.

(2) If both PLL_<L1/L4/R1/R4>_CLKp and PLL_<L1/L4/R1/R4>_CLKn pins are not used as a pair of differential clock pins, they can be used independently as single-ended clock input pins.

(3) For single-ended clock input, CLKn pins use the global network to drive the PLLs.

Clock Output Connections

PLLs in Stratix III devices can drive up to 20 regional clock networks and four global clock networks. Refer to Table 6–8 for Stratix III PLL connectivity to GCLK networks. The Quartus II software automatically assigns PLL clock outputs to regional or global clock networks.

Table 6–8 lists how the PLL clock outputs connect to GCLK networks.

Table 6–8. PLL Connectivity to GCLKs on Stratix III Devices (Part 1 of 2) *(Note 1)*

Clock Network	PLL Number											
	L1	L2	L3	L4	B1	B2	R1	R2	R3	R4	T1	T2
GCLK0	✓	✓	✓	✓	—	—	—	—	—	—	—	—
GCLK1	✓	✓	✓	✓	—	—	—	—	—	—	—	—
GCLK2	✓	✓	✓	✓	—	—	—	—	—	—	—	—
GCLK3	✓	✓	✓	✓	—	—	—	—	—	—	—	—
GCLK4	—	—	—	—	✓	✓	—	—	—	—	—	—
GCLK5	—	—	—	—	✓	✓	—	—	—	—	—	—
GCLK6	—	—	—	—	✓	✓	—	—	—	—	—	—
GCLK7	—	—	—	—	✓	✓	—	—	—	—	—	—
GCLK8	—	—	—	—	—	—	✓	✓	✓	✓	—	—
GCLK9	—	—	—	—	—	—	✓	✓	✓	✓	—	—
GCLK10	—	—	—	—	—	—	✓	✓	✓	✓	—	—
GCLK11	—	—	—	—	—	—	✓	✓	✓	✓	—	—

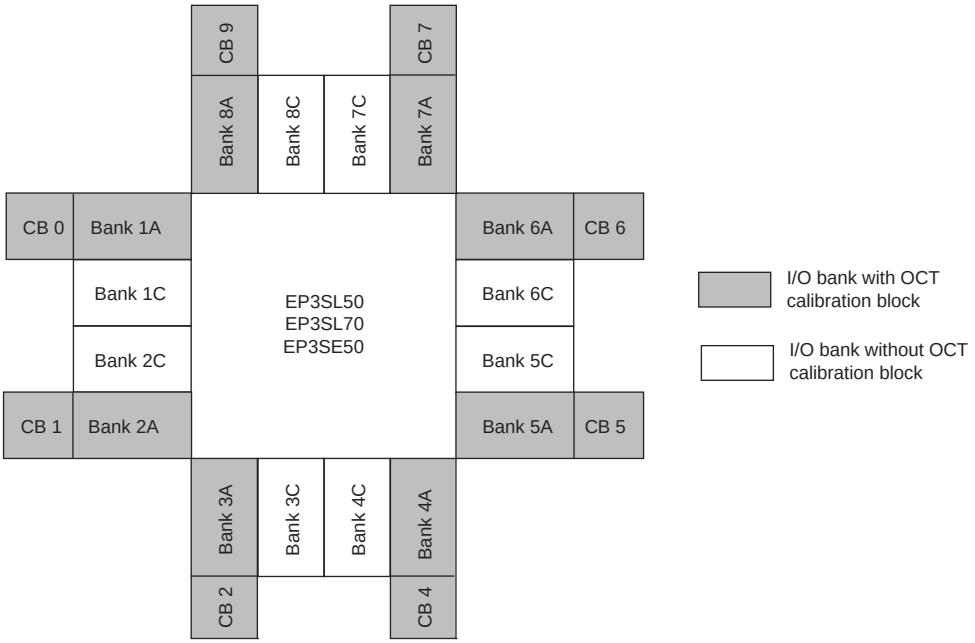
OCT Calibration

Stratix III devices support calibrated OCT R_S and calibrated OCT R_T on all I/O pins. You can calibrate the Stratix III I/O bank with any of eight OCT calibration blocks in EP3SL50, EP3SL70, EP3SL110, EP3SL150, EP3SE50, EP3SE80, and EP3SE110 devices and ten OCT calibration blocks in EP3SL200, EP3SE260, and EP3SL340 devices.

OCT Calibration Block Location

Figure 7–13, Figure 7–14, and Figure 7–15 show the location of OCT calibration blocks in Stratix III devices.

Figure 7–13. OCT Calibration Block (CB) Location in EP3SL50, EP3SL70, and EP3SE50 Devices *(Note 1)*



Note to Figure 7–13:

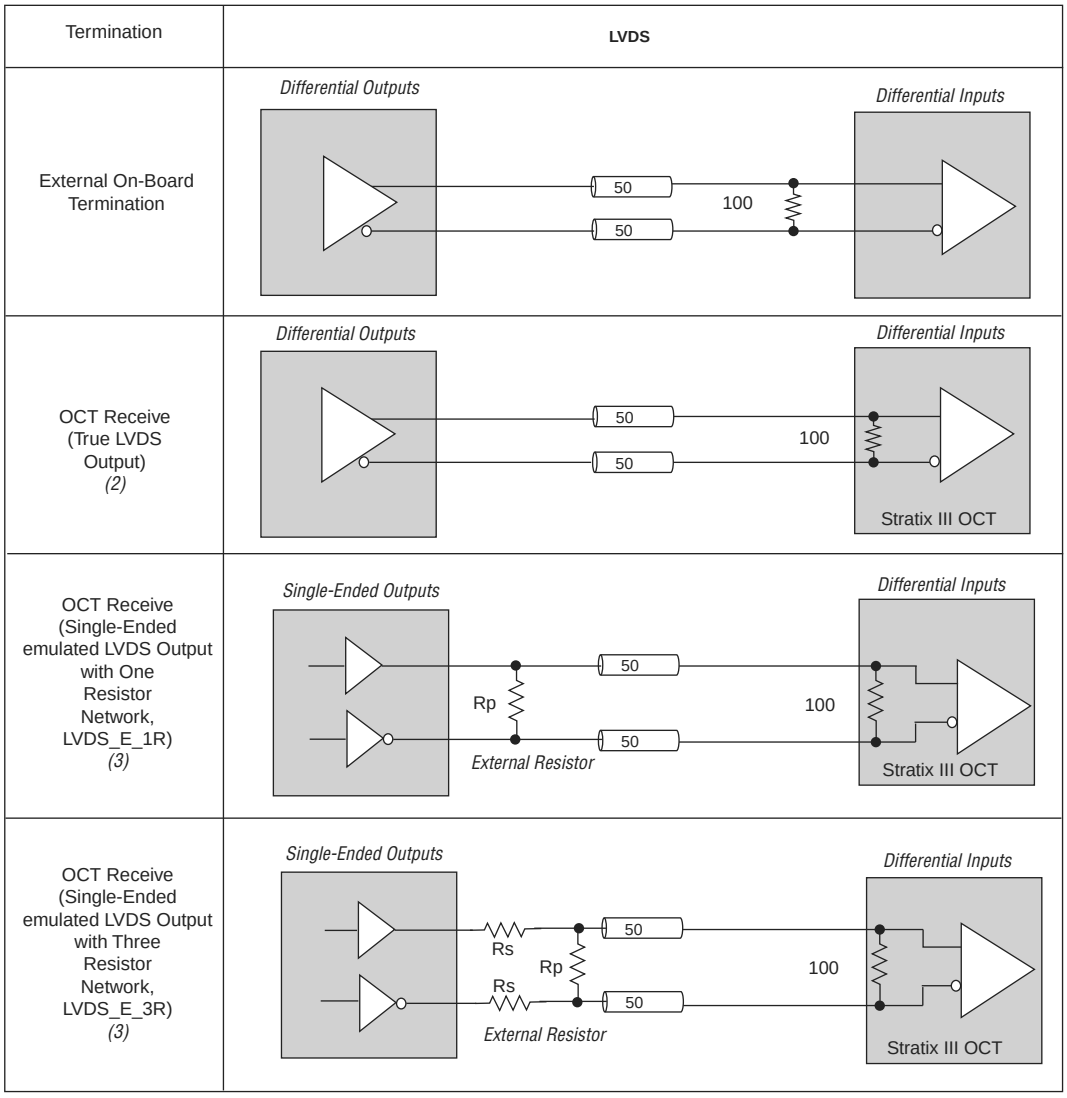
(1) Figure 7–13 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

LVDS

The LVDS I/O standard is a differential high-speed, low-voltage swing, low-power, general-purpose I/O interface standard. In Stratix III devices, the LVDS I/O standard requires a 2.5-V V_{CCIO} level. The LVDS input buffer requires 2.5-V V_{CCPD}. Use this standard in applications requiring high-bandwidth data transfer, backplane drivers, and clock distribution. LVDS requires a 100-Ω termination resistor between the two signals at the input buffer. Stratix III devices provide an optional 100-Ω differential termination resistor in the device using on-chip differential termination.

Figure 7–24 shows the details of LVDS termination. The OCT R_D is only available in row I/O banks.

Figure 7–24. LVDS I/O Standard Termination for Stratix III Devices *(Note 1)*



Notes to Figure 7–24:

(1) R_P=120 Ω for LVDS_E_1R, R_P=170 Ω and R_S=120 Ω for LVDS_E_3R.

(2) Row I/O banks support true LVDS output buffers.

(3) Column and row I/O banks support LVDS_E_1R and LVDS_E_3R I/O standards using two single-ended output buffers.

Voltage-Referenced Standards

To accommodate voltage-referenced I/O standards, each Stratix III device I/O bank has one VREF pin feeding a common V_{REF} bus. If it is not used as a VREF pin, it cannot be used as a generic I/O pin and should be tied to V_{CCIO} or GND. Each bank can only have a single V_{CCIO} voltage level and a single V_{REF} voltage level at a given time.

An I/O bank featuring single-ended or differential standards can support voltage-referenced standards as long as all voltage-referenced standards use the same V_{REF} setting.

For performance reasons, voltage-referenced input standards use their own V_{CCPD} level as the power source. This feature allows you to place voltage-referenced input signals in an I/O bank with a V_{CCIO} of 2.5 or below. For example, you can place HSTL-15 input pins in an I/O bank with a 2.5-V V_{CCIO}. However, voltage-referenced input with parallel OCT enabled requires the V_{CCIO} of the I/O bank to match the voltage of the input standard.

Voltage-referenced bi-directional and output signals must be the same as the I/O bank's V_{CCIO} voltage. For example, you can only place SSTL-2 output pins in an I/O bank with a 2.5-V V_{CCIO}.

Mixing Voltage-Referenced and Non-Voltage-Referenced Standards

An I/O bank can support both non-voltage-referenced and voltage-referenced pins by applying each of the rule sets individually. For example, an I/O bank can support SSTL-18 inputs and 1.8-V inputs and outputs with a 1.8-V V_{CCIO} and a 0.9-V V_{REF}. Similarly, an I/O bank can support 1.5-V standards, 1.8-V inputs (but not outputs), and HSTL and HSTL-15 I/O standards with a 1.5-V V_{CCIO} and 0.75-V V_{REF}.

For pin connection guidelines, refer to the *Stratix III Device Family Pin Connection Guidelines*.

Table 9–2 lists the LVDS channels (emulated) supported in Stratix III device column I/O banks.

Table 9–2. LVDS Channels (Emulated) Supported in Stratix III Device Column I/O Banks *(Note 1), (2)*

Device	484-Pin FineLine BGA	780-Pin FineLine BGA	1152-Pin FineLine BGA	1517-Pin FineLine BGA	1780-Pin FineLine BGA
EP3SL50	24Rx/eTx + 24eTx	64Rx/eTx + 64eTx	—	—	—
EP3SL70	24Rx/eTx + 24eTx	64Rx/eTx + 64eTx	—	—	—
EP3SL110	—	64Rx/eTx + 64eTx	96Rx/eTx + 96eTx	—	—
EP3SL150	—	64Rx/eTx + 64eTx	96Rx/eTx + 96eTx	—	—
EP3SL200	—	64Rx/eTx + 64eTx *(3)*	96Rx/eTx + 96eTx	128Rx/eTx + 128eTx	—
EP3SL340	—	—	96Rx/eTx + 96eTx *(4)*	128Rx/eTx + 128eTx	144Rx/eTx + 144eTx
EP3SE50	24Rx/eTx + 24eTx	64Rx/eTx + 64eTx	—	—	—
EP3SE80	—	64Rx/eTx + 64eTx	96Rx/eTx + 96eTx	—	—
EP3SE110	—	64Rx/eTx + 64eTx	96Rx/eTx + 96eTx	—	—
EP3SE260	—	64Rx/eTx + 64eTx *(3)*	96Rx/eTx + 96eTx	128Rx/eTx + 128eTx	—

Notes to Table 9–2:

(1) Rx = true LVDS input buffers without on-chip differential input termination.

(2) eTx = emulated LVDS output buffers, either `LVDS_E3R` or `LVDS_E1R`.

(3) The EP3SL200 and EP3SE260 FPGAs are offered in the H780 package, instead of the F780 package.

(4) The EP3SL340 FPGA is offered in the H1152 package, instead of the F1152 package.

Differential Transmitter

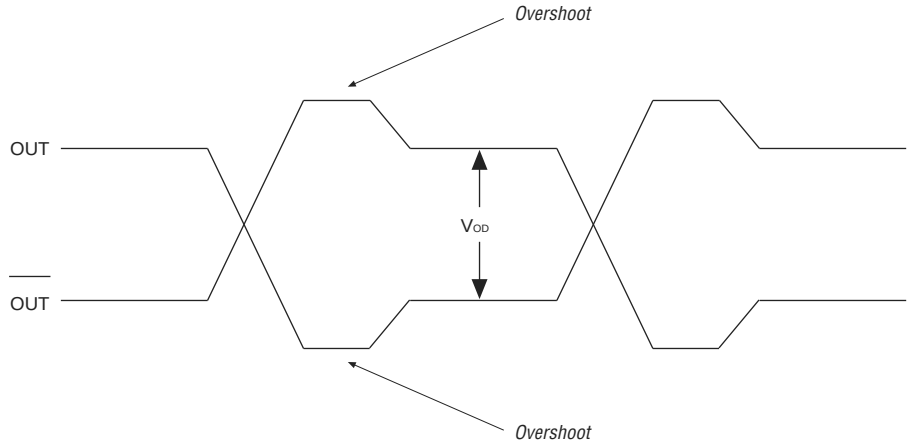
The Stratix III transmitter has dedicated circuitry to provide support for LVDS signaling. The dedicated circuitry consists of a differential buffer, a serializer, and a shared analog PLL (left/right PLL). The differential buffer can drive out LVDS, mini-LVDS, and RSDS signaling levels. The serializer takes up to 10-bits wide parallel data from the FPGA core, clocks it into the load registers, and serializes it using shift registers clocked by the left/right PLL before sending the data to the differential buffer. The most significant bit (MSB) of the parallel data is transmitted first.

The load and shift registers are clocked by the load enable (`load_en`) signal and the `diffioclk` (clock running at serial data rate) signal generated from PLL_Lx (left PLL) or PLL_Rx (right PLL). The serialization factor can be statically set to ×3, ×4, ×5, ×6, ×7, ×8, ×9, or ×10 with the Quartus II software. The load enable signal is derived from the serialization factor setting. Figure 9–2 shows a block diagram of the Stratix III transmitter.

Programmable Pre-Emphasis and Programmable V_{OD}

Stratix III LVDS transmitters support programmable pre-emphasis and programmable voltage output differential (V_{OD}). Pre-emphasis increases the amplitude of the high frequency component of the output signal, and thus helps compensate for the frequency dependent attenuation along the transmission line. Figure 9–10 shows an LVDS output with pre-emphasis. The overshoot is produced by pre-emphasis. This overshoot should not be included in the V_{OD} voltage. The definition of V_{OD} is also shown in Figure 9–10.

Figure 9–10. Programmable V_{OD}



Pre-emphasis is an important feature for high-speed transmission. Without pre-emphasis, the output current is limited by the V_{OD} setting and the output impedance of the driver. At high frequency, the slew rate may not be fast enough to reach the full V_{OD} before the next edge, producing a pattern dependent jitter.

With pre-emphasis, the output current is boosted momentarily during switching to increase the output slew rate. The overshoot introduced by the extra current happens only during switching and does not ring, unlike the overshoot caused by signal reflection. The amount of pre-emphasis required depends on the attenuation of the high-frequency component along the transmission line.

Stratix III pre-emphasis is programmable to create the right amount of overshoot at different transmission conditions. There are four settings for pre-emphasis: zero, low, medium, and high. The default setting is low. In the Quartus II Assignment Editor, pre-emphasis settings are represented in numbers with 0 (zero), 1 (low), 2 (medium) and 3 (high). For a particular design, simulation with an LVDS buffer and transmission line can be used to determine the best pre-emphasis setting.

The V_{OD} is also programmable with four settings: low, medium low, medium high, and high. The default setting is medium low. In the Quartus II Assignment Editor, programmable V_{OD} settings are represented in numbers with 0 (low), 1 (medium low), 2 (medium high) and 3 (high).

Source-Synchronous Timing Budget

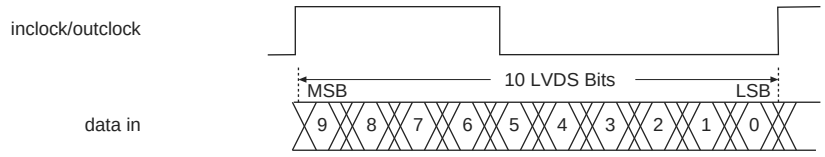
This section discusses the timing budget, waveforms, and specifications for source-synchronous signaling in Stratix III devices. LVDS I/O standards enable high-speed data transmission. This high data transmission rate results in better overall system performance. To take advantage of fast system performance, it is important to understand how to analyze timing for these high-speed signals. Timing analysis for the differential block is different from traditional synchronous timing analysis techniques.

Rather than focusing on clock-to-output and setup times, source synchronous timing analysis is based on the skew between the data and the clock signals. High-speed differential data transmission requires the use of timing parameters provided by IC vendors and is strongly influenced by board skew, cable skew, and clock jitter. This section defines the source-synchronous differential data orientation timing parameters, the timing budget definitions for Stratix III devices, and ways to use these timing parameters to determine the maximum performance of your design.

Differential Data Orientation

There is a set relationship between an external clock and the incoming data. For an operation at 1 Gbps and SERDES factor of 10, the external clock is multiplied by 10, and phase-alignment can be set in the PLL to coincide with the sampling window of each data bit. The data is sampled on the falling edge of the multiplied clock. Figure 9–15 shows the data bit orientation of the ×10 mode.

Figure 9–15. Bit Orientation in Quartus II Software



Differential I/O Bit Position

Data synchronization is necessary for successful data transmission at high frequencies. Figure 9–16 shows the data bit orientation for a channel operation. These figures are based on the following:

- SERDES factor equals clock multiplication factor
- Edge alignment is selected for phase alignment
- Implemented in hard SERDES

For other serialization factors, use the Quartus II software tools and find the bit position within the word and the bit positions after deserialization.

I/O Pins Remain Tri-Stated During Power Up

A device that does not support hot socketing can interrupt system operation or cause contention by driving out before or during power up. In a hot-socketing situation, the Stratix III device's output buffers are turned off during system power up or power down. Also, the Stratix III device does not drive out until the device is configured and working within recommended operating conditions.

Insertion or Removal of a Stratix III Device from a Powered-Up System

Devices that do not support hot socketing can short power supplies when powered up through the device signal pins. This irregular power up can damage both the driving and driven devices and can disrupt card power up.

You can insert a Stratix III device into or remove it from a powered-up system board without damaging the system board or interfering with its operation.

You can power up or power down the core voltage supplies (V_{CC}, V_{CCL}, V_{CCPT}, V_{CCA_PLL}, and V_{CCD_PLL}), V_{CCIO}, V_{CCPMG}, V_{CC_CLKIN}, and V_{CCPD} supplies in any sequence and at any time between them. The individual power supply ramp-up and ramp-down rates can range from 50 µs to 12 ms or 100 ms depending on the PORSEL setting. During hot socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

For more information about the hot socketing specification, refer to the *DC and Switching Characteristics of Stratix III Devices* chapter and the *Hot-Socketing and Power-Sequencing Feature and Testing for Altera Devices White Paper.*

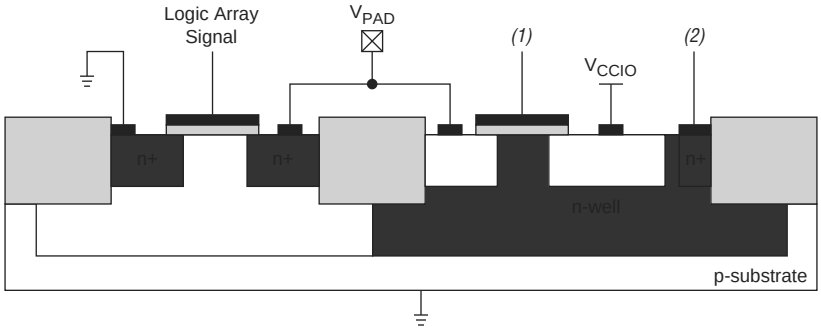
A possible concern regarding hot socketing is the potential for "latch-up". Nevertheless, Stratix III devices are immune to latch-up when hot socketing. Latch-up can occur when electrical subsystems are hot socketed into an active system. During hot socketing, the signal pins can be connected and driven by the active system before the power supply can provide current to the device's power and ground planes. This condition can lead to latch-up and cause a low-impedance path from power to ground within the device. As a result, the device draws a large amount of current, possibly causing electrical damage.

Hot-Socketing Feature Implementation in Stratix III Devices

The hot-socketing feature turns off the output buffer during power up and power down of the V_{CC}, V_{CCIO}, V_{CCPGM}, or V_{CCPD} power supplies. The hot-socketing circuitry generates an internal `HOTSCKT` signal when the V_{CC}, V_{CCIO}, V_{CCPGM}, or V_{CCPD} power supplies are below the threshold voltage. Hot-socketing circuitry is designed to prevent excess I/O leakage during power up. When the voltage ramps up very slowly, it is still relatively low, even after the POR signal is released and the configuration is completed. The `CONF_DONE`, `nCEO`, and `nSTATUS` pins fail to respond, as the output buffer cannot flip from the state set by the hot-socketing circuit at this low voltage. Therefore, the hot-socketing circuit has been removed on these configuration pins to make sure that they are able to operate during configuration. Thus, it is expected behavior for these pins to drive out during power-up and power-down sequences.

Figure 10–2 shows a transistor-level cross section of the Stratix III device I/O buffers. This design prevents leakage current from I/O pins to the V_{CCIO} supply when V_{CCIO} is powered before the other voltage supplies or if the I/O pad voltage is higher than V_{CCIO}. This also applies for sudden voltage spikes during hot insertion. The V_{PAD} leakage current charges the 3.3-V tolerant circuit capacitance.

Figure 10–2. Transistor Level Diagram of a Stratix III Device I/O Buffers



Notes to Figure 10–2:

(1) This is the logic array signal or the larger of either the V_{CCIO} or V_{PAD} signal.
(2) This is the larger of either the V_{CCIO} or V_{PAD} signal.

Power-On Reset Circuitry

When power is applied to a Stratix III device, a POR event occurs when all the power supplies reach the recommended operating range within a certain period of time (specified as a maximum power supply ramp time; t_{RAMP}). Hot socketing feature in Stratix III allows the required power supplies to be powered up in any sequence and at any time between them with each individual power supply must reach the recommended operating range within t_{RAMP}.

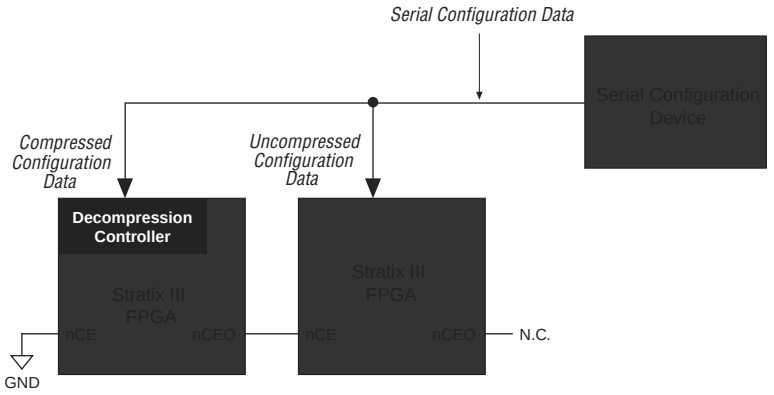
☞ For maximum power supplies ramp-up time for Stratix III Devices, refer Table 10–1.

Stratix III devices provide a dedicated input pin (PORSEL) to select a POR delay time during power up. When the PORSEL pin is connected to ground, the POR delay time is 100 ms. When the PORSEL pin is set to high, the POR delay time is 12 ms.

The POR block consists of a regulator POR, satellite POR, and main POR to check the power supply levels for proper device configuration. The satellite POR monitors V_{CCPD} and V_{CCPGM} power supplies that are used in the configuration buffers for device programming. The POR block also checks for functionality of I/O level shifters powered by V_{CCPD} and V_{CCPGM} during power-up mode. The main POR checks the V_{CC} and V_{CCL} supplies used in core. The internal configuration memory supply, which is used during device configuration, is checked by the regulator POR block and is gated in the main POR block for the final POR trip. A simplified block diagram of the POR block is shown in Figure 10–3.

☞ All configuration-related dedicated and dual function I/O pins must be powered by V_{CCPGM}.

Figure 11–2. Compressed and Uncompressed Configuration Data in the Same Configuration File



To generate programming files for this setup in the Quartus II software, on the File menu, click **Convert Programming Files**.

Design Security Using Configuration Bitstream Encryption

Stratix III devices support decryption of configuration bitstreams using the advanced encryption standard (AES) algorithm—the most advanced encryption algorithm available today. Both non-volatile and volatile key programming are supported using Stratix III devices. When using the design security feature, a 256-bit security key is stored in the Stratix III device. To successfully configure a Stratix III device that has the design security feature enabled, the device must be configured with a configuration file that was encrypted using the same 256-bit security key. Non-volatile key programming does not require any external devices, such as a battery backup, for storage. However, for certain applications, you can store the security keys in volatile memory in the Stratix III device. An external battery is needed for this volatile key storage.

When using a serial configuration scheme such as PS or fast AS, configuration time is the same whether or not the design security feature is enabled. If the FPP scheme is used with the design security or decompression feature, a ×4 DCLK is required. This results in a slower configuration time when compared to the configuration time of a Stratix III device that has neither the design security nor the decompression feature enabled.

For more information about this feature, refer to the *Design Security in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Table 12–3. Remote System Upgrade Control Register Contents (Part 2 of 2)

Control Register Bit	Remote System Upgrade Mode	Value *(2)*	Definition
wd_en	Remote update	1'b0	User watchdog timer enable bit
wd_timer[11..0]	Remote update	12'b000000000000	User watchdog time-out value (most significant 12 bits of 29-bit count value: {wd_timer[11..0], 17'b0})

Notes to Table 12–3:

(1) In remote update mode, the remote configuration block does not update the AnF bit automatically (you can update it manually).

(2) This is the default value of the control register bit.

Remote System Upgrade Status Register

The remote system upgrade status register specifies the reconfiguration trigger condition. The various trigger and error conditions include in the following:

- Cyclic redundancy check (CRC) error during application configuration
- nSTATUS assertion by an external device due to an error
- Stratix III device logic array triggers a reconfiguration cycle, possibly after downloading a new application configuration image
- External configuration reset (nCONFIG) assertion
- User watchdog timer time out

Figure 12–7 and Table 12–4 specify the contents of the status register. The numbers in the figure show the bit positions within a 5-bit register.

Figure 12–7. Remote System Upgrade Status Register

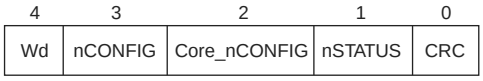


Table 12–4. Remote System Upgrade Status Register Contents

Status Register Bit	Definition	POR Reset Value
CRC (from configuration)	CRC error caused reconfiguration	1 bit '0'
nSTATUS	nSTATUS caused reconfiguration	1 bit '0'
CORE_nCONFIG *(1)*	Device logic array caused reconfiguration	1 bit '0'
nCONFIG	nCONFIG caused reconfiguration	1 bit '0'
wd	Watchdog timer caused reconfiguration	1 bit '0'

Note to Table 12–4:

(1) Logic array reconfiguration forces the system to load the application configuration data into the Stratix III device. This occurs after the factory configuration specifies the appropriate application configuration page address by updating the update register.

Conclusion

The need for design security is increasing as devices move from glue logic to implementing critical system functions. Stratix III devices address this concern by providing built-in design security. These devices not only offer high density, fast performance, and cutting-edge features to meet your design needs, but also protect your designs against IP theft and tampering of your configuration files.

Chapter Revision History

Table 14–6 shows the revision history for this document.

Table 14–6. Chapter Revision History

Date and Revision	Changes Made	Summary of Changes
May 2009, version 1.5	Updated "Flexible Security Key Storage" and "Non-Volatile Key with Tamper Protection Bit Set" sections.	—
February 2009, version 1.4	■ Updated "Flexible Security Key Storage" section. ■ Removed "Referenced Documents" section.	—
October 2008, version 1.3	■ Updated "Non-Volatile Key with Tamper Protection Bit Set" section. ■ Added Table 14–2. ■ Updated New Document Format.	—
May 2008, version 1.2	■ Updated "Introduction" section. ■ Updated "Flexible Security Key Storage" section. ■ Updated Table 14–1 and Table 14–4. ■ Updated "Security Modes Available" section.	—
October 2007, version 1.1	■ Added new section "Referenced Documents". ■ Added live links for references.	Minor update
November 2006, version 1.0	Initial Release.	—