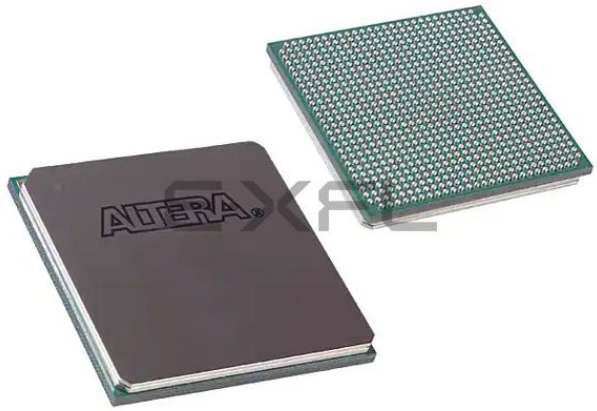

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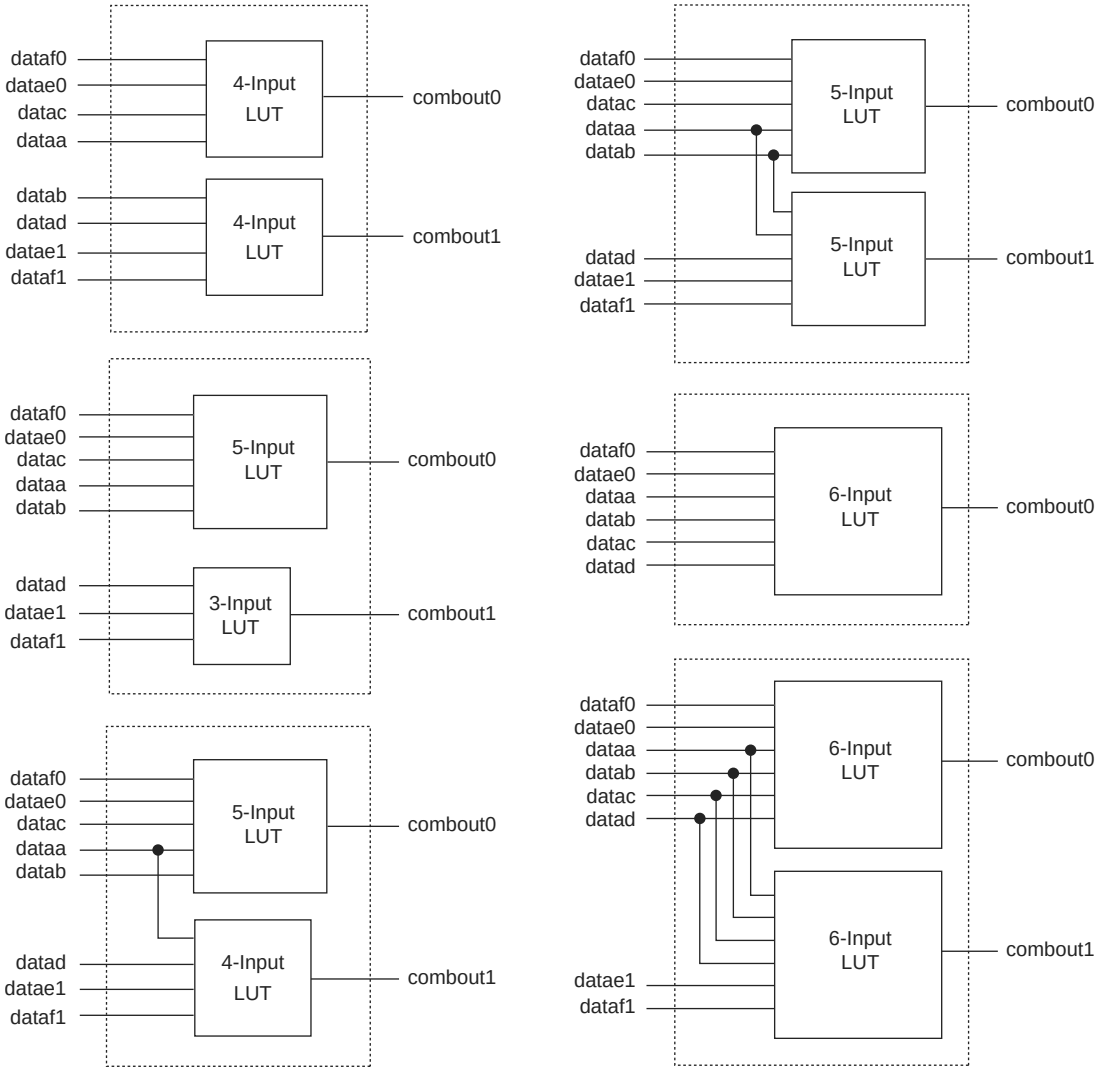
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	5700
Number of Logic Elements/Cells	142500
Total RAM Bits	6543360
Number of I/O	488
Number of Gates	-
Voltage - Supply	0.86V ~ 1.15V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep3sl150f780c4ln

Figure 2–7. ALM in Normal Mode *(Note 1)*



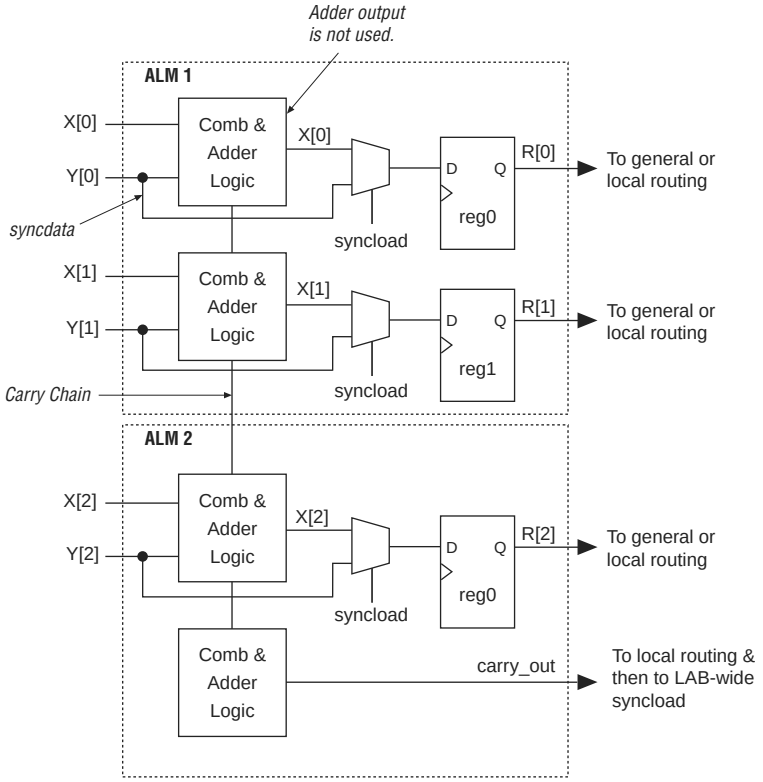
Note to Figure 2–7:

(1) Combinations of functions with fewer inputs than those shown are also supported. For example, combinations of functions with the following number of inputs are supported: 4 and 3, 3 and 3, 3 and 2, 5 and 2.

The normal mode provides complete backward compatibility with four-input LUT architectures.

For the packing of 2 five-input functions into one ALM, the functions must have at least two common inputs. The common inputs are `dataa` and `datab`. The combination of a four-input function with a five-input function requires one common input (either `dataa` or `datab`).

Figure 2–12. Conditional Operation Example



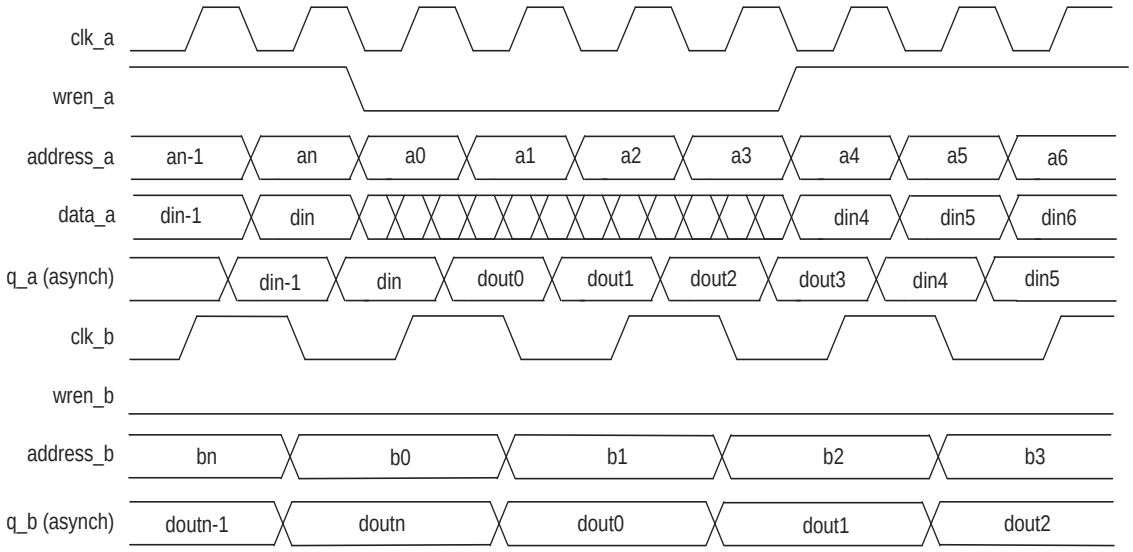
The equation for this example is:

$R = (X < Y) \ ? \ Y : X$

To implement this function, the adder is used to subtract *Y* from *X*. If *X* is less than *Y*, the `carry_out` signal is 1. The `carry_out` signal is fed to an adder where it drives out to the LAB local interconnect. It then feeds to the LAB-wide `syncload` signal. When asserted, `syncload` selects the `syncdata` input. In this case, the data *Y* drives the syncdata inputs to the registers. If *X* is greater than or equal to *Y*, the `syncload` signal is de-asserted and *X* drives the data port of the registers.

The arithmetic mode also offers clock enable, counter enable, synchronous up/down control, add/subtract control, synchronous clear, and synchronous load. The LAB local interconnect data inputs generate the clock enable, counter enable, synchronous up/down, and add/subtract control signals. These control signals are good candidates for the inputs that are shared between the four LUTs in the ALM. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. These signals can also be individually disabled or enabled per register. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Figure 4–16. Stratix III True Dual-Port Timing Waveform

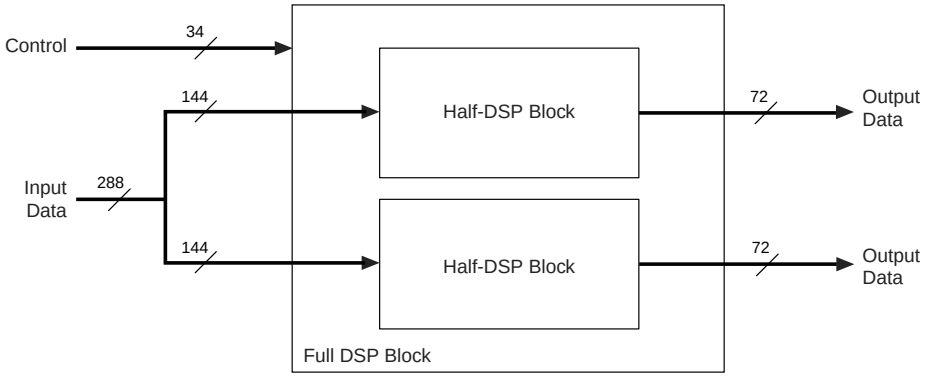


Shift-Register Mode

All Stratix III memory blocks support shift register mode. Embedded memory block configurations can implement shift registers for digital signal processing (DSP) applications, such as finite impulse response (FIR) filters, pseudo-random number generators, multi-channel filtering, and auto- and cross-correlation functions. These and other DSP applications require local data storage, traditionally implemented with standard flipflops that quickly exhaust many logic cells for large shift registers. A more efficient alternative is to use embedded memory as a shift-register block, which saves logic cell and routing resources.

The size of a shift register ($w \times m \times n$) is determined by the input data width (w), the length of the taps (m), and the number of taps (n). You can cascade memory blocks to implement larger shift registers.

Figure 5–1. Overview of DSP Block Signals



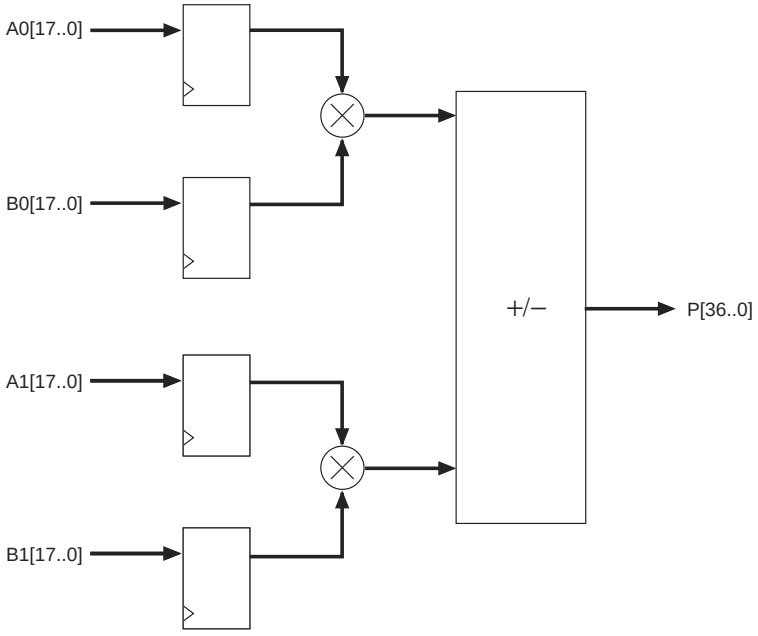
Simplified DSP Operation

In Stratix and Stratix II devices, the fundamental building block consists of an 18-bit × 18-bit multiplier that can also function as two 9-bit × 9-bit multipliers. For Stratix III, the fundamental building block is a pair of 18-bit × 18-bit multipliers followed by a first-stage 37-bit addition/subtraction unit, as shown in Equation 5–1 and Figure 5–2. Note that for all signed numbers, input and output data is represented in 2's complement format only.

Equation 5–1. Multiplier Equation

$$P[36..0] = A_0[17..0] \times B_0[17..0] \pm A_1[17..0] \times B_1[17..0]$$

Figure 5–2. Basic Two-Multiplier Adder Building Block



18 × 18 Complex Multiply

You can configure the DSP block when used in Two-Multiplier Adder mode to implement complex multipliers using the two-multiplier adder mode. A single half DSP block can implement one 18-bit complex multiplier.

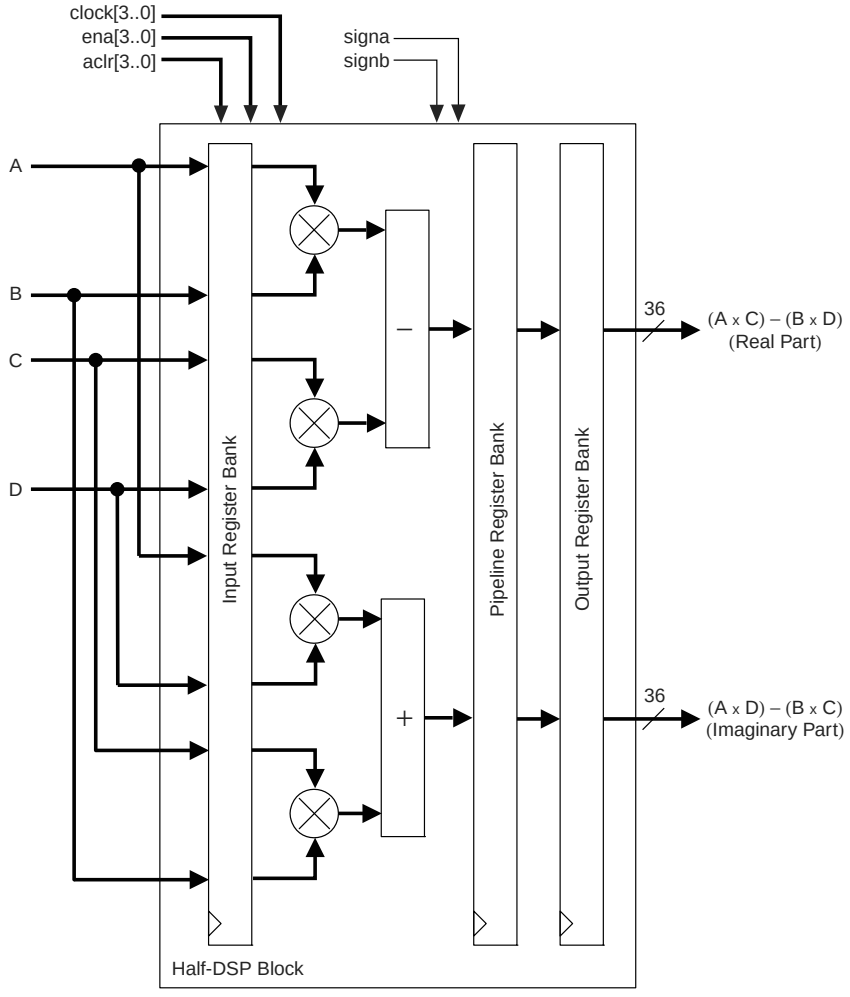
A complex multiplication can be written as shown in Equation 5–4.

Equation 5–4. Complex Multiplication Equation

$$(a + jb) \times (c + jd) = ((a \times c) - (b \times d)) + j((a \times d) + (b \times c))$$

To implement this complex multiplication within the DSP block, the real part ((a × c) – (b × d)) is implemented using two multipliers feeding one subtractor block while the imaginary part ((a × d) + (b × c)) is implemented using another two multipliers feeding an adder block. Figure 5–16 shows an 18-bit complex multiplication. This mode automatically assumes all inputs are using signed numbers.

Figure 5–16. Complex Multiplier Using Two-Multiplier Adder Mode

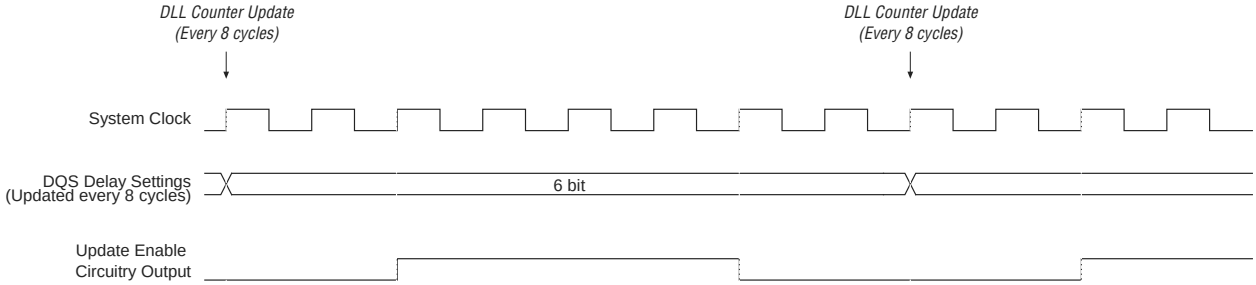


You can also bypass the DQS delay chain to achieve 0° phase shift.

Update Enable Circuitry

Both the DQS delay settings and phase-offset settings pass through a register before going into the DQS delay chains. The registers are controlled by the update enable circuitry to allow enough time for any changes in the DQS delay setting bits to arrive at all the delay elements. This allows them to be adjusted at the same time. The update enable circuitry enables the registers to allow enough time for the DQS delay settings to travel from the DQS phase-shift circuitry or core logic to all the DQS logic blocks before the next change. It uses the input reference clock or a user clock from the core to generate the update enable output. The ALTMEMPHY megafunction uses this circuit by default. See Figure 8–14 for an example waveform of the update enable circuitry output.

Figure 8–14. Example of a DQS Update Enable Waveform



DQS Postamble Circuitry

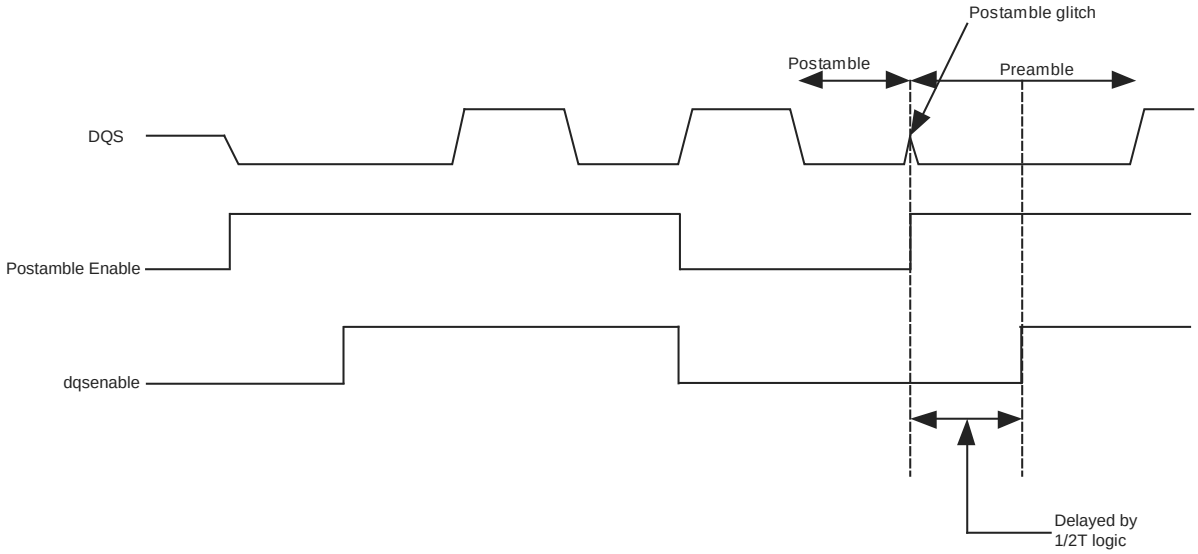
For external memory interfaces that use a bi-directional read strobe like DDR3, DDR2, and DDR SDRAM, the DQS signal is low before going to or coming from a high-impedance state. The state where DQS is low, just after a high-impedance state, is called the preamble. The state where DQS is low, just before it returns to a high-impedance state, is called the postamble. There are preamble and postamble specifications for both read and write operations in DDR3, DDR2, and DDR SDRAM. The DQS postamble circuitry ensures that the data is not lost if there is noise on the DQS line during the end of a read operation that occurs while the DQS is in a postamble state.

Stratix III devices have a dedicated postamble register that you can control to ground the shifted DQS signal used to clock the DQ input registers at the end of a read operation. This ensures that any glitches on the DQS input signals at the end of the read postamble time do not affect the DQ IOE registers.

In addition to the dedicated postamble register, Stratix III devices also have an HDR block inside the postamble enable circuitry. These registers are used if the controller is running at half the frequency of the I/Os.

Using the HDR block as the first stage capture register in the postamble enable circuitry block is optional. The HDR block is clocked by the half-rate resynchronization clock, which is the output of the I/O clock divider circuit (shown in Figure 8–20 on page 8–35). There is an AND gate after the postamble register outputs that is used to avoid postamble glitches from a previous read burst on a non-consecutive read burst. This scheme allows a half-a-clock cycle latency for `dqsenable` assertion and zero latency for `dqsenable` deassertion, as shown in Figure 8–15.

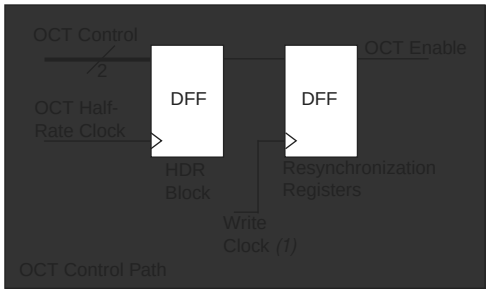
Figure 8–15. Avoiding a Glitch on a Non-Consecutive Read Burst Waveform



Leveling Circuitry

DDR3 SDRAM unbuffered modules use a fly-by clock distribution topology for better signal integrity. This means that the CK/CK# signals arrive at each DDR3 SDRAM device in the module at different times. The difference in arrival time between the first DDR3 SDRAM device and the last device on the module can be as long as 1.6 ns. Figure 8–16 shows the clock topology in DDR3 SDRAM unbuffered modules.

Figure 8–19. Stratix III Dynamic OCT Control Block



Note to Figure 8–19:

(1) The write clock comes from either the PLL or the write leveling delay chain.

IOE Registers

The IOE registers have been expanded to allow source-synchronous systems to have faster register-to-register transfers and resynchronization. Both top/bottom and left/right IOEs have the same capability with left/right IOEs having extra features to support LVDS data transfer.

Figure 8–20 shows the registers available in the Stratix III input path. The input path consists of the DDR input registers, resynchronization registers, and HDR block. You can bypass each block of the input path.

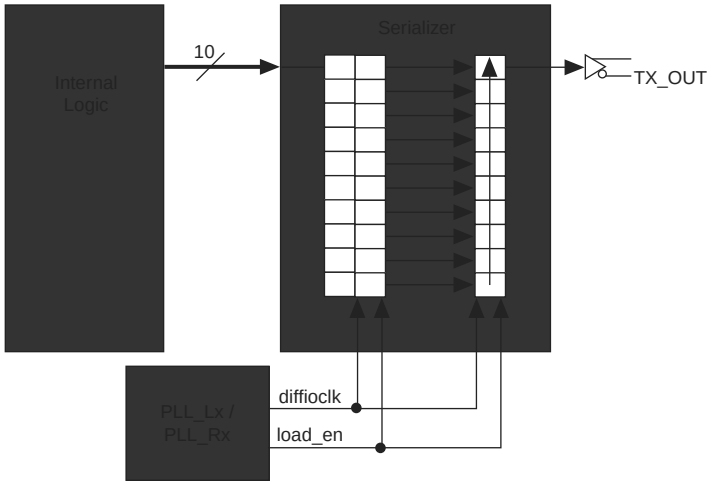
Chapter Revision History

Table 8–13 lists the revision history for this chapter.

Table 8–13. Chapter Revision History (Part 1 of 2)

Date and Revision	Changes Made	Summary of Changes
March 2010, version 1.9	■ Added "Delay Chain" section. ■ Updated "DLL", "DQS Logic Block", and "Dynamic OCT Control" sections. ■ Added Figure 8–22, Figure 8–23, Figure 8–24, and Figure 8–25. ■ Updated Figure 8–12, Figure 8–13,and Figure 8–20. ■ Added Table 8–11 and Table 8–12. ■ Updated Table 8–7. ■ Minor text edits.	Updated for the Quartus II software version 9.1 SP2 release.
May 2009, version 1.8	■ Updated Table 8–1, Table 8–2, Table 8–3, Table 8–2, Table 8–4, and Table 8–10. ■ Updated Figure 8–3, Figure 8–4, Figure 8–5, Figure 8–6, and Figure 8–7. ■ Updated "DLL", "Memory Interfaces Pin Support", and "Rules to Combine Groups"sections.	—
February 2009, version 1.7	■ Updated Table 8–1,Table 8–2, and Table 8–6. ■ Updated "Data and Data-Strobe/Clock Pins" section. ■ Removed "Referenced Document" section.	—
October 2008, version 1.6	■ Updated Table 8–1, Table 8–2, Table 8–3, Table 8–4, Table 8–5, Table 8–7, and Table 8–8. ■ Updated the "Rules to Combine Groups", "Phase Offset Control", "OCT", "Introduction", "Memory Interfaces Pin Support", "Combining ×16/×18 DQS/DQ groups for ×36 QDR II+/QDR II SRAM Interface", "Rules to Combine Groups", "DQS Phase-Shift Circuitry", "DLL", and "DQS Delay Chain" sections. ■ Updated Figure 8–2, Figure 8–4, Figure 8–10, Figure 8–21, and Figure 8–22. ■ Updated New Document Format. ■ Added (Note 3) to Table 8–5.	—
July 2008, version 1.5	Updated Table 8–1 and Table 8–2.	—
May 2008, version 1.4	■ Updated Figure 8–2, Figure 8–9, Figure 8–18, Figure 8–21, and Figure 8–22. ■ Updated Table 8–1, Table 8–2, Table 8–3, Table 8–4, Table 8–7, and Table 8–10. ■ Added Table 8–7 and Table 8–8. ■ Added Figure 8–19. ■ Added new "Supporting ×36 QDR II+/QDR II SRAM Interfaces in the F780 and F1152-Pin Packages" section. ■ Updated "Data and Data Clock/Strobe Pins". ■ Updated "Referenced Documents".	Text, Table, and Figure updates.

Figure 9–2. Transmitter Block Diagram for Stratix III Devices



You can configure any Stratix III transmitter data channel to generate a source-synchronous transmitter clock output. This flexibility allows placing the output clock near the data outputs to simplify board layout and reduce clock-to-data skew. Different applications often require specific clock-to-data alignments or specific data rate-to-clock rate factors. The transmitter can output a clock signal at the same rate as the data with a maximum frequency of 800 MHz. You can also divide the output clock by a factor of 2, 4, 8, or 10, depending on the serialization factor. The phase of the clock in relation to the data can be set at 0° or 180° (edge or center aligned). The left and right PLLs (PLL_Lx/PLL_Rx) provide additional support for other phase shifts in 45° increments. These settings are statically made in the MegaWizard® Plug-In Manager in the Quartus II software.

Figure 9–3 shows the Stratix III transmitter in clock output mode.

Figure 9–3. Transmitter in Clock Output Mode for Stratix III Devices

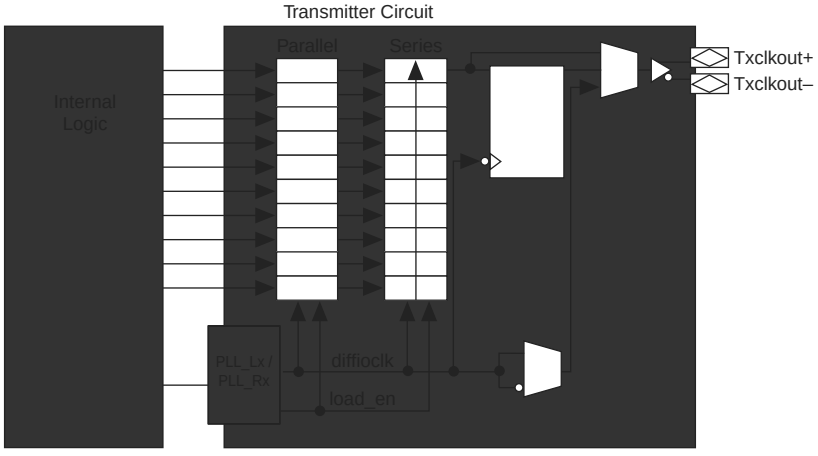


Figure 9–20. Invalid Placement of DPA-Enabled Differential I/Os Driven by Both Center Left/Right PLLs

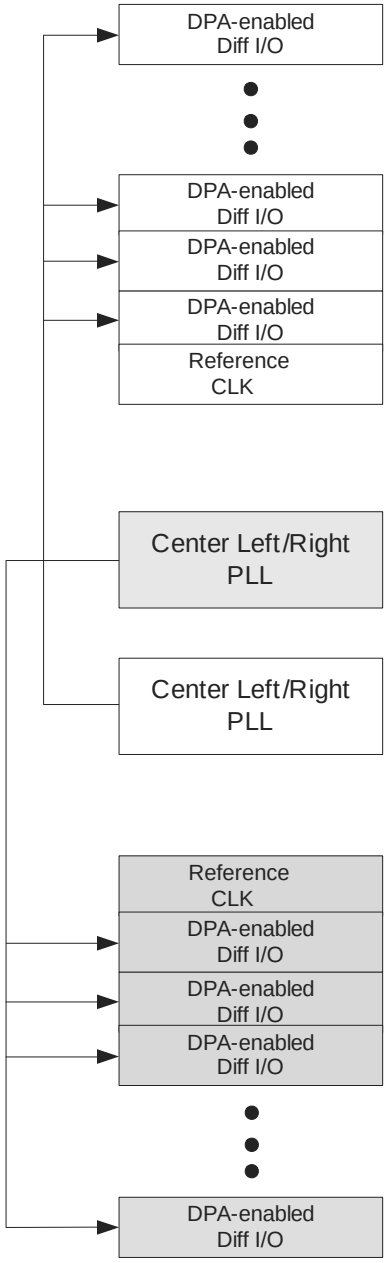
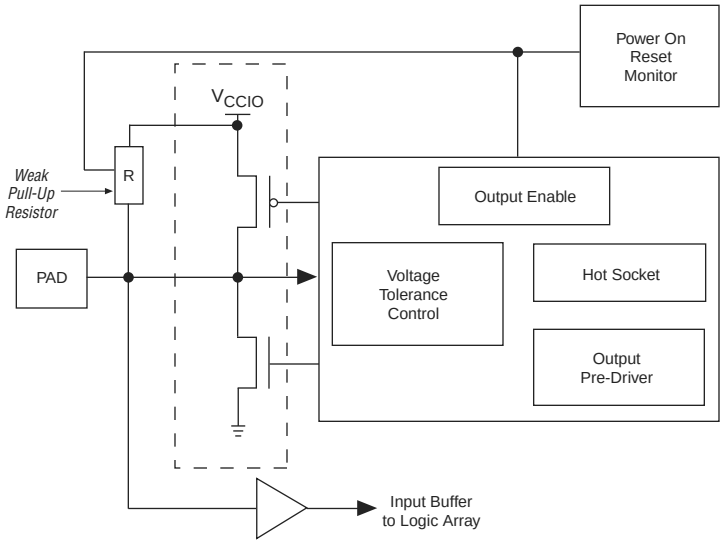


Figure 10–1 shows the Stratix III device's I/O pin circuitry.

Figure 10–1. Hot-Socketing Circuitry for Stratix III Devices

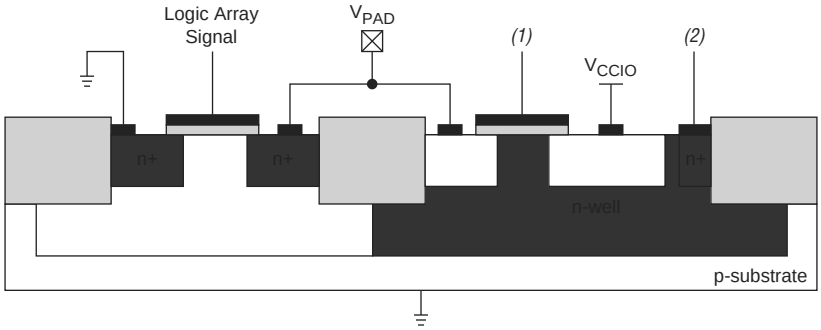


The POR circuit monitors the voltage level of power supplies (V_{CC}, V_{CCL}, V_{CCPD}, V_{CCPGM} and V_{CCPT}) and keeps the I/O pins tri-stated until the device is in user mode. The weak pull-up resistor (R) in the Stratix III input/output element (IOE) keeps the I/O pins from floating. The 3.3-V tolerance control circuit permits the I/O pins to be driven by 3.3 V before V_{CCIO}, V_{CC}, V_{CCPD}, and/or V_{CCPGM} supplies are powered, and it prevents the I/O pins from driving out when the device is not in user mode.

Altera uses GND as reference for hot-socketing operation and I/O buffer designs. To ensure proper operation, you must connect the GND between boards before connecting the power supplies. This will prevent the GND on your board from being pulled up inadvertently by a path to power through other components on your board. A pulled up GND could otherwise cause an out-of-specification I/O voltage or current condition with the Altera device.

Figure 10–2 shows a transistor-level cross section of the Stratix III device I/O buffers. This design prevents leakage current from I/O pins to the V_{CCIO} supply when V_{CCIO} is powered before the other voltage supplies or if the I/O pad voltage is higher than V_{CCIO}. This also applies for sudden voltage spikes during hot insertion. The V_{PAD} leakage current charges the 3.3-V tolerant circuit capacitance.

Figure 10–2. Transistor Level Diagram of a Stratix III Device I/O Buffers



Notes to Figure 10–2:

(1) This is the logic array signal or the larger of either the V_{CCIO} or V_{PAD} signal.
(2) This is the larger of either the V_{CCIO} or V_{PAD} signal.

Power-On Reset Circuitry

When power is applied to a Stratix III device, a POR event occurs when all the power supplies reach the recommended operating range within a certain period of time (specified as a maximum power supply ramp time; t_{RAMP}). Hot socketing feature in Stratix III allows the required power supplies to be powered up in any sequence and at any time between them with each individual power supply must reach the recommended operating range within t_{RAMP}.

☞ For maximum power supplies ramp-up time for Stratix III Devices, refer Table 10–1.

Stratix III devices provide a dedicated input pin (PORSEL) to select a POR delay time during power up. When the PORSEL pin is connected to ground, the POR delay time is 100 ms. When the PORSEL pin is set to high, the POR delay time is 12 ms.

The POR block consists of a regulator POR, satellite POR, and main POR to check the power supply levels for proper device configuration. The satellite POR monitors V_{CCPD} and V_{CCPGM} power supplies that are used in the configuration buffers for device programming. The POR block also checks for functionality of I/O level shifters powered by V_{CCPD} and V_{CCPGM} during power-up mode. The main POR checks the V_{CC} and V_{CCL} supplies used in core. The internal configuration memory supply, which is used during device configuration, is checked by the regulator POR block and is gated in the main POR block for the final POR trip. A simplified block diagram of the POR block is shown in Figure 10–3.

☞ All configuration-related dedicated and dual function I/O pins must be powered by V_{CCPGM}.

Fast Passive Parallel Configuration

Fast passive parallel (FPP) configuration in Stratix III devices is designed to meet the continuously increasing demand for faster configuration times. Stratix III devices are designed with the capability of receiving byte-wide configuration data per clock cycle. Table 11–4 lists the MSEL pin settings when using the FPP configuration scheme.

Table 11–4. Stratix III MSEL Pin Settings for FPP Configuration Schemes

Configuration Scheme	MSEL2	MSEL1	MSEL0
Fast Passive Parallel (FPP)	0	0	0
FPP with the design security feature, decompression feature, or both enabled *(1)*	0	0	1

Note to Table 11–4:

(1) These modes are only supported when using a MAX II device or a microprocessor with flash memory for configuration. In these modes, the host system must output a DCLK that is ×4 the data rate.

You can perform FPP configuration of Stratix III devices using an intelligent host, such as a MAX II device, or a microprocessor.

FPP Configuration Using a MAX II Device as an External Host

FPP configuration using compression and an external host provides the fastest method to configure Stratix III devices. In this configuration scheme, you can use a MAX II device as an intelligent host that controls the transfer of configuration data from a storage device, such as flash memory, to the target Stratix III device. You can store configuration data in **.rbf**, **.hex**, or **.ttf** format. When using the MAX II device as an intelligent host, a design that controls the configuration process, such as fetching the data from flash memory and sending it to the device, must be stored in the MAX II device.

If you are using the Stratix III decompression feature, design security feature or both, the external host must be able to send a DCLK frequency that is four times the data rate.

The ×4 DCLK signal does not require an additional pin and is sent on the DCLK pin. The maximum DCLK frequency is 100 MHz, which results in a maximum data rate of 200 Mbps. If you are not using the Stratix III decompression or design security features, the data rate is the same as the DCLK frequency.

Table 11–15 describes the optional configuration pins. If these optional configuration pins are not enabled in the Quartus II software, they are available as general-purpose user I/O pins. Therefore, during configuration, these pins function as user I/O pins and are tri-stated with weak pull-up resistors.

Table 11–15. Optional Configuration Pins

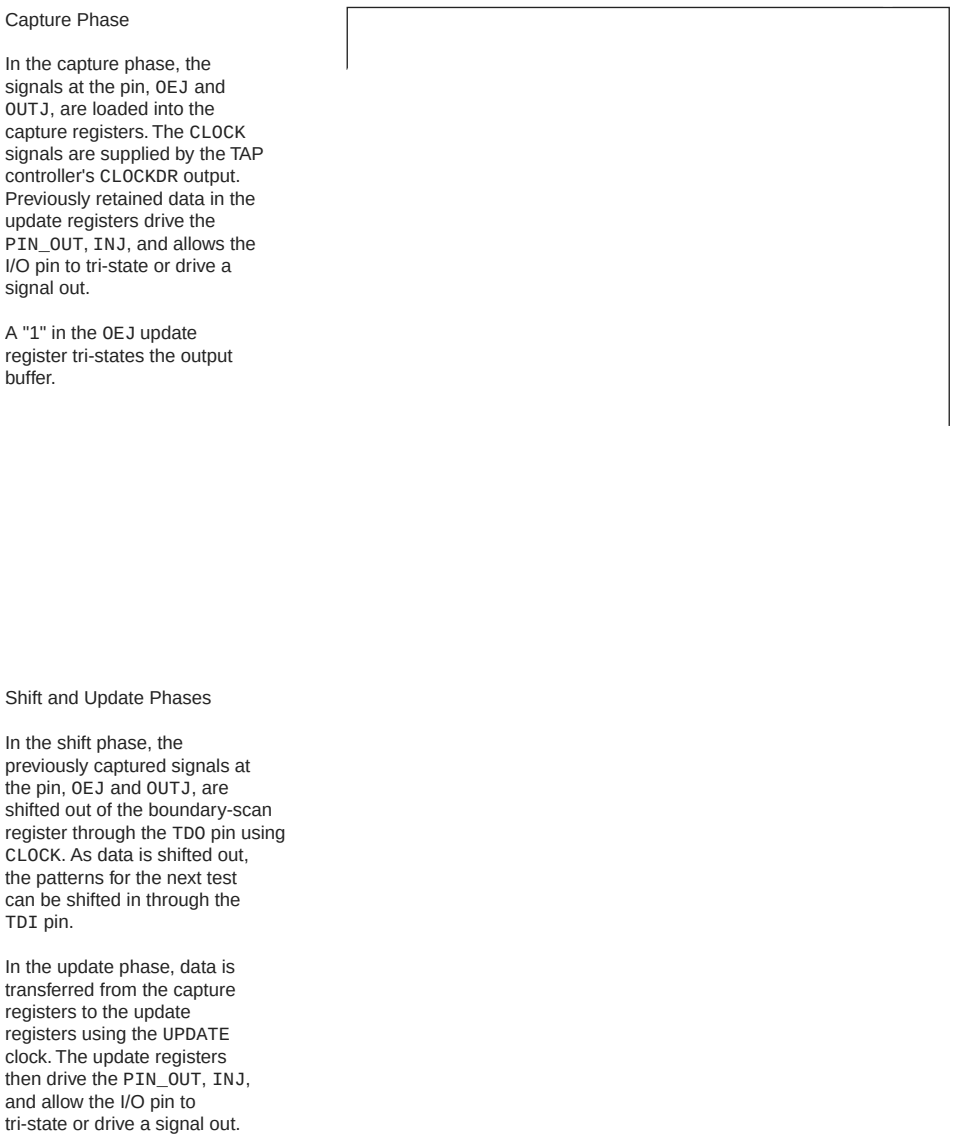
Pin Name	User Mode	Pin Type	Description
CLKUSR	N/A if option is on. I/O if option is off.	Input	Optional user-supplied clock input synchronizes the initialization of one or more devices. Enable this pin by turning on the **Enable user-supplied start-up clock** (**CLKUSR**) option in the Quartus II software.
INIT_DONE	N/A if option is on. I/O if option is off.	Output open-drain	Use the Status pin to indicate when the device has initialized and is in user mode. When nCONFIG is low and during the beginning of configuration, the INIT_DONE pin is tri-stated and pulled high due to an external 10-kΩ pull-up resistor. After the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin will go low. When initialization is complete, the INIT_DONE pin is released and pulled high and the device enters user mode. Thus, the monitoring circuitry must be able to detect a low-to-high transition. This pin is enabled by turning on the **Enable INIT_DONE output** option in the Quartus II software.
DEV_OE	N/A if option is on. I/O if option is off.	Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated, when this pin is driven high, all I/O pins behave as programmed. Enable this pin by turning on the **Enable device-wide output enable** (**DEV_OE**) option in the Quartus II software.
DEV_CLRn	N/A if option is on. I/O if option is off.	Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared. When this pin is driven high, all registers behave as programmed. This pin is enabled by turning on the **Enable device-wide reset** (**DEV_CLRn**) option in the Quartus II software.

EXTEST Instruction Mode

Use the EXTEST instruction mode primarily to check external pin connections between devices. Unlike the SAMPLE/PRELOAD mode, EXTEST allows test data to be forced onto the pin signals. By forcing known logic high and low levels on output pins, you can detect opens and shorts at pins of any device in the scan chain.

Figure 13–10 shows the capture, shift, and update phases of the EXTEST mode.

Figure 13–10. IEEE Std. 1149.1 BST EXTEST Mode



For possible values of each power supply, refer to the *DC and Switching Characteristics of Stratix III Devices* chapter in volume 2 of the *Stratix III Device Handbook*.

For detailed guidelines about how to connect and isolate VCCL and VCC power supply pins, refer to the *Stratix III Device Family Pin Connections Guidelines*.

Table 16–2. Stratix III Power Supply Requirements

Power Supply Pin	Recommended Board Connection	Description
VCCL	VCCL	Selectable core voltage power supply
VCC	VCC	I/O registers power supply
VCCD_PLL	VCCD_PLL	PLL digital power supply
VCCA_PLL	VCCA_PLL *(1)*	PLL analog power supply
VCCPT		Power supply for programmable power technology
VCCPGM	VCCPGM	Configuration pins power supply
VCCPD	VCCPD *(2)*	I/O pre-driver power supply
VCCIO	VCCIO *(3)*	I/O power supply
VCC_CLKIN		Differential clock input pins power supply (top and bottom I/O banks only)
VCCBAT	VCCBAT	Battery back-up power supply for design security volatile key register
VREF	VREF *(4)*	Power supply for voltage-referenced I/O standards
GND	GND	Ground

Notes to Table 16–2:

(1) You can minimize the number of external power sources by driving the left column and supplies with the same voltage regulator. Note that separate power planes, decoupling capacitors, and ferrite beads are required for VCCA_PLL and VCCPT when implementing this scheme.

(2) V_{CCPD} can be either 2.5 V, 3.0 V, or 3.3 V. For a 3.3-V standard, V_{CCPD} = 3.3 V. For a 3.0-V I/O standard, V_{CCPD} = 3.0 V. For 2.5 V and below I/O standards, V_{CCPD} = 2.5 V.

(3) This scheme is for VCCIO = 2.5 V.

(4) There is one VREF pin per I/O bank. Use an external power supply or a resistor divider network to supply this voltage.

Thermal Resistance

For Stratix III devices thermal resistance specifications, refer to the *Stratix Series Device Thermal Resistance Data Sheet*.

Package Outlines

You can download Stratix III device package outlines from the *Device Packaging Specifications* web page.

Chapter Revision History

Table 17–2 lists the revision history for this chapter.

Table 17–2. Chapter Revision History

Date	Version	Changes Made
March 2010	1.7	Updated for the Quartus II software version 9.1 SP2 release: ■ Updated Table 17–1. ■ Minor text edits.
February 2009	1.6	Removed "Referenced Documents" section.
October 2008	1.5	Updated New Document Format.
May 2008	1.4	Updated "Package Outlines" section hyperlink.
November 2007	1.3	Updated Table 17–1.
October 2007	1.2	■ Added new section "Referenced Documents". ■ Added live links for references.
May 2007	1.1	Removed thermal resistance and package outline information and replaced with links referencing this information.
November 2006	1.0	Initial Release.