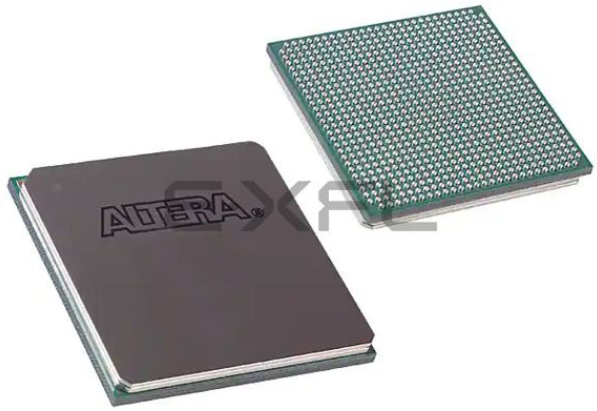

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	5700
Number of Logic Elements/Cells	142500
Total RAM Bits	6543360
Number of I/O	488
Number of Gates	-
Voltage - Supply	0.86V ~ 1.15V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep3sl150f780c4n

MultiTrack Interconnect

In the Stratix III architecture, connections between ALMs, TriMatrix memory, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive technology. The MultiTrack interconnect consists of continuous, performance-optimized row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities. The MultiTrack interconnect provides 1-hop connection to 34 adjacent LABs, 2-hop connections to 96 adjacent LABs and 3-hop connections to 160 adjacent LABs.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement in the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the reoptimization cycles that typically follow design changes and additions. The Quartus II Compiler also automatically places critical design paths on faster interconnects to improve design performance.

f For more information, refer to the MultiTrack Interconnect in Stratix III Devices chapter.

TriMatrix Embedded Memory Blocks

TriMatrix embedded memory blocks provide three different sizes of embedded SRAM to efficiently address the needs of Stratix III FPGA designs. TriMatrix memory includes the following blocks:

- 320-bit MLAB blocks optimized to implement filter delay lines, small FIFO buffers, and shift registers
- 9-Kbit M9K blocks that can be used for general purpose memory applications
- 144-Kbit M144K blocks that are ideal for processor code storage, packet and video frame buffering

Each embedded memory block can be independently configured to be a single- or dual-port RAM, ROM, or shift register via the Quartus II MegaWizard ™ Plug-In Manager. Multiple blocks of the same type can also be stitched together to produce larger memories with minimal timing penalty. TriMatrix memory provides up to 16,272 Kbits of embedded SRAM at up to 600 MHz operation.

f For more information about TriMatrix memory blocks, modes, features, and design considerations, refer to the TriMatrix Embedded Memory Blocks in Stratix III Devices chapter.

DSP Blocks

Stratix III devices have dedicated high-performance digital signal processing (DSP) blocks optimized for DSP applications requiring high data throughput. Stratix III devices provide you with the ability to implement various high-performance DSP functions easily. Complex systems such as WiMAX, 3GPP WCDMA, CDMA2000, voice over Internet Protocol (VoIP), H.264 video compression, and high-definition television (HDTV) require high-performance DSP blocks to process data. These system designs typically use DSP blocks to implement finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, and discrete cosine transform (DCT) functions.

Stratix III devices include an enhanced interconnect structure in LABs for routing-shared arithmetic chains and carry chains for efficient arithmetic functions. The register chain connection allows the register output of one ALM to connect directly to the register input of the next ALM in the LAB for fast shift registers. These ALM-to-ALM connections bypass the local interconnect. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 3–2 shows the shared arithmetic chain, carry chain, and register chain interconnects.

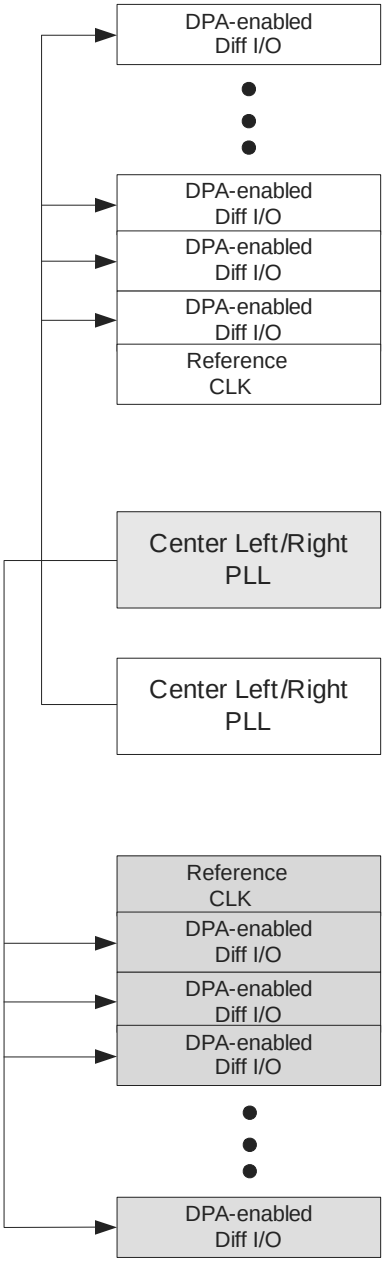
7. Stratix III Device I/O Features

SIII51007-1.9

Stratix® III I/Os are specifically designed for ease of use and rapid system integration while simultaneously providing the high bandwidth required to maximize internal logic capabilities and produce system-level performance. Independent modular I/O banks with a common bank structure for vertical migration lend efficiency and flexibility to the high speed I/O. Package and die enhancements with dynamic termination and output control provide best-in-class signal integrity. Numerous I/O features assist in high-speed data transfer into and out of the device, including:

- Single-ended, non-voltage-referenced, and voltage-referenced I/O standards
- Low-voltage differential signaling (LVDS), reduced swing differential signal (RSDS), mini-LVDS, high-speed transceiver logic (HSTL), and stub series terminated logic (SSTL)
- Single data rate (SDR) and half data rate (HDR—half frequency and twice data width of SDR) input and output options
- Up to 132-full duplex 1.6-Gbps true LVDS channels (132 Tx + 132 Rx) on the row I/O banks
- Hard dynamic phase alignment (DPA) block with serializer/deserializer (SERDES)
- De-skew, read and write leveling, and clock-domain crossing functionality
- Programmable output current strength
- Programmable slew rate
- Programmable delay
- Programmable bus-hold
- Programmable pull-up resistor
- Open-drain output
- Serial, parallel, and dynamic on-chip termination (OCT)
- Differential OCT
- Programmable pre-emphasis
- Programmable differential output voltage (V_{OD})

Figure 9 20. Invalid Placement of DPA-Enabled Differential I/Os Driven by Both Center Left/Right PLLs



f For more information about programming serial configuration devices and fast AS Configuration Timing, refer to the Serial Configuration Devices (EPCS1, EPCS4, EPCS16, EPCS64, and EPCS128) Data Sheet in the Configuration Handbook.

Passive Serial Configuration

You can program PS configuration of Stratix III devices using an intelligent host, such as a MAX II device or microprocessor with flash memory, or a download cable. In the PS scheme, an external host (a MAX II device, embedded processor, or host PC) controls configuration. Configuration data is clocked into the target Stratix III device by using the DATA0 pin at each rising edge of DCLK.

1 The Stratix III decompression and design security features are fully available when configuring your Stratix III device using PS mode.

Table 11–9 lists the MSEL pin settings when using the PS configuration scheme.

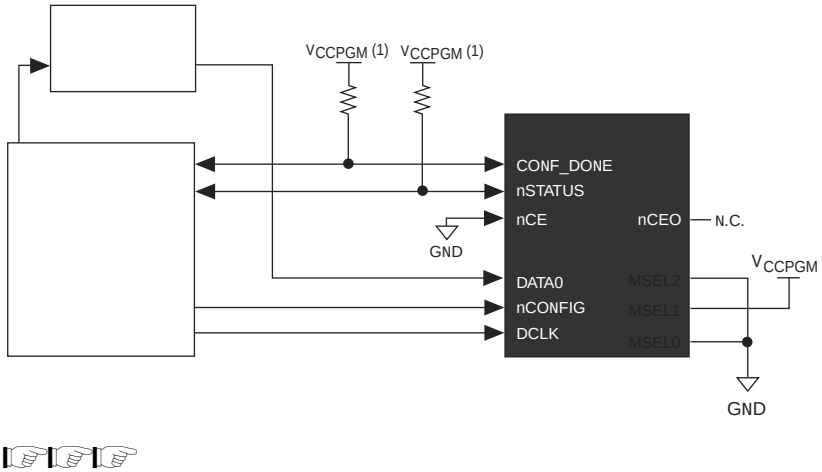
Table 11–9. Stratix III MSEL Pin Settings for PS Configuration Scheme

Configuration Scheme	MSEL2	MSEL1	MSEL0
PS	0	1	0

PS Configuration Using a MAX II Device as an External Host

In this configuration scheme, you can use a MAX II device as an intelligent host that controls the transfer of configuration data from a storage device, such as flash memory, to the target Stratix III device. You can store configuration data in .rbf, .hex, or .ttf format. Figure 11–13 shows the configuration interface connections between a Stratix III device and a MAX II device for single device configuration.

Figure 11–13. Single Device PS Configuration Using an External Host



(1) Connect the resistor to a supply that provides an acceptable input signal for the Stratix III device. V_{CCPGM} must be high enough to meet the V_{IH} specification of the I/O on the external host. It is recommended to power up all configuration systems' I/O with V_{CCPGM}.