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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8000
Number of Logic Elements/Cells	200000
Total RAM Bits	10901504
Number of I/O	744
Number of Gates	-
Voltage - Supply	0.86V ~ 1.15V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep3sl200f1152c3n

Stratix III devices have up to 112 DSP blocks. The architectural highlights of the Stratix III DSP block are the following:

- High-performance, power optimized, fully pipelined multiplication operations
- Native support for 9-bit, 12-bit, 18-bit, and 36-bit word lengths
- Native support for 18-bit complex multiplications
- Efficient support for floating point arithmetic formats (24-bit for Single Precision and 53-bit for Double Precision)
- Signed and unsigned input support
- Built-in addition, subtraction, and accumulation units to efficiently combine multiplication results
- Cascading 18-bit input bus to form tap-delay lines
- Cascading 44-bit output bus to propagate output results from one block to the next block
- Rich and flexible arithmetic rounding and saturation units
- Efficient barrel shifter support
- Loopback capability to support adaptive filtering

DSP block multipliers can optionally feed an adder/subtractor or accumulator in the block depending on user configuration. This option saves ALM routing resources and increases performance, because all connections and blocks are inside the DSP block. Additionally, the DSP Block input registers can efficiently implement shift registers for FIR filter applications, and the Stratix III DSP blocks support rounding and saturation. The Quartus II software includes megafunctions that control the mode of operation of the DSP blocks based on user parameter settings.

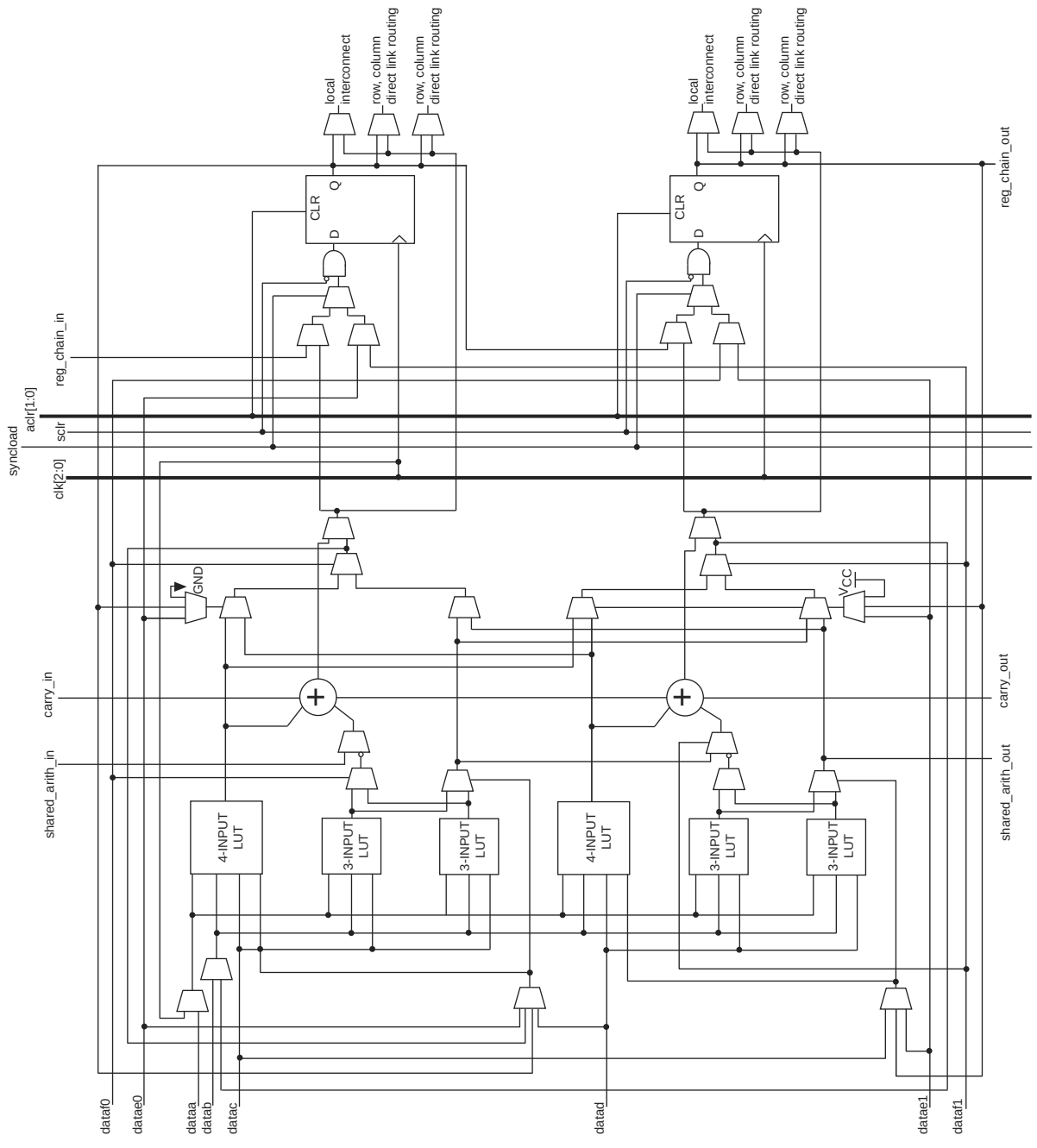
For more information, refer to the *DSP Blocks in Stratix III Devices* chapter.

Clock Networks and PLLs

Stratix III devices provide dedicated Global Clock Networks (GCLKs), Regional Clock Networks (RCLKs), and Periphery Clock Networks (PCLKs). These clocks are organized into a hierarchical clock structure that provides up to 104 unique clock domains (16 GCLK + 88 RCLK) within the Stratix III device and allows for up to 38 (16 GCLK + 22 RCLK) unique GCLK/RCLK clock sources per device quadrant.

Stratix III devices deliver abundant PLL resources with up to 12 PLLs per device and up to 10 outputs per PLL. Every output can be independently programmed, creating a unique, customizable clock frequency. Inherent jitter filtration and fine granularity control over multiply, divide ratios, and dynamic phase-shift reconfiguration provide the high-performance precision required in today's high-speed applications. Stratix III PLLs are feature rich, supporting advanced capabilities such as clock switchover, reconfigurable phase shift, PLL reconfiguration, and reconfigurable bandwidth. PLLs can be used for general-purpose clock management supporting multiplication, phase shifting, and programmable duty cycle. Stratix III PLLs also support external feedback mode, spread-spectrum input clock tracking, and post-scale counter cascading.

Figure 2–6. Stratix III ALM Details



One ALM contains two programmable registers. Each register has data, clock, clock enable, synchronous and asynchronous clear, and synchronous load/clear inputs. Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable. For combinational functions, the register is bypassed and the output of the LUT drives directly to the outputs of an ALM.

Table 4–8 lists the possible M144K block mixed-port width configurations in true dual-port mode.

Table 4–8. Stratix III M144K Block Mixed-Width Configurations (True Dual-Port Mode)

Read Port	Write Port					
	16K×8	8K×16	4K×32	16K×9	8K×18	4K×36
16K×8	✓	✓	✓	—	—	—
8K×16	✓	✓	✓	—	—	—
4K×32	✓	✓	✓	—	—	—
16K×9	—	—	—	✓	✓	✓
8K×18	—	—	—	✓	✓	✓
4K×36	—	—	—	✓	✓	✓

In true dual-port mode, M9K and M144K blocks support separate write-enable and read-enable signals. You can save power by keeping the read-enable signal low (inactive) when not reading. Read-during-write operations to the same address can either output new data at that location or old data. To choose the desired behavior, set the read-during-write behavior to either new data or old data in the RAM MegaWizard Plug-In Manager in the Quartus II software. See "Read During Write" on page 4–21 for more details about this behavior.

In true dual-port mode you can access any memory location at any time from either port. When accessing the same memory location from both ports, you must avoid possible write conflicts. A write conflict happens when you attempt to write to the same address location from both ports at the same time. This results in unknown data being stored to that address location. No conflict resolution circuitry is built into the Stratix III TriMatrix memory blocks. You must handle address conflicts external to the RAM block.

Figure 4–16 shows the true dual-port timing waveforms for the write operation at port A and read operation at port B with the Read-During-Write behavior set to new data. Registering the RAM's outputs would simply delay the q outputs by one clock cycle.

5. DSP Blocks in Stratix III Devices

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Introduction

The Stratix® III family of devices have dedicated high-performance digital signal processing (DSP) blocks optimized for DSP applications. These DSP blocks of the Altera® Stratix device family are the third generation of hardwired, fixed function silicon blocks dedicated to maximizing signal processing capability, ease of use, and lowest silicon cost.

Many complex systems such as WiMAX, 3GPP WCDMA, high-performance computing (HPC), voice over Internet protocol (VoIP), H.264 video compression, medical imaging, and HDTV use sophisticated digital signal processing techniques, and this typically requires a large number of mathematical computations. Stratix III devices are ideally suited as the DSP blocks consist of a combination of dedicated elements that perform multiplication, addition, subtraction, accumulation, summation, and dynamic shift operations. Along with the high-performance Stratix III soft logic fabric and TriMatrix™ memory structures, you can configure these blocks to build sophisticated fixed-point and floating-point arithmetic functions. These can be manipulated easily to implement common larger computationally intensive subsystems such as finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, and discrete cosine transform (DCT) functions.

DSP Block Overview

Each Stratix III device has two to seven columns of DSP blocks that implement multiplication, multiply-add, multiply-accumulate (MAC), and dynamic shift functions efficiently. The logical functionality of the Stratix III DSP block is a superset of the previous generation of the DSP block found in Stratix and Stratix II devices.

Architectural highlights of the Stratix III DSP block include:

- High-performance, power-optimized, fully registered and pipelined multiplication operations
- Natively supported 9-bit, 12-bit, 18-bit, and 36-bit wordlengths
- Natively supported 18-bit complex multiplications
- Efficiently supported floating-point arithmetic formats (24-bit for single precision and 53-bit for double precision)
- Signed and unsigned input support
- Built-in addition, subtraction, and accumulation units to combine multiplication results efficiently
- Cascading 18-bit input bus to form tap-delay line for filtering applications
- Cascading 44-bit output bus to propagate output results from one block to the next block without external logic support
- Rich and flexible arithmetic rounding and saturation units

The structure shown in Figure 5–2 is very useful for building more complex structures, such as complex multipliers and 36 × 36 multipliers, as described in later sections.

Each Stratix III DSP block contains four Two-Multiplier Adder units (two Two-Multiplier Adder units per half-block). Therefore, there are eight 18 × 18 multiplier functionalities per DSP block.

Following the Two-Multiplier Adder units are the pipeline registers, the second-stage adders, and an output register stage. You can configure the second-stage adders to provide the following alternative functions per Half-Block:

Equation 5–2. Four-Multiplier Adder Equation

$$Z[37..0] = P_0[36..0] + P_1[36..0]$$

Equation 5–3. Four-Multiplier Adder Equation (44-Bit Accumulation)

$$W_n[43..0] = W_{n-1}[43..0] \pm Z_n[37..0]$$

In these equations, *n* denotes sample time, and P[36..0] are the results from the Two-Multiplier Adder units.

Equation 5–2 provides a sum of four 18-bit × 18-bit multiplication operations (Four-Multiplier Adder), and Equation 5–3 provides a four 18-bit × 18-bit multiplication operation but with maximum of a 44-bit accumulation capability by feeding the output of the unit back to itself. This is shown in Figure 5–3.

You can bypass all register stages depending on which mode you select.

Table 6–13. PLL Output Signals (Part 2 of 2)

Port	Description	Source	Destination
scandone	Signal indicating when the PLL has completed reconfiguration. One-to-0 transition indicates that the PLL has been reconfigured.	PLL scan chain	Logic array
phasedone	When asserted it indicates that the phase reconfiguration is complete and the PLL is ready to act on a possible second reconfiguration. Asserts based on internal PLL timing. De-asserts on rising edge of SCANCLK.	PLL scan chain	Logic array
fbout	Output of m counter. Used for clock delay compensation.	M counter	Logic array

Clock Feedback Modes

Stratix III PLLs support up to six different clock feedback modes. Each mode allows clock multiplication and division, phase shifting, and programmable duty cycle. Table 6–14 lists the clock feedback modes supported by Stratix III PLLs.

Table 6–14. Clock Feedback Mode Availability

Clock Feedback Mode	Availability	
	Top/Bottom PLLs	Left/Right PLLs
Source-synchronous mode	Yes	Yes
No-compensation mode	Yes	Yes
Normal mode	Yes	Yes
Zero-delay buffer (ZDB) mode	Yes	Yes
External feedback mode *(2)*	Yes *(3)*	Yes *(1)*
LVDS compensation	No	Yes

Notes to Table 6–14:

(1) External feedback mode supported for single-ended inputs and outputs only on Left/Right PLLs.

(2) High-bandwidth PLL settings are not supported in external feedback mode. Select a "low" or "medium" PLL bandwidth in the ALTPLL MegaWizard™ Plug-in Manager when using PLLs in external feedback mode.

(3) Differential HSTL and SSTL I/O standards are not supported in Top/Bottom PLLs for external feedback mode.

The input and output delays are fully compensated by a PLL only when they are using the dedicated clock input pins associated with a given PLL as the clock source. Input and output delays are not compensated when cascading two adjacent top or bottom PLLs even if they are using dedicated routing for cascading. For example, when using PLL_T1 in normal mode, the clock delays from the input pin to the PLL clock output-to-destination register are fully compensated provided the clock input pin is one of the following four pins: CLK12, CLK13, CLK14, or CLK15. When an RCLK or GCLK network drives the PLL, the input and output delays may not be fully compensated in the Quartus II software.

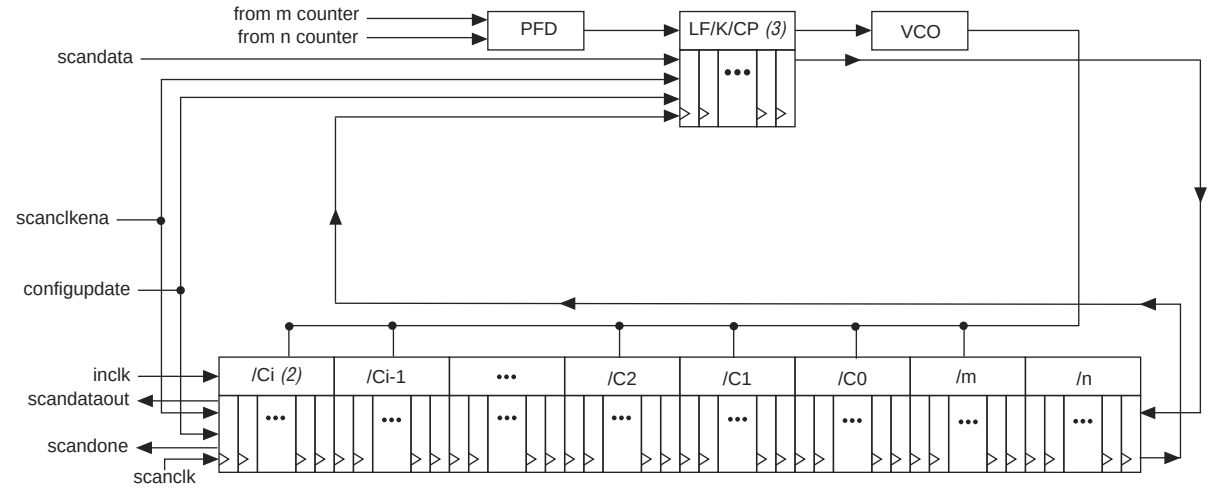
PLL Reconfiguration Hardware Implementation

The following PLL components are reconfigurable in real time:

- Pre-scale counter (n)
- Feedback counter (m)
- Post-scale output counters (C0 – C9)
- Post VCO Divider (K)
- Dynamically adjust the charge-pump current (I_{cp}) and loop-filter components (R, C) to facilitate reconfiguration of the PLL bandwidth

Figure 6–40 shows how PLL counter settings can be dynamically adjusted by shifting their new settings into a serial shift-register chain or scan chain. Serial data is input to the scan chain via the scandataport and shift registers are clocked by scanclk. The maximum scanclk frequency is 100 MHz. Serial data is shifted through the scan chain as long as the scanclkena signal stays asserted. After the last bit of data is clocked, asserting the configupdate signal for at least one scanclk clock cycle causes the PLL configuration bits to be synchronously updated with the data in the scan registers.

Figure 6–40. PLL Reconfiguration Scan Chain



Notes to Figure 6–40:

(1) The Stratix III Left/Right PLLs support C0 - C6 counters.

(2) i = 6 or i = 9.

(3) This figure shows the corresponding scan register for the K counter in between the scan registers for the charge pump and loop filter. The K counter is physically located after the VCO.

The counter settings are updated synchronously to the clock frequency of the individual counters. Therefore, all counters are not updated simultaneously.

Table 7–1. I/O Standard Applications for Stratix III Devices (Part 2 of 2)

I/O Standard	Typical Application
mini-LVDS	Flat panel display
LVPECL	Video graphics and clock distribution

I/O Standards and Voltage Levels

Stratix III devices support a wide range of industry I/O standards, including single-ended, voltage-referenced single-ended, and differential I/O standards.

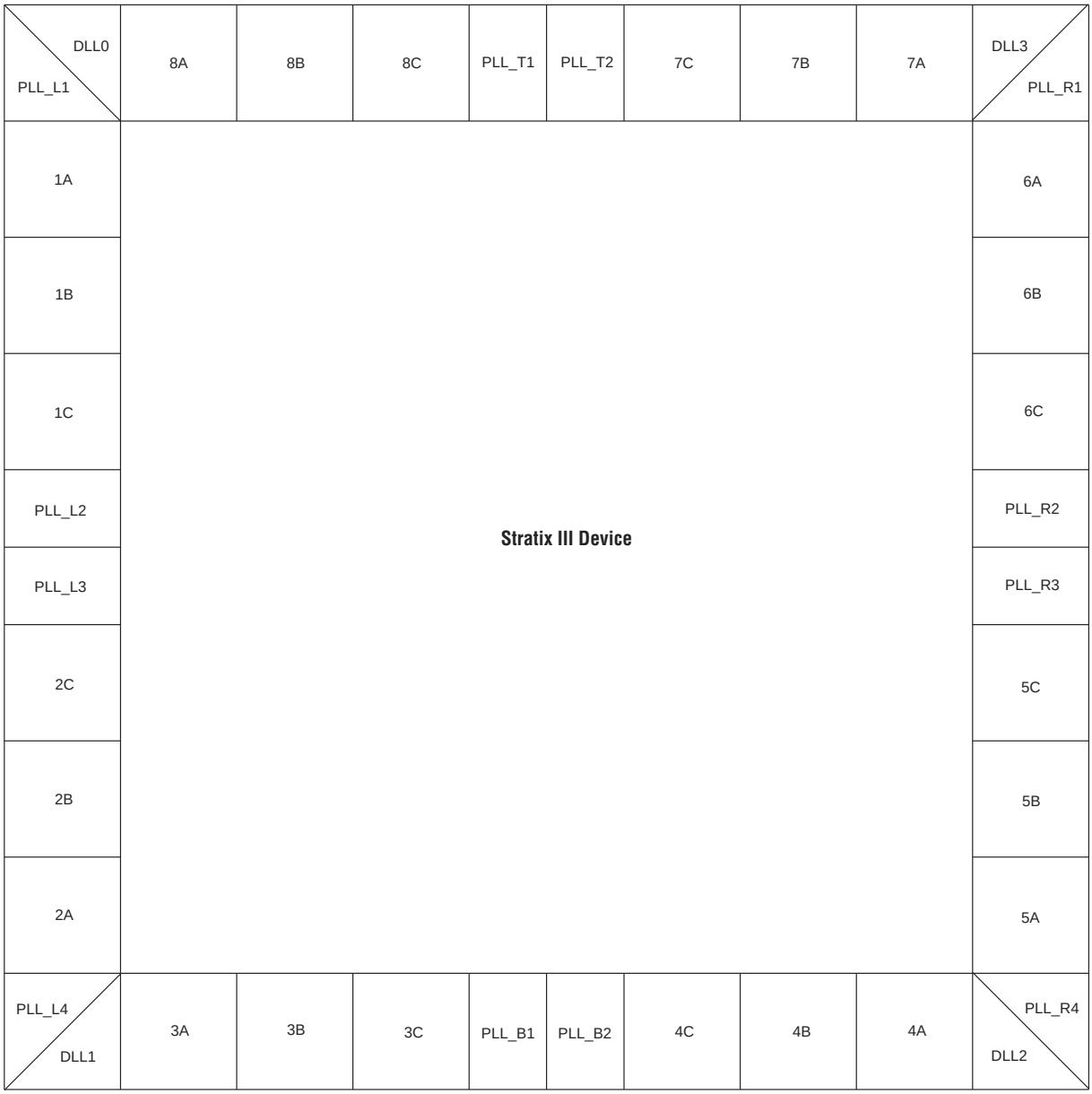
Table 7–2 lists the supported I/O standards and the typical values for input and output V_{CCIO}, V_{CCPD}, V_{REF}, and board V_{TT}.

Table 7–2. I/O Standards and Voltage Levels for Stratix III Devices *(Note 1)*, *(3)* (Part 1 of 3)

I/O Standard	Standard Support	V_{CCIO} (V)				V_{CCPD} (V) (Pre-Driver Voltage)	V_{REF} (V) (Input Ref Voltage)	V_{TT} (V) (Board Termination Voltage)
		Input Operation		Output Operation				
		Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks			
3.3-V LVTTL	JESD8-B	3.3/3.0/2.5	3.3/3.0/2.5	3.3	3.3	3.3	—	—
3.3-V LVCMOS	JESD8-B	3.3/3.0/2.5	3.3/3.0/2.5	3.3	3.3	3.3	—	—
3.0-V LVTTL	JESD8-B	3.3/3.0/2.5	3.3/3.0/2.5	3.0	3.0	3.0	—	—
3.0-V LVCMOS	JESD8-B	3.3/3.0/2.5	3.3/3.0/2.5	3.0	3.0	3.0	—	—
2.5-V LVTTL/LVCMOS	JESD8-5	3.3/3.0/2.5	3.3/3.0/2.5	2.5	2.5	2.5	—	—
1.8-V LVTTL/LVCMOS	JESD8-7	1.8/1.5	1.8/1.5	1.8	1.8	2.5	—	—
1.5-V LVTTL/LVCMOS	JESD8-11	1.8/1.5	1.8/1.5	1.5	1.5	2.5	—	—
1.2-V LVTTL/LVCMOS	JESD8-12	1.2	1.2	1.2	1.2	2.5	—	—
3.0-V PCI	PCI Rev 2.2	3.0	3.0	3.0	3.0	3.0	—	—
3.0-V PCI-X	PCI-X Rev 1.0	3.0	3.0	3.0	3.0	3.0	—	—
SSTL-2 Class I	JESD8-9B	*(2)*	*(2)*	2.5	2.5	2.5	1.25	1.25
SSTL-2 Class II	JESD8-9B	*(2)*	*(2)*	2.5	2.5	2.5	1.25	1.25
SSTL-18 Class I	JESD8-15	*(2)*	*(2)*	1.8	1.8	2.5	0.90	0.90
SSTL-18 Class II	JESD8-15	*(2)*	*(2)*	1.8	1.8	2.5	0.90	0.90
SSTL-15 Class I	—	*(2)*	*(2)*	1.5	1.5	2.5	0.75	0.75
SSTL-15 Class II	—	*(2)*	*(2)*	1.5	—	2.5	0.75	0.75
HSTL-18 Class I	JESD8-6	*(2)*	*(2)*	1.8	1.8	2.5	0.90	0.90
HSTL-18 Class II	JESD8-6	*(2)*	*(2)*	1.8	1.8	2.5	0.90	0.90
HSTL-15 Class I	JESD8-6	*(2)*	*(2)*	1.5	1.5	2.5	0.75	0.75
HSTL-15 Class II	JESD8-6	*(2)*	*(2)*	1.5	—	2.5	0.75	0.75
HSTL-12 Class I	JESD8-16A	*(2)*	*(2)*	1.2	1.2	2.5	0.6	0.6
HSTL-12 Class II	JESD8-16A	*(2)*	*(2)*	1.2	—	2.5	0.6	0.6

Figure 8–1 shows a package bottom view for Stratix III external memory support, showing the phase-locked loop (PLL), delay-locked loop (DLL), and I/O banks. The number of available I/O banks and PLLs depend on the device density.

Figure 8–1. Package Bottom View for Stratix III Devices *(Note 1), (2)*



Notes to Figure 8–1:

(1) The number of I/O banks and PLLs available depends on the device density.

(2) There is only one PLL in the center of each side of the device in EP3SL50, EP3SL70, and EP3SE50 devices.

Data and Data-Strobe/Clock Pins

Read data-strobes or clocks are called DQS pins. Depending on the memory specifications, DQS pins can be bi-directional single-ended signals (in DDR2 and DDR SDRAM), uni-directional differential signals (in RLDRAM II), bi-directional differential signals (DDR3 and DDR2 SDRAM), or uni-directional complementary signals (QDR II+ and QDR II SRAM). Connect the uni-directional read and write data-strobes or clocks to Stratix III DQS pins.

Stratix III devices offer differential input buffers for differential read data-strobe/clock operations and provide an independent DQS logic block for each CQn pin for complementary read data-strobe/clock operations. The differential DQS pin-pairs are denoted as DQS and DQSn pins, while the complementary DQS signals are denoted as CQ and CQn pins. DQSn and CQn pins are marked separately in the pin table. Each CQn pin connects to a DQS logic block and the shifted CQn signals go to the negative-edge input registers in the IOE registers.

☞ Use differential DQS signaling for DDR2 SDRAM interfaces running higher than 333 MHz.

☞ For DDR3 and DDR2 SDRAM application, pseudo-differential DQS signaling is used for write operation.

Stratix III DDR memory interface data pins are called DQ pins. DQ pins can be bi-directional signals (in DDR3, DDR2, and DDR SDRAM, and RLDRAM II common I/O (CIO) interfaces), or uni-directional signals (in QDR II+, QDR II SRAM, and RLDRAM II separate I/O (SIO) devices). Connect the uni-directional read data signals to Stratix III DQ pins and the uni-directional write data signals to a different DQS/DQ group other than the read DQS/DQ group. You must assign the write clocks to the DQS/DQSn pins associated to this write DQS/DQ group. Do not use the CQ/CQn pin-pair for write clocks.

☞ Using a DQS/DQ group for write data signals minimizes output skew, allows access to the write leveling circuitry (for DDR3 SDRAM interfaces), and allows for vertical migration. These pins also have access to deskewing circuitry that can compensate for delay mismatch between signals on the bus.

For more information about pin planning, refer to *Section I. Device and Pin Planning* chapter in volume 2 of the *External Memory Interface Handbook*.

The DQS and DQ pin locations are fixed in the pin table. Memory interface circuitry is available in every Stratix III I/O bank. All memory interface pins support the I/O standards required to support DDR3, DDR2, DDR SDRAM, QDR II+, QDR II SRAM, and RLDRAM II devices.

The Stratix III device supports DQS and DQ signals with DQ bus modes of ×4, ×8/×9, ×16/×18, or ×32/×36, although not all devices support DQS bus mode ×32/×36. When any of these pins are not used for memory interfacing, you can use them as user I/Os. In addition, you can use any DQSn or CQn pins not used for clocking as DQ (data) pins. Table 8–1 lists pin support per DQS/DQ bus mode, including the DQS/CQ and DQSn/CQn pin pair.

Source-Synchronous Timing Budget

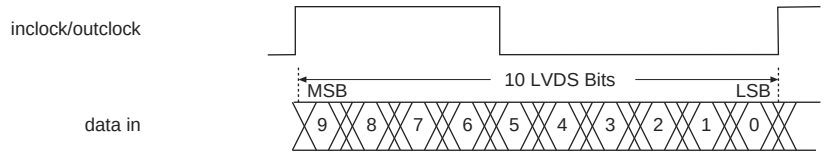
This section discusses the timing budget, waveforms, and specifications for source-synchronous signaling in Stratix III devices. LVDS I/O standards enable high-speed data transmission. This high data transmission rate results in better overall system performance. To take advantage of fast system performance, it is important to understand how to analyze timing for these high-speed signals. Timing analysis for the differential block is different from traditional synchronous timing analysis techniques.

Rather than focusing on clock-to-output and setup times, source synchronous timing analysis is based on the skew between the data and the clock signals. High-speed differential data transmission requires the use of timing parameters provided by IC vendors and is strongly influenced by board skew, cable skew, and clock jitter. This section defines the source-synchronous differential data orientation timing parameters, the timing budget definitions for Stratix III devices, and ways to use these timing parameters to determine the maximum performance of your design.

Differential Data Orientation

There is a set relationship between an external clock and the incoming data. For an operation at 1 Gbps and SERDES factor of 10, the external clock is multiplied by 10, and phase-alignment can be set in the PLL to coincide with the sampling window of each data bit. The data is sampled on the falling edge of the multiplied clock. Figure 9–15 shows the data bit orientation of the ×10 mode.

Figure 9–15. Bit Orientation in Quartus II Software



Differential I/O Bit Position

Data synchronization is necessary for successful data transmission at high frequencies. Figure 9–16 shows the data bit orientation for a channel operation. These figures are based on the following:

- SERDES factor equals clock multiplication factor
- Edge alignment is selected for phase alignment
- Implemented in hard SERDES

For other serialization factors, use the Quartus II software tools and find the bit position within the word and the bit positions after deserialization.

Section III. Hot Socketing, Configuration, Remote Upgrades, and Testing

This section provides information on hot socketing and power-on reset, configuring Stratix® III devices, remote system upgrades, and IEEE 1149.1 (JTAG) Boundary-Scan Testing in the following sections:

- Chapter 10, Hot Socketing and Power-On Reset in Stratix III Devices
- Chapter 11, Configuring Stratix III Devices
- Chapter 12, Remote System Upgrades with Stratix III Devices
- Chapter 13, IEEE 1149.1 (JTAG) Boundary-Scan Testing in Stratix III Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

I/O Pins Remain Tri-Stated During Power Up

A device that does not support hot socketing can interrupt system operation or cause contention by driving out before or during power up. In a hot-socketing situation, the Stratix III device's output buffers are turned off during system power up or power down. Also, the Stratix III device does not drive out until the device is configured and working within recommended operating conditions.

Insertion or Removal of a Stratix III Device from a Powered-Up System

Devices that do not support hot socketing can short power supplies when powered up through the device signal pins. This irregular power up can damage both the driving and driven devices and can disrupt card power up.

You can insert a Stratix III device into or remove it from a powered-up system board without damaging the system board or interfering with its operation.

You can power up or power down the core voltage supplies (V_{CC}, V_{CCL}, V_{CCPT}, V_{CCA_PLL}, and V_{CCD_PLL}), V_{CCIO}, V_{CCPMG}, V_{CC_CLKIN}, and V_{CCPD} supplies in any sequence and at any time between them. The individual power supply ramp-up and ramp-down rates can range from 50 µs to 12 ms or 100 ms depending on the PORSEL setting. During hot socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

For more information about the hot socketing specification, refer to the *DC and Switching Characteristics of Stratix III Devices* chapter and the *Hot-Socketing and Power-Sequencing Feature and Testing for Altera Devices White Paper.*

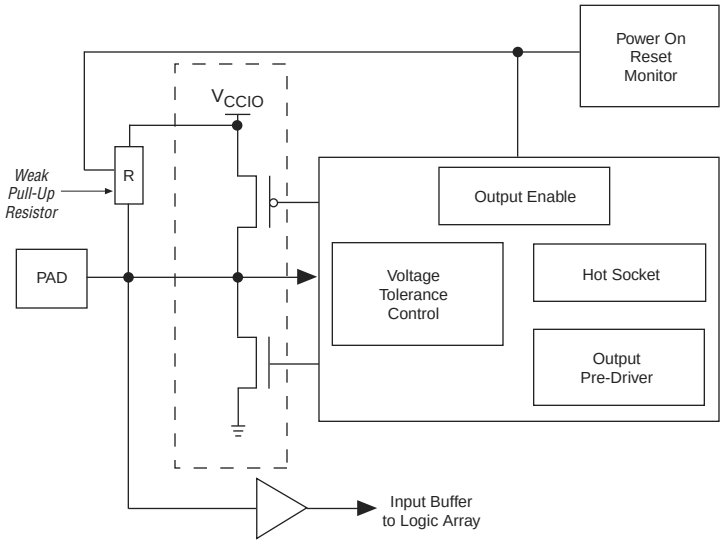
A possible concern regarding hot socketing is the potential for "latch-up". Nevertheless, Stratix III devices are immune to latch-up when hot socketing. Latch-up can occur when electrical subsystems are hot socketed into an active system. During hot socketing, the signal pins can be connected and driven by the active system before the power supply can provide current to the device's power and ground planes. This condition can lead to latch-up and cause a low-impedance path from power to ground within the device. As a result, the device draws a large amount of current, possibly causing electrical damage.

Hot-Socketing Feature Implementation in Stratix III Devices

The hot-socketing feature turns off the output buffer during power up and power down of the V_{CC}, V_{CCIO}, V_{CCPGM}, or V_{CCPD} power supplies. The hot-socketing circuitry generates an internal `HOTSCKT` signal when the V_{CC}, V_{CCIO}, V_{CCPGM}, or V_{CCPD} power supplies are below the threshold voltage. Hot-socketing circuitry is designed to prevent excess I/O leakage during power up. When the voltage ramps up very slowly, it is still relatively low, even after the POR signal is released and the configuration is completed. The `CONF_DONE`, `nCEO`, and `nSTATUS` pins fail to respond, as the output buffer cannot flip from the state set by the hot-socketing circuit at this low voltage. Therefore, the hot-socketing circuit has been removed on these configuration pins to make sure that they are able to operate during configuration. Thus, it is expected behavior for these pins to drive out during power-up and power-down sequences.

Figure 10–1 shows the Stratix III device's I/O pin circuitry.

Figure 10–1. Hot-Socketing Circuitry for Stratix III Devices



The POR circuit monitors the voltage level of power supplies (V_{CC}, V_{CCL}, V_{CCPD}, V_{CCPGM} and V_{CCPT}) and keeps the I/O pins tri-stated until the device is in user mode. The weak pull-up resistor (R) in the Stratix III input/output element (IOE) keeps the I/O pins from floating. The 3.3-V tolerance control circuit permits the I/O pins to be driven by 3.3 V before V_{CCIO}, V_{CC}, V_{CCPD}, and/or V_{CCPGM} supplies are powered, and it prevents the I/O pins from driving out when the device is not in user mode.

Altera uses GND as reference for hot-socketing operation and I/O buffer designs. To ensure proper operation, you must connect the GND between boards before connecting the power supplies. This will prevent the GND on your board from being pulled up inadvertently by a path to power through other components on your board. A pulled up GND could otherwise cause an out-of-specification I/O voltage or current condition with the Altera device.

Table 11–10. PS Timing Parameters for Stratix III Devices (Part 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units
t	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode *(2)*	20	100	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	tCD2CU + (4,436 × CLKUSR period)	—	—

Notes to Table 11–10:

(1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for starting the device.

Device configuration options and how to create configuration files are discussed further in the *Device Configuration Options and Configuration File Formats* chapters in volume 2 of the *Configuration Handbook*.

PS Configuration Using a Microprocessor

In this PS configuration scheme, a microprocessor can control the transfer of configuration data from a storage device, such as flash memory, to the target Stratix III device.

You can do a PS configuration using MicroBlaster™ Passive Serial Software Driver. For more information, refer to *AN423: Configuring the MicroBlaster Passive Serial Software Driver*.

For all configuration and timing information, refer to "PS Configuration Using a MAX II Device as an External Host" on page 11–27. This section is also applicable when using a microprocessor as an external host.

PS Configuration Using a Download Cable

In this section, the generic term *download cable* includes the Altera USB-Blaster USB port download cable, MasterBlaster™ serial/USB communications cable, ByteBlaster II parallel port download cable, ByteBlasterMV™ parallel port download cable, and the EthernetBlaster download cable.

In PS configuration with a download cable, an intelligent host (such as a PC) transfers data from a storage device to the device by using the USB-Blaster, MasterBlaster, ByteBlaster II, EthernetBlaster, or ByteBlasterMV cable.

IEEE Std. 1149.1 BST Operation Control

Stratix III devices support the IEEE Std. 1149.1 (JTAG) instructions listed in Table 13–4.

Table 13–4. Stratix III JTAG Instructions

JTAG Instruction	Instruction Code	Description
SAMPLE / PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap® II embedded logic analyzer.
EXTEST *(1)*	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Places the 32-bit device identification register between TDI and TDO. The USERCODE value are loaded into this Device ID register for shifting out through TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions	—	Used when configuring a Stratix III device through the JTAG port with a USB-Blaster™, ByteBlaster™ II, MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code (JBC) File through an embedded processor.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO	00 0000 1101	Allows I/O reconfiguration through JTAG ports using the IOCSR for JTAG testing. Can be executed before, after, or during configurations.

Note to Table 13–4:

(1) Bus hold and weak pull-up resistor features override the high-impedance state of the HIGHZ, CLAMP, and EXTEST instructions.

The IEEE Std. 1149.1 TAP controller, a 16-state machine clocked on the rising edge of TCK, uses the TMS pin to control IEEE Std. 1149.1 operation in the device. Figure 13–5 shows the TAP controller state machine.