# Intel - EP3SL200F1517C3N Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 8000 |
| Number of Logic Elements/Cells | 200000 |
| Total RAM Bits | 10901504 |
| Number of I/O | 976 |
| Number of Gates | - |
| Voltage - Supply | 0.86V ~ 1.15V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1517-BBGA, FCBGA |
| Supplier Device Package | 1517-FBGA (40x40) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep3sl200f1517c3n |

## Chapter 3. MultiTrack Interconnect in Stratix III Devices



## Chapter 4. TriMatrix Embedded Memory Blocks in Stratix III Devices

# 1. Stratix III Device Family Overview

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The Stratix® III family provides one of the most architecturally advanced, high-performance, low-power FPGAs in the marketplace.

Stratix III FPGAs lower power consumption through Altera's innovative Programmable Power Technology, which provides the ability to turn on the performance where needed and turn down the power consumption for blocks not in use. Selectable Core Voltage and the latest in silicon process optimizations are also employed to deliver the industry's lowest power, high-performance FPGAs.

Specifically designed for ease of use and rapid system integration, the Stratix III FPGA family offers two variants optimized to meet different application needs:

- The Stratix III *L* family provides balanced logic, memory, and multiplier ratios for mainstream applications.
- The Stratix III *E* family is memory- and multiplier-rich for data-centric applications.

Modular I/O banks with a common bank structure for vertical migration lend efficiency and flexibility to the high-speed I/O. Package and die enhancements with dynamic on-chip termination, output delay, and current strength control provide best-in-class signal integrity.

Based on a 1.1-V, 65-nm all-layer copper SRAM process, the Stratix III family is a programmable alternative to custom ASICs and programmable processors for high-performance logic, digital signal processing (DSP), and embedded designs.

Stratix III devices include optional configuration bit stream security through volatile or non-volatile 256-bit Advanced Encryption Standard (AES) encryption. Where ultra-high reliability is required, Stratix III devices include automatic error detection circuitry to detect data corruption by soft errors in the configuration random-access memory (CRAM) and user memory cells.

## Features Summary

Stratix III devices offer the following features:

- 48,000 to 338,000 equivalent logic elements (LEs) (refer to Table 1–1)
- 2,430 to 20,497 Kbits of enhanced TriMatrix memory consisting of three RAM block sizes to implement true dual-port memory and FIFO buffers
- High-speed DSP blocks provide dedicated implementation of 9×9, 12×12, 18×18, and 36×36 multipliers (at up to 550 MHz), multiply-accumulate functions, and finite impulse response (FIR) filters
- I/O:GND:PWR ratio of 8:1:1 along with on-die and on-package decoupling for robust signal integrity
- Programmable Power Technology, which minimizes power while maximizing device performance

**Table 1–6.** Chapter Revision History (Part 2 of 2)

| Date | Version | Changes Made |
|---|---|---|
| May 2008 | 1.4 | ■ Updated "Introduction".<br>■ Updated Table 1–1.<br>■ Updated Table 1–2.<br>■ Added Table 1–5.<br>■ Updated "Reference and Ordering Information".<br>■ Updated package type information in Figure 1–1. |
| November 2007 | 1.3 | ■ Updated Table 1–1.<br>■ Updated Table 1–2. |
| October 2007 | 1.2 | ■ Minor typo fixes.<br>■ Added Table 1–4.<br>■ Added section "Referenced Documents".<br>■ Added live links for references. |
| May 2007 | 1.1 | Minor formatting changes, fixed PLL numbers and ALM, LE and MLAB bit counts in Table 1–1. |
| November 2006 | 1.0 | Initial Release. |

### Read/Write Clock Mode

Stratix III TriMatrix memory blocks can implement read/write clock mode for simple dual-port memories. In this mode, a write clock controls the data-input, write-address, and write-enable registers. Similarly, a read clock control the data-output, read-address, and read-enable registers. The memory blocks support independent clock enables for both the read and write clocks. Asynchronous clears are available on data output latches and registers only.

When using read/write mode, if you perform a simultaneous read/write to the same address location, the output read data will be unknown. If you require the output data to be a known value in this case, use either single-clock mode or input/output clock mode and choose the appropriate read-during-write behavior in the Megawizard.

### Single Clock Mode

Stratix III TriMatrix memory blocks can implement single-clock mode for true dual-port, simple dual-port, and single-port memories. In this mode, a single clock, together with a clock enable, is used to control all registers of the memory block. Asynchronous clears are available on output latches and output registers only.

## Design Considerations

This section describes guidelines for designing with TriMatrix memory blocks.

### Selecting TriMatrix Memory Blocks

The Quartus II software automatically partitions user-defined memory into embedded memory blocks by taking into account both speed and size constraints placed on your design. For example, the Quartus II software may spread out a memory across multiple memory blocks when resources are available to increase the performance of the design. You can manually assign the memory to a specific block size via the RAM MegaWizard Plug-In Manager.

MLABs can implement single-port SRAM through emulation via the Quartus II software. Emulation results in minimal additional logic resources being used. Because of the dual-purpose architecture of the MLAB, it only has data input registers and output registers in the block. MLABs gain input address registers and additional optional data output registers from adjacent ALMs by using register packing.

For more information about register packing, refer to the *Logic Array Blocks and Adaptive Logic Modules in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

### Conflict Resolution

When using the memory blocks in true dual-port mode, it is possible to attempt two write operations to the same memory location (address). Since no conflict resolution circuitry is built into the memory blocks, this results in unknown data being written to that location. Therefore, you must implement conflict resolution logic external to the memory block to avoid address conflicts.

**Figure 5–15.** Loopback Mode for Half-DSP Block

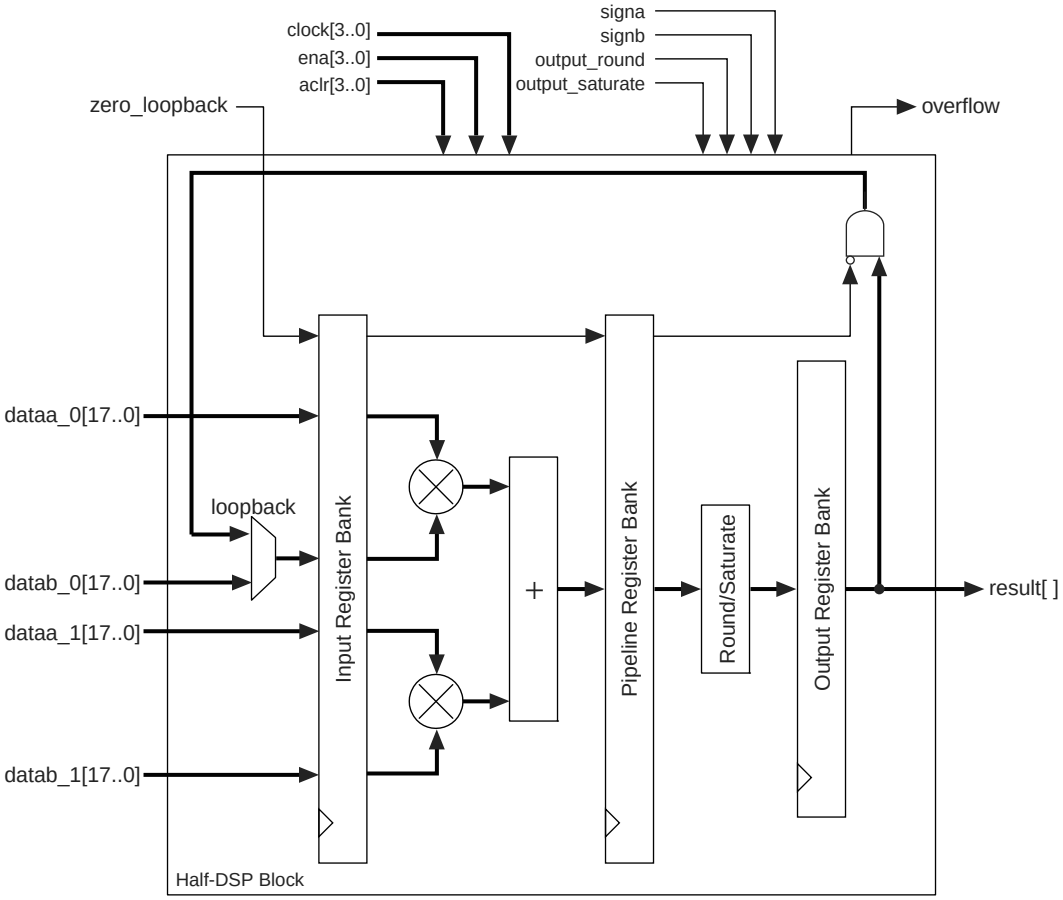
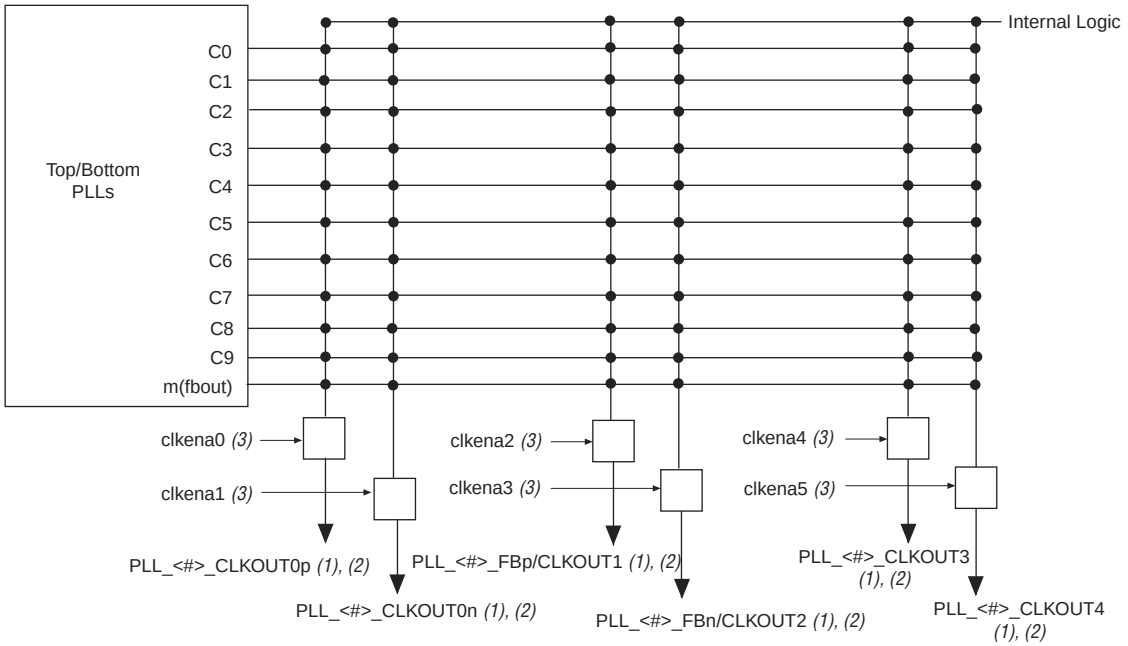


Figure 6–20 shows the clock I/O pins associated with Top/Bottom PLLs.

**Figure 6–20.** External Clock Outputs for Top/Bottom PLLs




**Notes to Figure 6–20:**

(1) These clock output pins can be fed by any one of the C[9..0], m counters.

(2) The CLKOUT0p and CLKOUT0n pins can be either single-ended or differential clock outputs. CLKOUT1 and CLKOUT2 pins are dual-purpose I/O pins that can be used as two single-ended outputs, one differential external feedback input pin pair or one single-ended external feedback input pin (CLKOUT1 only). CLKOUT3 and CLKOUT4 pins are two single-ended output pins.

(3) These external clock enable signals are available only when using the ALTCLKCTRL megafunction.

Any of the output counters (C[9..0] on Top/Bottom PLLs and C[6..0] on Left/Right PLLs) or the M counter can feed the dedicated external clock outputs, as shown in Figure 6–20 and Figure 6–21. Therefore, one counter or frequency can drive all output pins available from a given PLL.

Each Left/Right PLL supports two clock I/O pins, configured as either two single-ended I/Os or one differential I/O pair. When using both pins as single-ended I/Os, one of them can be the clock output while the other pin is the external feedback input (FB) pin. Hence, Left/Right PLLs only support external feedback mode for single-ended I/O standards.

# 7. Stratix III Device I/O Features

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Stratix® III I/Os are specifically designed for ease of use and rapid system integration while simultaneously providing the high bandwidth required to maximize internal logic capabilities and produce system-level performance. Independent modular I/O banks with a common bank structure for vertical migration lend efficiency and flexibility to the high speed I/O. Package and die enhancements with dynamic termination and output control provide best-in-class signal integrity. Numerous I/O features assist in high-speed data transfer into and out of the device, including:

- Single-ended, non-voltage-referenced, and voltage-referenced I/O standards
- Low-voltage differential signaling (LVDS), reduced swing differential signal (RSDS), mini-LVDS, high-speed transceiver logic (HSTL), and stub series terminated logic (SSTL)
- Single data rate (SDR) and half data rate (HDR—half frequency and twice data width of SDR) input and output options
- Up to 132-full duplex 1.6-Gbps true LVDS channels (132 Tx + 132 Rx) on the row I/O banks
- Hard dynamic phase alignment (DPA) block with serializer/deserializer (SERDES)
- De-skew, read and write leveling, and clock-domain crossing functionality
- Programmable output current strength
- Programmable slew rate
- Programmable delay
- Programmable bus-hold
- Programmable pull-up resistor
- Open-drain output
- Serial, parallel, and dynamic on-chip termination (OCT)
- Differential OCT
- Programmable pre-emphasis
- Programmable differential output voltage ($V_{OD}$)

# Stratix III I/O Standards Support

Stratix III devices support a wide range of industry I/O standards. Table 7–1 lists the I/O standards supported by Stratix III devices as well as typical applications. Stratix III devices support $V_{CCIO}$ voltage levels of 3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V.

**Table 7–1.** I/O Standard Applications for Stratix III Devices (Part 1 of 2)

| I/O Standard | Typical Application |
|---|---|
| 3.3-V LVTTL/LVCMOS | General purpose |
| 3.0-V LVTTL/LVCMOS | General purpose |
| 2.5-V LVTTL/LVCMOS | General purpose |
| 1.8-V LVTTL/LVCMOS | General purpose |
| 1.5-V LVTTL/LVCMOS | General purpose |
| 1.2-V LVTTL/LVCMOS | General purpose |
| 3.0-V PCI | PC and embedded system |
| 3.0-V PCI-X | PC and embedded system |
| SSTL-2 Class I | DDR SDRAM |
| SSTL-2 Class II | DDR SDRAM |
| SSTL-18 Class I | DDR2 SDRAM |
| SSTL-18 Class II | DDR2 SDRAM |
| SSTL-15 Class I | DDR3 SDRAM |
| SSTL-15 Class II | DDR3 SDRAM |
| HSTL-18 Class I | QDR II/RLDRAM II |
| HSTL-18 Class II | QDR II/RLDRAM II |
| HSTL-15 Class I | QDR II/QDR II+/RLDRAM II |
| HSTL-15 Class II | QDR II/QDR II+/RLDRAM II |
| HSTL-12 Class I | General purpose |
| HSTL-12 Class II | General purpose |
| Differential SSTL-2 Class I | DDR SDRAM |
| Differential SSTL-2 Class II | DDR SDRAM |
| Differential SSTL-18 Class I | DDR2 SDRAM |
| Differential SSTL-18 Class II | DDR2 SDRAM |
| Differential SSTL-15 Class I | DDR3 SDRAM |
| Differential SSTL-15 Class II | DDR3 SDRAM |
| Differential HSTL-18 Class I | Clock interfaces |
| Differential HSTL-18 Class II | Clock interfaces |
| Differential HSTL-15 Class I | Clock interfaces |
| Differential HSTL-15 Class II | Clock interfaces |
| Differential HSTL-12 Class I | Clock interfaces |
| Differential HSTL-12 Class II | Clock interfaces |
| LVDS | High-speed communications |
| RSDS | Flat panel display |

**Table 7–2.** I/O Standards and Voltage Levels for Stratix III Devices *(Note 1), (3)* (Part 2 of 3)

| I/O Standard | Standard Support | $V_{CCIO}$ (V) | | | | $V_{CCPD}$ (V) (Pre-Driver Voltage) | $V_{REF}$ (V) (Input Ref Voltage) | $V_{TT}$ (V) (Board Termination Voltage) |
|---|---|---|---|---|---|---|---|---|
| | | Input Operation | | Output Operation | | | | |
| | | Column I/O Banks | Row I/O Banks | Column I/O Banks | Row I/O Banks | | | |
| Differential SSTL-2 Class I | JESD8-9B | *(2)* | *(2)* | 2.5 | 2.5 | 2.5 | — | 1.25 |
| Differential SSTL-2 Class II | JESD8-9B | *(2)* | *(2)* | 2.5 | 2.5 | 2.5 | — | 1.25 |
| Differential SSTL-18 Class I | JESD8-15 | *(2)* | *(2)* | 1.8 | 1.8 | 2.5 | — | 0.90 |
| Differential SSTL-18 Class II | JESD8-15 | *(2)* | *(2)* | 1.8 | 1.8 | 2.5 | — | 0.90 |
| Differential SSTL-15 Class I | — | *(2)* | *(2)* | 1.5 | 1.5 | 2.5 | — | 0.75 |
| Differential SSTL-15 Class II | — | *(2)* | *(2)* | 1.5 | — | 2.5 | — | 0.75 |
| Differential HSTL-18 Class I | JESD8-6 | *(2)* | *(2)* | 1.8 | 1.8 | 2.5 | — | 0.90 |
| Differential HSTL-18 Class II | JESD8-6 | *(2)* | *(2)* | 1.8 | 1.8 | 2.5 | — | 0.90 |
| Differential HSTL-15 Class I | JESD8-6 | *(2)* | *(2)* | 1.5 | 1.5 | 2.5 | — | 0.75 |
| Differential HSTL-15 Class II | JESD8-6 | *(2)* | *(2)* | 1.5 | — | 2.5 | — | 0.75 |
| Differential HSTL-12 Class I | JESD8-16A | *(2)* | *(2)* | 1.2 | 1.2 | 2.5 | — | 0.60 |
| Differential HSTL-12 Class II | JESD8-16A | *(2)* | *(2)* | 1.2 | — | 2.5 | — | 0.60 |
| LVDS *(6), (8)* | ANSI/TIA/EIA-644 | *(2)* | *(2)* | 2.5 | 2.5 | 2.5 | — | — |
| RSDS *(6), (7), (8)* | — | *(2)* | *(2)* | 2.5 | 2.5 | 2.5 | — | — |
| mini-LVDS *(6), (7), (8)* | — | *(2)* | *(2)* | 2.5 | 2.5 | 2.5 | — | — |

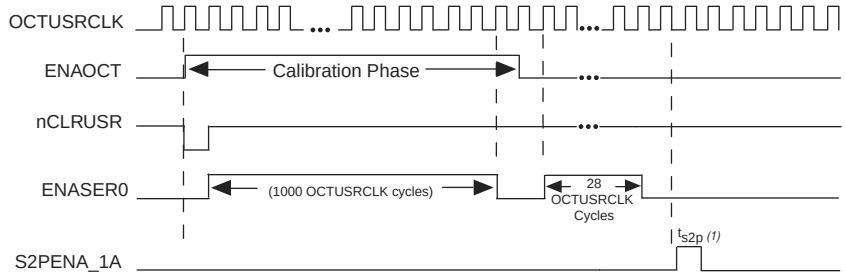
## OCT Calibration

Figure 7–18 shows the user-mode signal-timing waveforms. To calibrate OCT block[N] (where N is a calibration block number), you must assert ENAOCT one cycle before asserting ENASER[N]. Also, nCLRUSR must be set to low for one OCTUSRCLK cycle before ENASER[N] signal is asserted. An asserted ENASER[N] signals for 1000 OCTUSRCLK cycles to perform $OCTR_S$ and $OCTR_T$ calibration. ENAOCT can be deasserted one clock cycle after the last ENASER is deasserted.

## Serial Data Transfer

When calibration is complete, you must serially shift out the 28-bit OCT calibration code (14-bit OCT RS code and 14-bit OCT RT) from each OCT calibration block to the corresponding I/O buffers. Only one OCT calibration block can send out the codes at any given time by asserting only one ENASER[N] signal at a time. After ENAOCT is deasserted, you must wait at least 1 OCTUSRCLK cycle to enable any ENASER[N] signal to begin serial transfer. To shift 28-bit code from OCT calibration block[N], ENASER[N] must be asserted for exactly 28 OCTUSRCLK cycles. There must be at least one OCTUSRCLK cycle gap between two consecutive asserted ENASER signals. For these requirements, refer to Figure 7–18.

**Figure 7–18.** OCT User-Mode Signal Timing Waveform for One OCT Block




**Note to Figure 7–18:**

(1) ts2p ≥ 25 ns

After calibrated codes are shifted serially to the corresponding I/O buffers, they must be converted from serial format to parallel format before being used in the I/O buffers. Figure 7–18 shows S2PENA signals that can be asserted at any time to update the calibration codes in each I/O bank. All I/O banks that received the codes from the same OCT calibration block can have S2PENA asserted at the same time, or at a different time, even while another OCT calibration block is calibrating and serially shifting codes. The S2PENA signal is asserted one OCTUSRCLK cycle after ENASER is deasserted for at least 25 ns. You cannot use I/Os for transmitting or receiving data when their S2PENA is asserted for parallel codes transfer.

## Example of Using Multiple OCT Calibration Blocks

Figure 7–19 shows a signal timing waveform for two OCT calibration blocks doing $R_S$ and $R_T$ calibration. Calibration blocks can start calibrating at different times by asserting ENASER signals at different times. ENAOCT must stay asserted while any calibration is ongoing. nCLRUSR must be set to low for one OCTUSRCLK cycle before each ENASER[N] signal is asserted. In Figure 7–19, when nCLRUSR is set to 0 for the second time to initialize OCT calibration block 0, this does not affect OCT calibration block 1, whose calibration is already in progress.

**Table 8–2.** Number of DQS/DQ Groups in Stratix III Devices per Side (Part 2 of 2)

| Device | Package | Side | ×4 *(1)* | ×8/×9 | ×16/×18 | ×32/×36 *(2)* |
|---|---|---|---|---|---|---|
| EP3SL340 | 1152-pin Hybrid FineLine BGA | Left/ Right | 26 | 12 | 4 | 0 |
| | | Top/ Bottom | 26 | 12 | 4 | 0 |
| | 1517-pin FineLine BGA | Left/ Right | 34 | 16 | 6 | 0 |
| | | Top/ Bottom | 38 | 18 | 8 | 4 |
| | 1760-pin FineLine BGA | Left/ Right | 40 | 18 | 6 | 0 |
| | | Top/ Bottom | 44 | 22 | 10 | 4 |

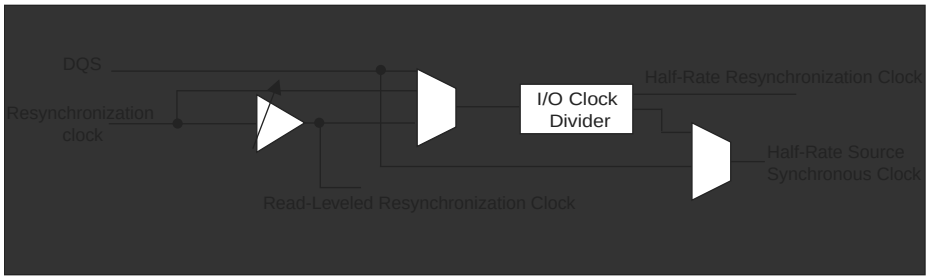
**Notes to Table 8–2:**

(1) Some of the ×4 groups may use configuration or RUP/RDN pins. You cannot use these ×4 groups if the pins are used for configuration or as RUP and RDN pins for OCT calibration.

(2) To interface with a ×36 QDR II+/QDR II SRAM device in a Stratix III FPGA that does not support the ×32/×36 DQS/DQ group, refer to the *Device, Pin, and Board Layout Guidelines* in volume 2 of the *External Memory Interface Handbook*.

Figure 8–18 illustrates the Stratix III read leveling circuitry.

**Figure 8–18.** Stratix III Read Leveling Delay Chains and Multiplexers *(Note 1)*




**Note to Figure 8–18:**

(1) There is only one leveling delay chain per I/O bank with the same I/O number (for example, I/O banks 1A, 1B, and 1C). You can only have one memory controller in these I/O banks when you use leveling delay chains.

The –90° write clock of the ALTMEMPHY megafunction feeds the write-leveling circuitry to produce the clock that generates the DQS and DQ signals. During initialization, the ALTMEMPHY megafunction picks the correct write-leveled clock for the DQS and DQ clocks for each DQS/DQ group after sweeping all the available clocks in the write calibration process. The DQ clock output is –90° phase-shifted compared to the DQS clock output.

Similarly, the resynchronization clock feeds the read-leveling circuitry to produce the optimal resynchronization and postamble clock for each DQS/DQ group in the calibration process. Resynchronization and the postamble clocks can use different clock outputs from the leveling circuitry. Output from the read-leveling circuitry can also generate the half-rate resynchronization clock that goes to the FPGA fabric.

☞ The ALTMEMPHY megafunction calibrates the alignment for read and write leveling dynamically during the initialization process.

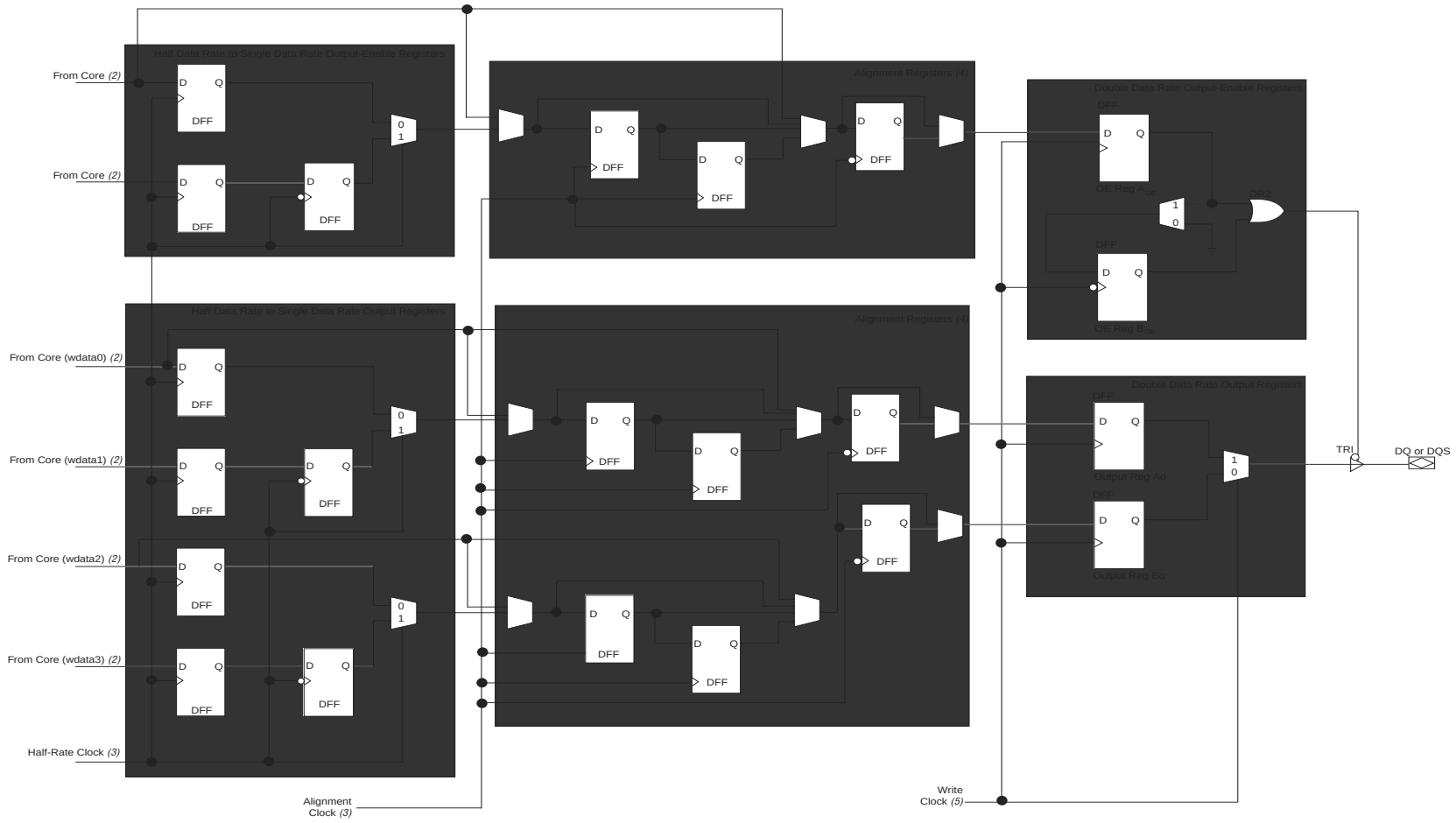
For more information about the ALTMEMPHY megafunction, refer to the *Volume 3: Implementing Altera Memory Interface IP*.

## Dynamic OCT Control

Figure 8–19 shows the dynamic OCT control block. The block includes all the registers required to dynamically turn on OCT $R_T$ during a read and turn OCT $R_T$ off during a write.

For more information about dynamic OCT control, refer to the *Stratix III Device I/O Features* chapter.

**Figure 8–21.** Stratix III IOE Output and Output-Enable Path Registers *(Note 1)*




**Notes to Figure 8–21:**

(1) You can bypass each register block of the output and output-enable paths.
(2) Data coming from the FPGA core are at half the frequency of the memory interface.
(3) Half-rate and alignment clocks come from the PLL.
(4) These registers are only used in DDR3 SDRAM interfaces for write-leveling purposes.
(5) The write clock can come from either the PLL or from the write-leveling delay chain. The DQ write clock and DQS write clock have a 90° offset between them.

# 9. High-Speed Differential I/O Interfaces and DPA in Stratix III Devices

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Stratix® III devices offers up to 1.6-Gbps differential I/O capabilities to support source-synchronous communication protocols such as Utopia, Rapid I/O®, XSBI, SGMII, SFI, and SPI.

Stratix III devices have the following dedicated circuitry for high-speed differential I/O support:

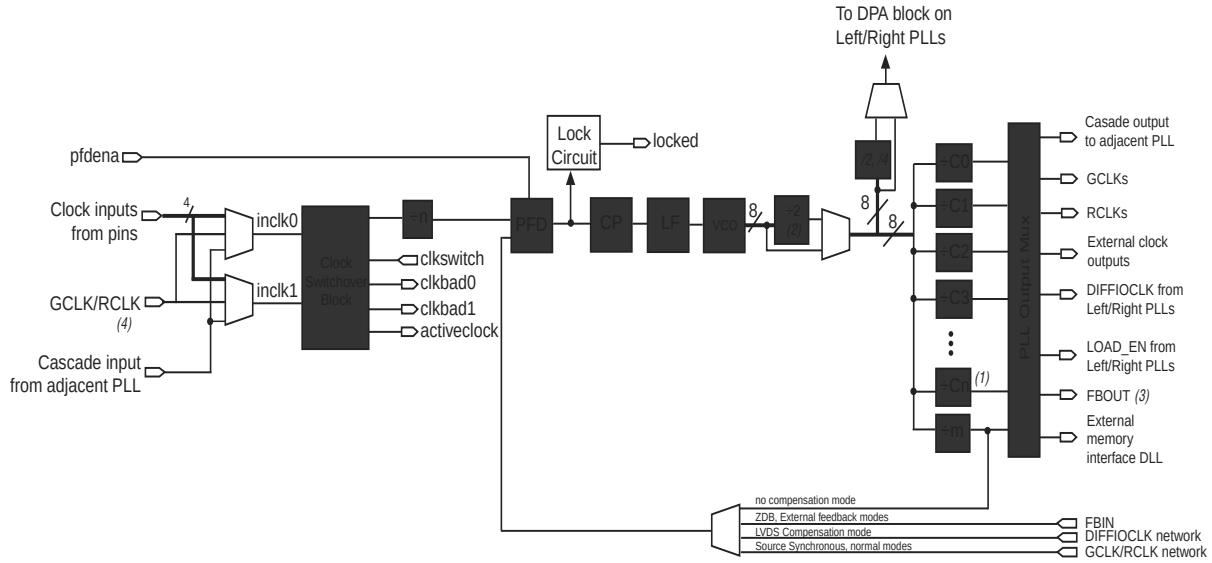
- Differential I/O buffer
- Transmitter serializer
- Receiver deserializer
- Data realignment
- Dynamic phase aligner (DPA)
- Synchronizer (FIFO buffer)
- Analog Phase-Locked Loops (PLLs) (located on left and right sides of the device)

For high-speed differential interfaces, Stratix III devices support the following differential I/O standards:

- Low voltage differential signaling (LVDS)
- Mini-LVDS
- Reduced swing differential signaling (RSDS)
- High-speed Transceiver Logic (HSTL)
- Stub Series Terminated Logic (SSTL)

Figure 9–12 shows a simplified block diagram of the major components of the Stratix III PLL.

**Figure 9–12.** PLL Block Diagram for Stratix III Devices




**Notes to Figure 9–12:**

(1) n = 6 for Left/Right PLLs; n = 9 for Top/Bottom PLLs.

(2) This is the VCO post-scale counter K.

(3) The FBOUT port is fed by the M counter in Stratix III PLLs.

(4) The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal or general purpose I/O pin cannot drive the PLL.

## Source-Synchronous Timing Budget

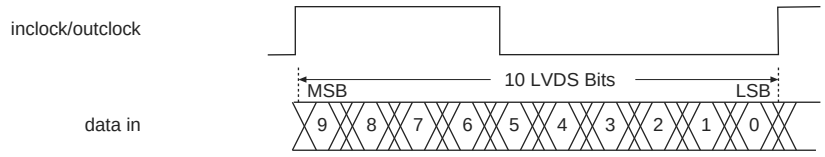
This section discusses the timing budget, waveforms, and specifications for source-synchronous signaling in Stratix III devices. LVDS I/O standards enable high-speed data transmission. This high data transmission rate results in better overall system performance. To take advantage of fast system performance, it is important to understand how to analyze timing for these high-speed signals. Timing analysis for the differential block is different from traditional synchronous timing analysis techniques.

Rather than focusing on clock-to-output and setup times, source synchronous timing analysis is based on the skew between the data and the clock signals. High-speed differential data transmission requires the use of timing parameters provided by IC vendors and is strongly influenced by board skew, cable skew, and clock jitter. This section defines the source-synchronous differential data orientation timing parameters, the timing budget definitions for Stratix III devices, and ways to use these timing parameters to determine the maximum performance of your design.

## Differential Data Orientation

There is a set relationship between an external clock and the incoming data. For an operation at 1 Gbps and SERDES factor of 10, the external clock is multiplied by 10, and phase-alignment can be set in the PLL to coincide with the sampling window of each data bit. The data is sampled on the falling edge of the multiplied clock. Figure 9–15 shows the data bit orientation of the ×10 mode.

**Figure 9–15.** Bit Orientation in Quartus II Software




## Differential I/O Bit Position

Data synchronization is necessary for successful data transmission at high frequencies. Figure 9–16 shows the data bit orientation for a channel operation. These figures are based on the following:

- SERDES factor equals clock multiplication factor
- Edge alignment is selected for phase alignment
- Implemented in hard SERDES

For other serialization factors, use the Quartus II software tools and find the bit position within the word and the bit positions after deserialization.

Enabling compression reduces the amount of configuration data that is transmitted to the Stratix III device, which also reduces configuration time. On average, compression reduces configuration time, depending on the design.

Figure 11–11 shows the timing waveform for AS configuration.

**Figure 11–11.** Fast AS Configuration Timing

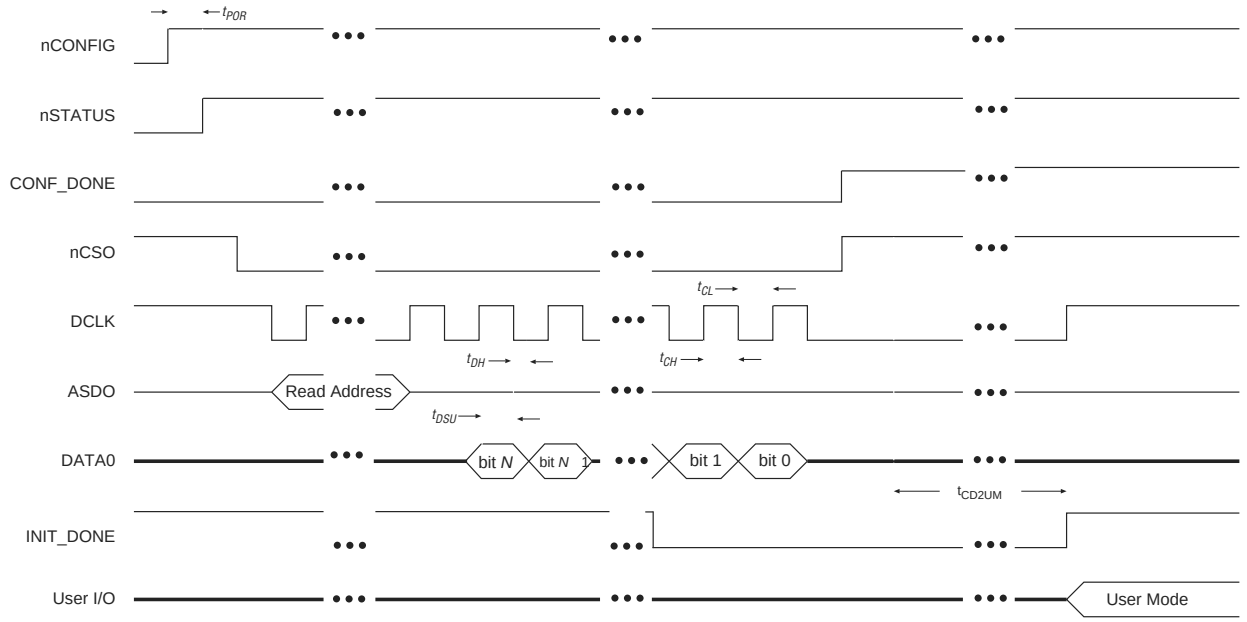



Table 11–8 defines the timing parameters for Stratix III devices for fast AS configuration.

**Table 11–8.** Fast AS Timing Parameters for Stratix III Devices

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $f_{CLK}$ | DCLK frequency from Stratix III | 15 | 25 | 40 | MHz |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | — | 100 | µs |
| $t_{DSU}$ | Data setup time before falling edge on DCLK | 7 | — | — | ns |
| $t_{DH}$ | Data hold time after falling edge on DCLK | 0 | — | — | ns |
| $t_{CH}$ | DCLK high time | 10 | — | — | ns |
| $t_{CL}$ | DCLK low time | 10 | — | — | ns |
| $t_{CD2UM}$ | CONF_DONE high to user mode | 20 | — | 100 | µs |

# 14. Design Security in Stratix III Devices

SIII51014-1.5

## Introduction

This chapter provides an overview of the design security feature and its implementation on Stratix® III devices using advanced encryption standard (AES) as well as security modes available in Stratix III devices.

As Stratix III devices start to play a role in larger and more critical designs in competitive commercial and military environments, it is increasingly important to protect the designs from copying, reverse engineering, and tampering. Stratix III devices address these concerns and are the industry's only high-density, high-performance devices with both volatile and non-volatile security feature support. Stratix III devices have the ability to decrypt configuration bitstreams using the AES algorithm, an industry standard encryption algorithm that is FIPS-197 certified. They also have a design security feature that utilizes a 256-bit security key.

Altera® Stratix III devices store configuration data in static random access memory (SRAM) configuration cells during device operation. Because SRAM memory is volatile, SRAM cells must be loaded with configuration data each time the device powers-up. It is possible to intercept configuration data when it is being transmitted from the memory source (flash memory or a configuration device) to the device. The intercepted configuration data could then be used to configure another device.

When using the Stratix III design security feature, the security key is stored in the Stratix III device. Depending on the security mode, you can configure the Stratix III device using a configuration file that is encrypted with the same key, or for board testing, configured with a normal configuration file.

The design security feature is available when configuring Stratix III devices using the fast passive parallel (FPP) configuration mode with an external host (such as a MAX® II device or microprocessor), or when using fast active serial (AS) or passive serial (PS) configuration schemes. However, the design security feature is also available in remote update with fast AS configuration mode. The design security feature is not available when you are configuring your Stratix III device using Joint Test Action Group (JTAG)-based configuration. For more information, refer to "Supported Configuration Schemes" on page 14–5.

## Stratix III Security Protection

Stratix III device designs are protected from copying, reverse engineering, and tampering using configuration bitstream encryption.

### Security Against Copying

The security key is securely stored in the Stratix III device and cannot be read out through any interfaces. In addition, as configuration file read-back is not supported in Stratix III devices, the design information cannot be copied.