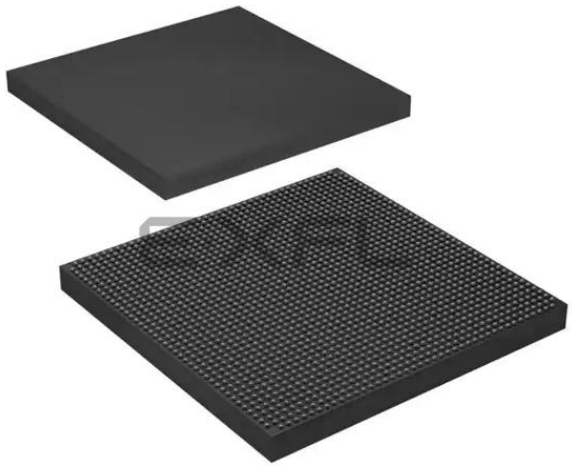

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	13500
Number of Logic Elements/Cells	337500
Total RAM Bits	18822144
Number of I/O	1120
Number of Gates	-
Voltage - Supply	0.86V ~ 1.15V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1760-BBGA, FCBGA
Supplier Device Package	1760-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep3sl340f1760c3n

Table 1–1 lists the Stratix III FPGA family features.

Table 1–1. FPGA Family Features for Stratix III Devices

	Device/ Feature	ALMs	LEs	M9K Blocks	M144K Blocks	MLAB Blocks	Total Embedded RAM Kbits	MLAB RAM Kbits *(1)*	Total RAM Kbits*(2)*	18×18-bit Multipliers (FIR Mode)	PLLs *(3)*
Stratix III Logic Family	EP3SL50	19K	47.5K	108	6	950	1,836	297	2,133	216	4
	EP3SL70	27K	67.5K	150	6	1,350	2,214	422	2,636	288	4
	EP3SL110	43K	107.5K	275	12	2,150	4,203	672	4,875	288	8
	EP3SL150	57K	142.5K	355	16	2,850	5,499	891	6,390	384	8
	EP3SL200	80K	200K	468	36	4,000	9,396	1,250	10,646	576	12
	EP3SL340	135K	337.5K	1,040	48	6,750	16,272	2,109	18,381	576	12
Stratix III Enhanced Family	EP3SE50	19K	47.5K	400	12	950	5,328	297	5,625	384	4
	EP3SE80	32K	80K	495	12	1,600	6,183	500	6,683	672	8
	EP3SE110	43K	107.5K	639	16	2,150	8,055	672	8,727	896	8
	EP3SE260	102K	255K	864	48	5,100	14,688	1,594	16,282	768	12

Notes to Table 1–1:

(1) MLAB ROM mode supports twice the number of MLAB RAM Kbits.

(2) For total ROM Kbits, use this equation to calculate:
Total ROM Kbits = Total Embedded RAM Kbits + [(# of MLAB blocks × 640)/1024]

(3) The availability of the PLLs shown in this column is based on the device with the largest package. Refer to the *Clock Networks and PLLs in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook* for the availability of the PLLs for each device.

The Stratix III logic family (*L*) offers balanced logic, memory, and multipliers to address a wide range of applications, while the enhanced family (*E*) offers more memory and multipliers per logic and is ideal for wireless, medical imaging, and military applications.

Stratix III devices are available in space-saving FineLine BGA (FBGA) packages (refer to Table 1–2 and Table 1–3).

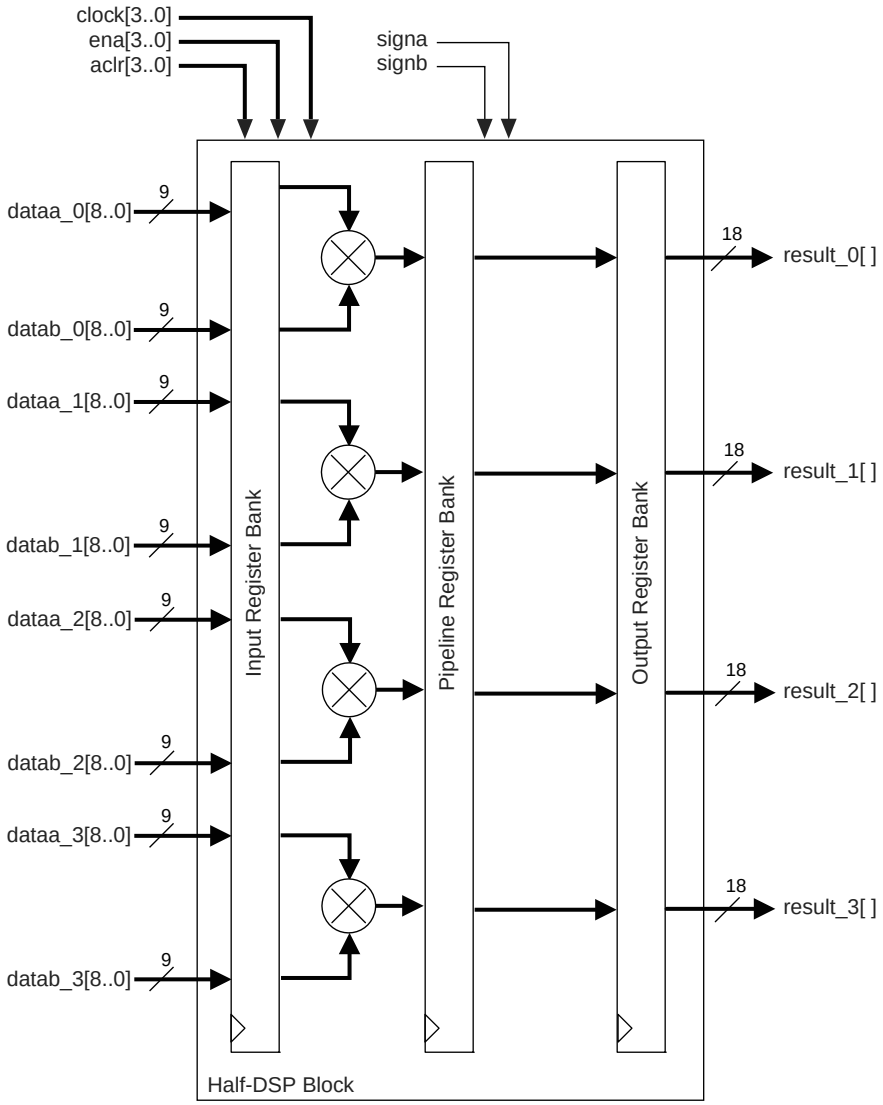
Chapter Revision History

Table 4–10 shows the revision history for this chapter.

Table 4–10. Chapter Revision History

Date and Revision	Changes Made	Summary of Changes
May 2009, version 1.8	■ Updated Table 4–1. ■ Updated "Read/Write Clock Mode" and "Simple Dual-Port Mode" sections.	—
February 2009, version 1.7	■ Updated Figure 4–2, Figure 4–4, and Figure 4–5. ■ Removed "Referenced Documents" section.	—
November 2008, Version 1.6	■ Updated "Byte-Enable Support", "Address Clock Enable Support", "Asynchronous Clear", "Single Port RAM", and "Simple Dual-Port Mode" sections. ■ Updated Figure 4–1, Figure 4–5, Figure 4–8, Figure 4–10, and Figure 4–15. ■ Added Figure 4–2, Figure 4–6, Figure 4–11, Figure 4–14, and Figure 4–16.	—
October 2008, version 1.5	■ Updated Table 4–1. ■ Updated "Asynchronous Clear" and "Clocking Modes" section. ■ Added "Programming File Compatibility" section. ■ Updated New Document Format.	—
May 2008, version 1.4	■ Updated "Introduction" section. ■ Updated "TriMatrix Memory Block Types" section. ■ Updated "Byte-Enable Support" section. ■ Updated "Mixed Width Support" section. ■ Updated "Same-Port Read-During-Write Mode" section. ■ Updated Figure 4–16, Figure 4–17, and Figure 4–18. ■ Updated "Mixed-Port Read-During-Write Mode" section. ■ Updated Table 4–1, Table 4–2, and Table 4–4.	—
November 2007, version 1.3	Updated Table 4–2.	—
October 2007, version 1.2	■ Updated Table 4–1. ■ Added section "Referenced Documents". ■ Added live links for references.	—
May 2007, version 1.1	Updated Table 4–2, Table 4–9.	—
November 2006, version 1.0	Initial Release.	—

Figure 5–10. 9-Bit Independent Multiplier Mode for Half-Block



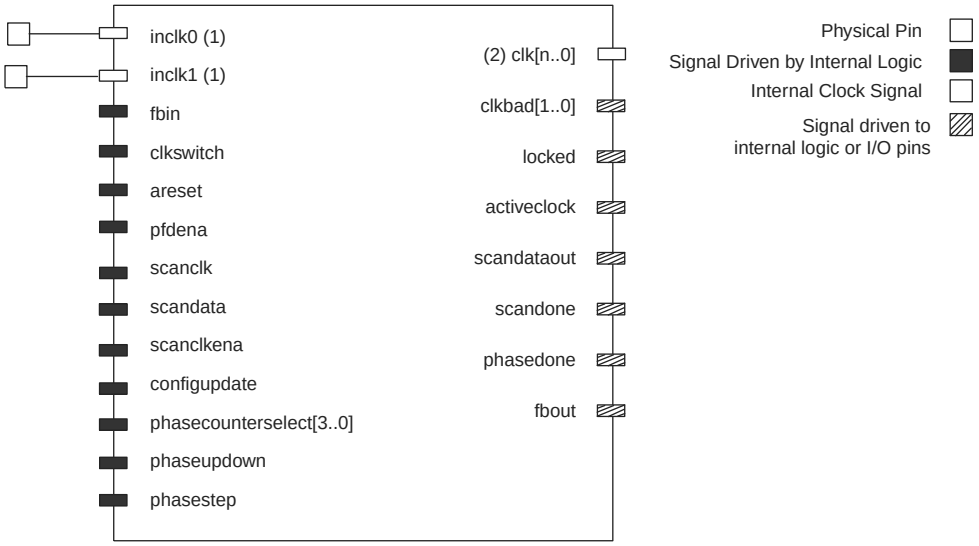
The multiplier operands can accept signed integers, unsigned integers, or a combination of both. You can change the `signa` and `signb` signals dynamically and can be registered in the DSP block. Additionally, the multiplier inputs and result can be registered independently. You can use the pipeline registers within the DSP block to pipeline the multiplier result, increasing the performance of the DSP block.

☞ The round and saturation logic unit is supported for the 18-bit independent multiplier mode only.

Stratix III PLL Software Overview

Stratix III PLLs are enabled in the Quartus II software by using the ALTPLL megafunction. Figure 6–22 shows the Stratix III PLL ports as they are named in the ALTPLL megafunction of the Quartus II software.

Figure 6–22. Stratix III PLL Ports



Notes to Figure 6–22:

(1) You can feed the `inclk0` or `inclk1` clock input from any one of four dedicated clock pins located on the same side of the device as the PLL.
(2) You can drive to global or regional clock networks or dedicated external clock output pins. n = 6 for Left/Right PLLs and n = 9 for Top/Bottom PLLs.

Table 6–12 lists the PLL input signals for Stratix III devices.

Table 6–12. PLL Input Signals (Part 1 of 2)

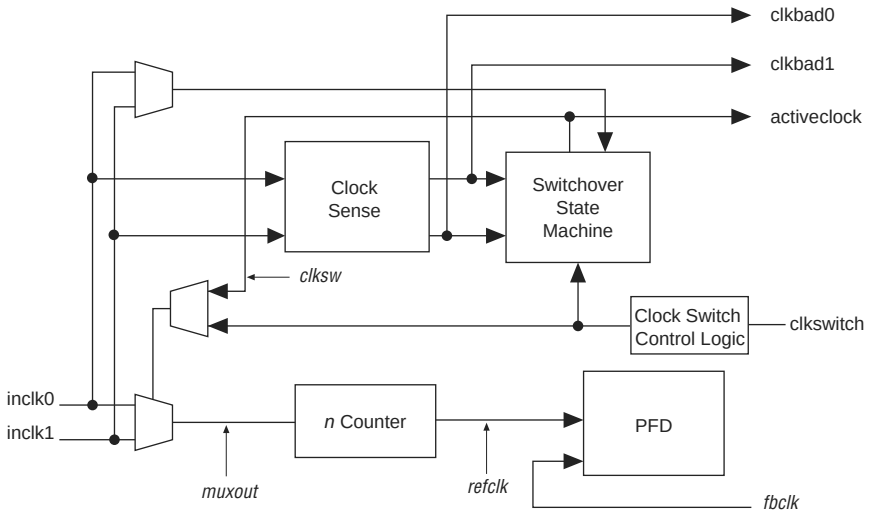
Port	Description	Source	Destination
`inclk0`	Input clock to the PLL	Dedicated pin, adjacent PLL, GCLK, or RCLK network	N counter
`inclk1`	Input clock to the PLL	Dedicated pin, adjacent PLL, GCLK, or RCLK network	N counter
`fbin`	Compensation feedback input to the PLL. Share the same clock spines used by GCLK/RCLKs.	Pin LVSDCLK	PFD
`clkswitch`	Switchover signal used to initiate clock switchover asynchronously. When used in manual switchover, `clkswitch` is used as a select signal between `inclk0` and `inclk1`. If `clkswitch` = `0`, `inclk0` is selected. If `clkswitch` = `1`, `inclk1` is selected. Both `inclk0` and `inclk1` must be switched in order for manual switchover to function.	Logic array or I/O pin	Clock switchover circuit

The following clock switchover modes are supported in Stratix III PLLs:

- Automatic switchover—The clock sense circuit monitors the current reference clock and if it stops toggling, automatically switches to the other clock `inclk0` or `inclk1`.
- Manual clock switchover—Clock switchover is controlled via the `clkswitch` signal in this mode. When the `clkswitch` signal goes from logic low to logic high, and stays high for at least three clock cycles, the reference clock to the PLL is switched from `inclk0` to `inclk1`, or vice-versa.
- Automatic switchover with manual override—This mode combines Modes 1 and 2. When the `clkswitch` signal goes high, it overrides automatic clock switchover mode.

Stratix III device PLLs support a fully configurable clock switchover capability. Figure 6–32 shows the block diagram of the switchover circuit built into the PLL. When the current reference clock is not present, the clock sense block automatically switches to the backup clock for PLL reference. The clock switchover circuit also sends out three status signals—`clkbad[0]`, `clkbad[1]`, and `activeclock`—from the PLL to implement a custom switchover circuit in the logic array. You can select a clock source as the backup clock by connecting it to the `inclk1` port of the PLL in your design.

Figure 6–32. Automatic Clock Switchover Circuit Block Diagram



Automatic Clock Switchover

Use the switchover circuitry to automatically switch between `inclk0` and `inclk1` when the current reference clock to the PLL stops toggling. For example, in applications that require a redundant clock with the same frequency as the reference clock, the switchover state machine generates a signal (`clksw`) that controls the multiplexer select input as shown in Figure 6–32. In this case, `inclk1` becomes the reference clock for the PLL. When using the automatic switchover mode, you can switch back and forth between `inclk0` and `inclk1` clocks any number of times, when one of the two clocks fails and the other clock is available.

Programmable Bandwidth

Stratix III PLLs provide advanced control of the PLL bandwidth using the PLL loop's programmable characteristics, including loop filter and charge pump.

Background

PLL bandwidth is the measure of the PLL's ability to track the input clock and its associated jitter. The closed-loop gain 3-dB frequency in the PLL determines the PLL bandwidth. The bandwidth is approximately the unity gain point for open loop PLL response. As Figure 6–37 shows, these points correspond to approximately the same frequency. Stratix III PLLs provide three bandwidth settings—low, medium (default), and high.

Figure 6–37. Open- and Closed-Loop Response Bode Plots

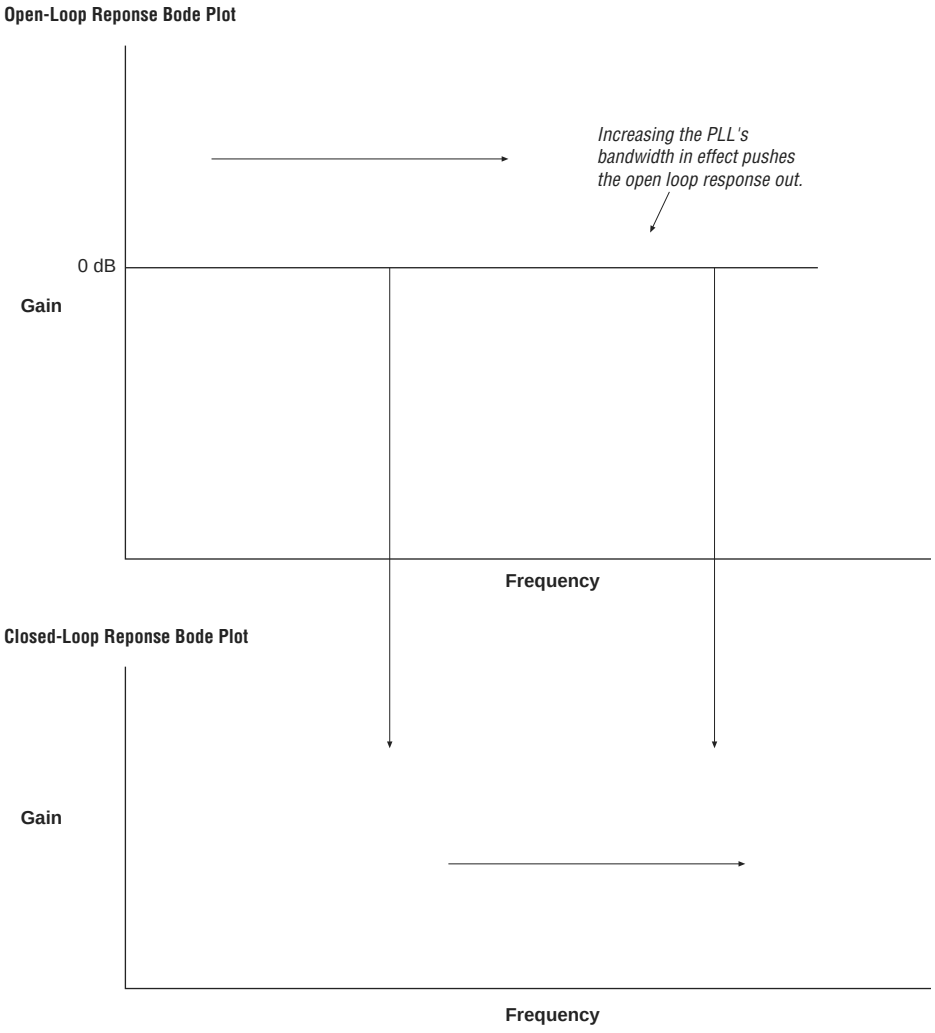
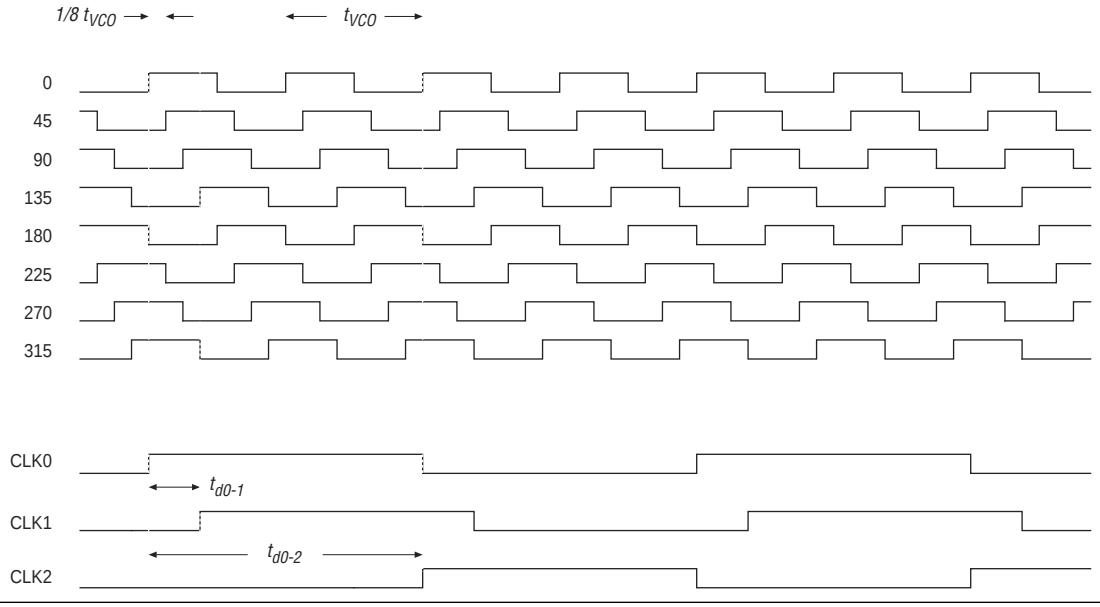


Figure 6–39. Delay Insertion Using VCO Phase Output and Counter Delay Time



You can use the coarse- and fine-phase shifts to implement clock delays in Stratix III devices.

Stratix III devices support dynamic phase-shifting of VCO phase taps only. The phase shift is reconfigurable any number of times, and each phase shift takes about one SCANCLK cycle, allowing you to implement large phase shifts quickly.

PLL Reconfiguration

PLLs use several divide counters and different VCO phase taps to perform frequency synthesis and phase shifts. In Stratix III PLLs, you can reconfigure both the counter settings and phase-shift the PLL output clock in real time. You can also change the charge pump and loop-filter components, which dynamically affects the PLL bandwidth. You can use these PLL components to update the output-clock frequency and the PLL bandwidth and to phase-shift in real time, without reconfiguring the entire Stratix III device.

The ability to reconfigure the PLL in real time is useful in applications that operate at multiple frequencies. It is also useful in prototyping environments, allowing you to sweep PLL output frequencies and adjust the output-clock phase dynamically. For example, a system generating test patterns is required to generate and transmit patterns at 75 or 150 MHz, depending on the requirements of the device under test. Reconfiguring the PLL components in real time allows you to switch between two such output frequencies within a few microseconds. You can also use this feature to adjust clock-to-out (t_{co}) delays in real time by changing the PLL output clock phase shift. This approach eliminates the need to regenerate a configuration file with the new PLL settings.

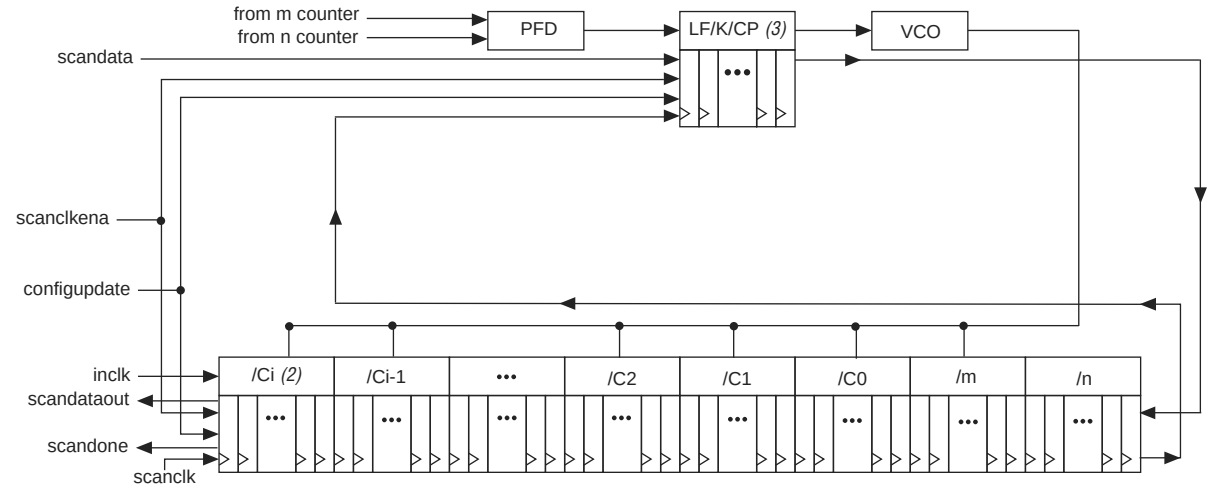
PLL Reconfiguration Hardware Implementation

The following PLL components are reconfigurable in real time:

- Pre-scale counter (n)
- Feedback counter (m)
- Post-scale output counters (C0 – C9)
- Post VCO Divider (K)
- Dynamically adjust the charge-pump current (I_{cp}) and loop-filter components (R, C) to facilitate reconfiguration of the PLL bandwidth

Figure 6–40 shows how PLL counter settings can be dynamically adjusted by shifting their new settings into a serial shift-register chain or scan chain. Serial data is input to the scan chain via the scandataport and shift registers are clocked by scanclk. The maximum scanclk frequency is 100 MHz. Serial data is shifted through the scan chain as long as the scanclkena signal stays asserted. After the last bit of data is clocked, asserting the configupdate signal for at least one scanclk clock cycle causes the PLL configuration bits to be synchronously updated with the data in the scan registers.

Figure 6–40. PLL Reconfiguration Scan Chain



Notes to Figure 6–40:

(1) The Stratix III Left/Right PLLs support C0 - C6 counters.

(2) i = 6 or i = 9.

(3) This figure shows the corresponding scan register for the K counter in between the scan registers for the charge pump and loop filter. The K counter is physically located after the VCO.

The counter settings are updated synchronously to the clock frequency of the individual counters. Therefore, all counters are not updated simultaneously.

Table 7–9. Selectable I/O Standards with Expanded On-Chip Series Termination with Calibration Range

I/O Standard	Expanded OCT R_S range		
	Row I/O	Column I/O	Unit
3.3-V LVTTL/LVCMOS	20–60	20–60	Ω
3.0-V LVTTL/LVCMOS	20–60	20–60	Ω
2.5-V LVTTL/LVCMOS	20–60	20–60	Ω
1.8-V LVTTL/LVCMOS	20–60	20–60	Ω
1.5-V LVTTL/LVCMOS	40–60	20–60	Ω
1.2-V LVTTL/LVCMOS	40–60	20–60	Ω
SSTL-2	20–60	20–60	Ω
SSTL-18	20–60	20–60	Ω
SSTL-15	40–60	20–60	Ω
HSTL-18	20–60	20–60	Ω
HSTL-15	40–60	20–60	Ω
HSTL-12	40–60	20–60	Ω

Note to Table 7–9:

(1) The expanded On-Chip Series Termination with calibration of SSTL and HSTL is for impedance matching to improve signal integrity and not for meeting JEDEC standard.

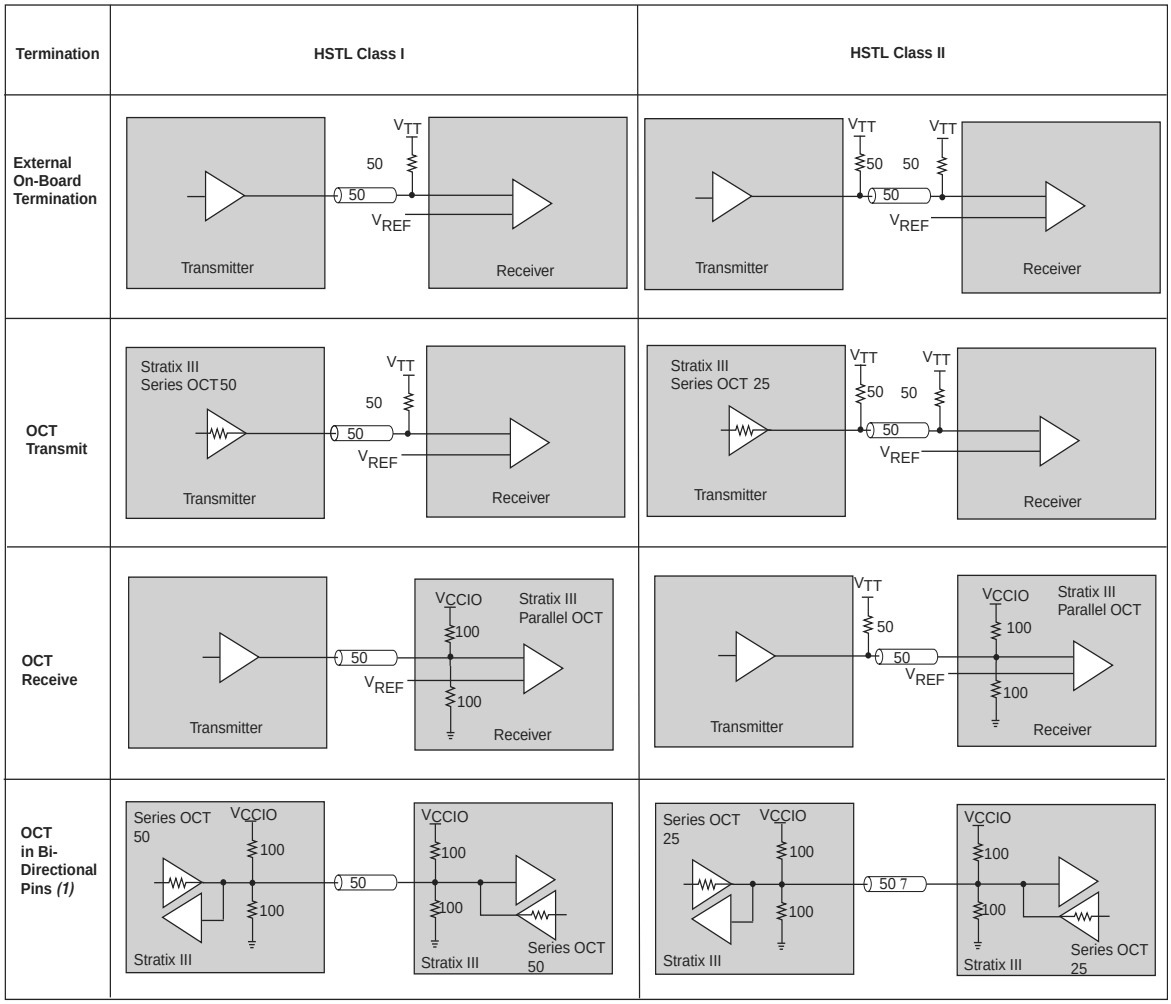
Left Shift Series Termination Control

Stratix III devices support left shift series termination control. You can use the left shift series termination control to get the calibrated OCT R_S with half of the impedance value of the external reference resistors connected to RUP and RDN pins. This feature is useful in applications which require both 25-Ω and 50-Ω calibrated OCT R_S at the same V_{CCIO}. For example, if your applications require 25-Ω and 50-Ω calibrated OCT R_S for SSTL–2 Class I and Class II I/O standards, you would only require one OCT calibration block with 50-Ω external reference resistors. You can enable this feature in the ALTIOBUF megafunction in the Quartus II software. The Quartus II software only allows the left shift series termination control for 25-Ω calibrated OCT R_S with 50-Ω external reference resistors connected to RUP and RDN pins. You can only use left shift series termination control for I/O standards that support 25 Ω calibrated OCT R_S.

Left shift series termination control is automatically enabled if you use a bidirectional I/O with 25- Ω calibrated OCT R_S and 50- Ω parallel OCT.

For more information about how to enable left shift series termination in the ALTIOBUF megafunction, refer to the *ALTIOBUF Megafunction User Guide*.

Figure 7–21. HSTL I/O Standard Termination for Stratix III Devices



Note to Figure 7–21:

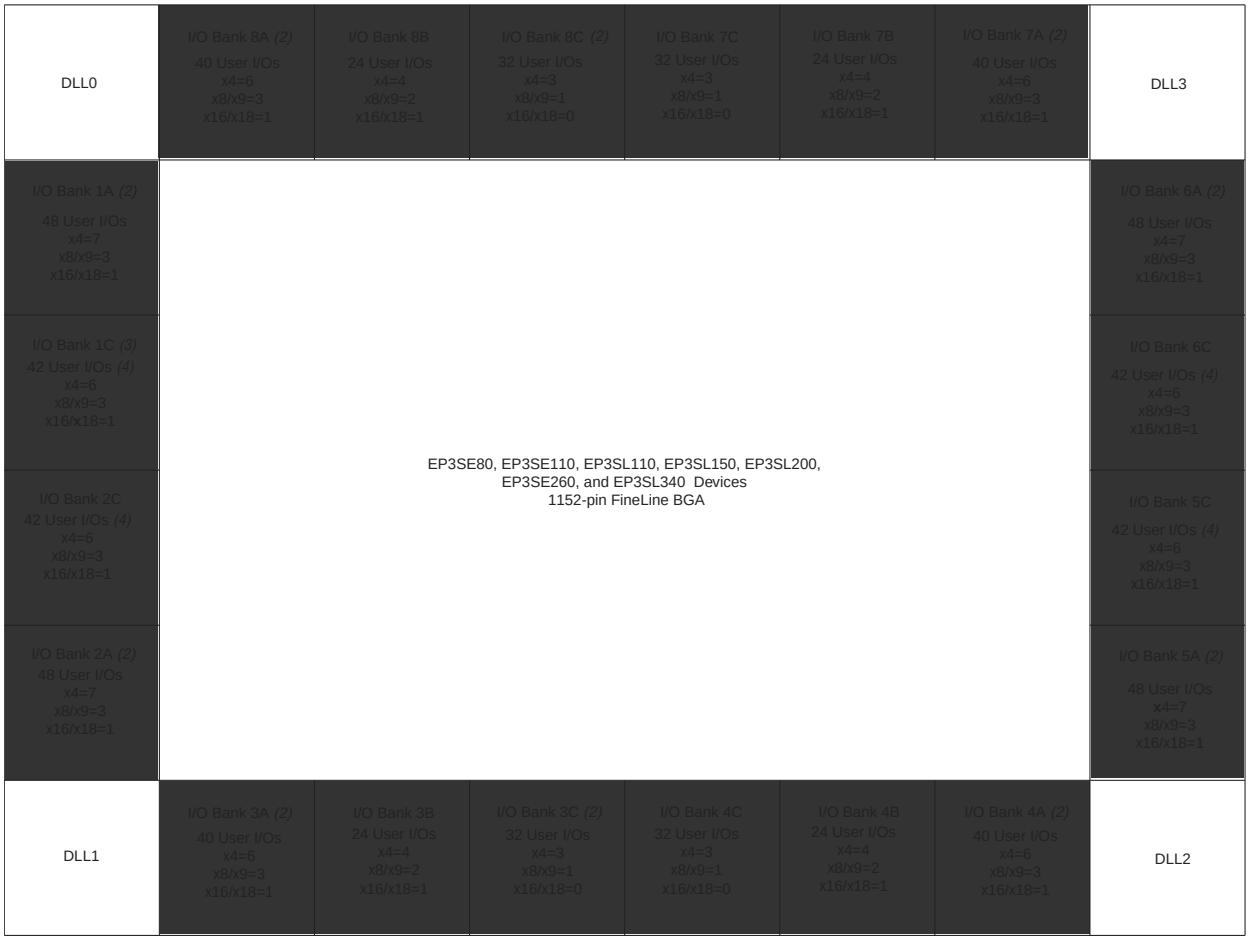
(1) In Stratix III devices, you cannot use simultaneously series and parallel OCT. For more information, refer to "Dynamic OCT" on page 7–25.

Differential I/O Standards Termination

Stratix III devices support differential SSTL-2 and SSTL-18, differential HSTL-18, HSTL-15, HSTL-12, LVDS, LVPECL, RSDS, and mini-LVDS. Figure 7–22 through Figure 7–28 show the details of various differential I/O termination on Stratix III devices.

☞ Differential HSTL and SSTL outputs are not true differential outputs. They use two single-ended outputs with the second output programmed as inverted.

Figure 8–5. Number of DQS/DQ Groups in EP3SE80, EP3SE110, EP3SL110, EP3SL150, EP3SL200, EP3SE260, and EP3SL340 Devices in the 1152-pin FineLine BGA Package *(Note 1)*



Notes to Figure 8–5:

(1) This device does not support ×32/×36 mode.

(2) You can also use DQS/DQSn pins in some of the ×4 groups as RUP/RDN pins. You cannot use a ×4 group for memory interfaces if two pins of the group are being used as RUP and RDN pins for OCT calibration. You can still use the ×16/×18 or ×32/×36 groups that includes these ×4 groups. However, there are restrictions on using ×8/×9 groups that include these ×4 groups as described on page 8–5.

(3) Some of the DQS/DQ pins in this bank can also be used as configuration pins. Choose the DQS/DQ pins that are not going to be used by your configuration scheme.

(4) All I/O pin counts include eight dedicated clock inputs (CLK1p, CLK1n, CLK3p, CLK3n, CLK8p, CLK8n, CLK10p, and CLK10n).

Chapter Revision History

Table 9–4 lists the revision history for this chapter.

Table 9–4. Chapter Revision History

Date	Revision	Changes Made
July 2010	1.9	Updated "Differential Transmitter" and "Differential Receiver" sections.
March 2010	1.8	Updated for the Quartus II software version 9.1 SP2 release: ■ Updated "LVDS Channels", "Differential Transmitter", and "Differential Receiver" section. ■ Minor changes to the text.
May 2009	1.7	■ Updated Table 9–1 and Table 9–2. ■ Updated Figure 9–5. ■ Updated "DPA-Enabled Channels and Single-Ended I/Os" section.
February 2009	1.6	■ Updated "DPA-Enabled Channels and Single-Ended I/Os" section. ■ Updated Table 9–2. ■ Removed "Reference Documents" section.
October 2008	1.5	■ Updated "Introduction", "Differential Receiver", and "Synchronizer" sections. ■ Updated Figure 9–5. ■ Updated New Document Format.
May 2008	1.4	■ Updated "Soft-CDR Mode", "Dynamic Phase Aligner (DPA)", "Programmable Pre-Emphasis and Programmable VOD", and "Guidelines for DPA-Enabled Differential Channels" sections. ■ Updated Table 9–1 and Table 9–2. ■ Removed "Figure 9–19. Left/Right PLL Driving Distance for DPA-Enabled Channels".
November 2007	1.3	■ Updated Table 9–1 and Table 9–2.
October 2007	1.2	■ Added material to "DPA-Enabled Channels and Single-Ended I/Os" on page 9–21 and removed material from "DPA-Disabled Channels and Single-Ended I/Os" on page 9–29. ■ Added new sections "Programmable Pre-Emphasis and Programmable VOD" on page 9–12, "Soft-CDR Mode", and "Referenced Documents". ■ Added live links for references. ■ Added Figure 9–10. ■ Minor edits to "DPA-Enabled Channel Driving Distance" section.
May 2007	1.1	■ Minor changes to second paragraph of the section "Differential I/O Termination". ■ Added Table 9–1 and Table 9–2.
November 2006	1.0	Initial release.

Remote System Upgrade

Stratix III devices contain the remote update feature. For more information about this feature, refer to the *Remote System Upgrades with Stratix III Devices* in volume 1 of the *Stratix III Device Handbook*.

Power-On Reset Circuit

The POR circuit keeps the entire system in reset until the power supply voltage levels have stabilized on power-up. On power-up, the device does not release nSTATUS until V_{CCPT}, V_{CCL}, V_{CC}, V_{CCPD}, and V_{CCPGM} are above the device's POR trip point. On power down, brown-out occurs if V_{CC} or V_{CCL} ramps down below the POR trip point and V_{CC}, V_{CCPD}, or V_{CCPGM} drops below the threshold voltage.

In Stratix III devices, a pin-selectable option (PORSEL) is provided that allows you to select a typical POR time setting of 12 ms or 100 ms. In both cases, you can extend the POR time by using an external component to assert the nSTATUS pin low.

V_{CCPGM} Pins

Stratix III devices offer a new power supply, V_{CCPGM}, for all the dedicated configuration pins and dual function pins. The configuration voltages supported are 1.8 V, 2.5 V, 3.0 V, and 3.3 V. Stratix III devices do not support the 1.5 V configuration.

Use this pin to power all dedicated configuration inputs, dedicated configuration outputs, dedicated configuration bi-directional pins, and some of the dual functional pins that you use for configuration. With V_{CCPGM}, configuration input buffers do not have to share power lines with the regular I/O buffer in Stratix III devices.

The operating voltage for the configuration input pin is independent of the I/O bank's power supply V_{CCIO} during the configuration. Therefore, no configuration voltage constraints on V_{CCIO} are needed in Stratix III devices.

V_{CCPD} Pins

Stratix III devices have a dedicated programming power supply, V_{CCPD}, which must be connected to 3.3 V/3.0 V/2.5 V to power the I/O pre-drivers, the JTAG input and output pins (TCK, TMS, TDI, TDO, and TRST), and the design security circuitry.

V_{CCPGM} and V_{CCPD} must ramp up from 0 V to the desired voltage level within 100 ms. If these supplies are not ramped up within this specified time, your Stratix III device will not configure successfully. If your system does not allow ramp-up time of 100 ms or less, you must hold nCONFIG low until all power supplies are stable.

For more information about the configuration pins power supply, refer to "Device Configuration Pins" on page 11–43.

An optional INIT_DONE pin is available, which signals the end of initialization and the start of user-mode with a low-to-high transition. The **Enable INIT_DONE Output** option is available in the Quartus II software on the **General** tab of the **Device and Pin Options** dialog box. If you use the INIT_DONE pin, it will be high due to an external 10-kΩ pull-up resistor when nCONFIG is low and during the beginning of configuration. When the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin will go low. When initialization is complete, the INIT_DONE pin will be released and pulled high. The MAX II device must be able to detect this low-to-high transition, which signals the device has entered user mode. When initialization is complete, the device enters user mode. In user mode, the user I/O pins will no longer have weak pull-up resistors and will function as assigned in your design.

To ensure DCLK and DATA0 are not left floating at the end of configuration, the MAX II device must drive them either high or low, whichever is convenient on your board. The DATA[0] pin is available as a user I/O pin after configuration. When you choose the PS scheme as a default in the Quartus II software, this I/O pin is tri-stated in user mode and should be driven by the MAX II device. To change this default option in the Quartus II software, click the **Dual-Purpose Pins** tab of the **Device and Pin Options** dialog box.

The configuration clock (DCLK) speed must be below the specified frequency to ensure correct configuration. No maximum DCLK period exists, which means you can pause configuration by halting DCLK for an indefinite amount of time.

If an error occurs during configuration, the device drives its nSTATUS pin low, resetting itself internally. The low signal on the nSTATUS pin also alerts the MAX II device that there is an error. If the **Auto-restart configuration after error** option (available in the Quartus II software on the **General** tab of the **Device and Pin Options** dialog box) is turned on, the Stratix III device releases nSTATUS after a reset time-out period (maximum of 100 µs). After nSTATUS is released and pulled high by a pull-up resistor, the MAX II device can attempt to reconfigure the target device without needing to pulse nCONFIG low. If this option is turned off, the MAX II device must generate a low-to-high transition (with a low pulse of at least 2 µs) on nCONFIG to restart the configuration process.

☞ If you have enabled the **Auto-restart configuration after error** option, the nSTATUS pin transitions from high to low and back again to high when a configuration error is detected. This appears as a low pulse at the nSTATUS pin with a minimum pulse width of 10 µs to a maximum pulse width of 500 µs, as defined in the t_{STATUS} specification.

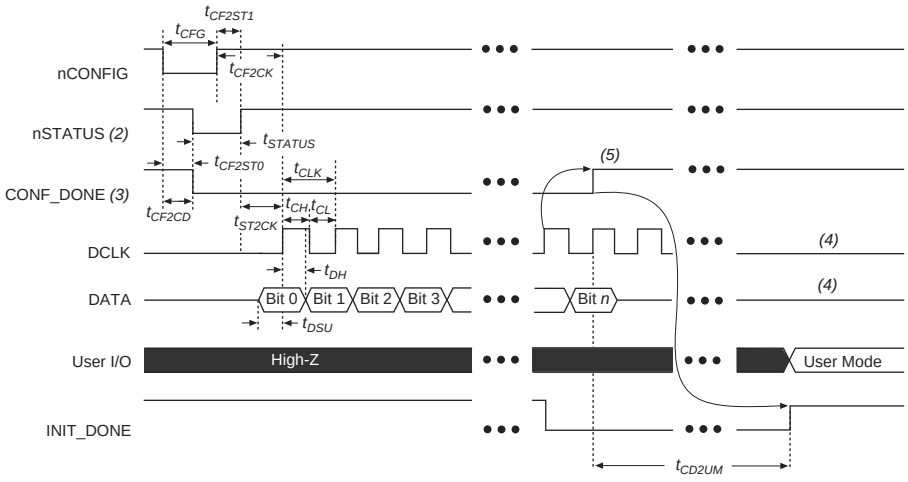
The MAX II device can also monitor the CONF_DONE and INIT_DONE pins to ensure successful configuration. The CONF_DONE pin must be monitored by the MAX II device to detect errors and determine when programming completes. If all configuration data is sent, but CONF_DONE or INIT_DONE have not gone high, the MAX II device must reconfigure the target device.

☞ If you use the optional CLKUSR pin and nCONFIG is pulled low to restart configuration during device initialization, you must ensure that CLKUSR continues toggling during the time nSTATUS is low (maximum of 100 µs).

PS Configuration Timing

Figure 11–16 shows the timing waveform for PS configuration when using a MAX II device as an external host.

Figure 11–16. PS Configuration Timing Waveform *(Note 1)*



Notes to Figure 11–16:

(1) The beginning of this waveform shows the device in user-mode. In user-mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(2) Upon power-up, the Stratix III device holds nSTATUS low for the time of the POR delay.

(3) Upon power-up, before and during configuration, CONF_DONE is low.

(4) Do not leave DCLK floating after configuration. You should drive it high or low, whichever is more convenient. DATA[0] is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.

(5) Two DCLK falling edges are required after CONF_DONE goes high to begin the initialization of the device.

Table 11–10 defines the timing parameters for Stratix III devices for PS configuration.

Table 11–10. PS Timing Parameters for Stratix III Devices (Part 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	800	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	800	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	10	100 *(1)*	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	100 *(1)*	µs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	100	—	µs
t_{ST2CK}	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	Data setup time before rising edge on DCLK	5	—	ns
t_{DH}	Data hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	4	—	ns
t_{CL}	DCLK low time	4	—	ns
t_{CLK}	DCLK period	10	—	ns
f_{MAX}	DCLK frequency	—	100	MHz
t_{R}	Input rise time	—	40	ns

Table 11–14. Dedicated Configuration Pins on the Stratix III Device (Part 5 of 5)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
DCLK *(1)*	N/A	Synchronous configuration schemes (PS, FPP, AS)	Input (PS, FPP) Output (AS)	DCLK has an internal pull-up resistor (typically 25 kΩ) that is always active. In AS mode, DCLK is an output from the Stratix III device that provides timing for the configuration interface. After AS configuration, this pin is driven to an inactive state. In schemes that use a configuration device, DCLK will be driven low after configuration is done. In schemes that use a control host, DCLK should be driven either high or low, whichever is more convenient. Toggling this pin after configuration does not affect the configured device.
DATA0 *(1)*	N/A in AS mode. I/O in PS or FPP mode	PS, FPP, AS	Input	Data input. In serial configuration modes, bit-wide configuration data is presented to the target device on the DATA0 pin. In AS mode, DATA0 has an internal pull-up resistor that is always active. After PS or FPP configuration, DATA0 is available as a user I/O pin and the state of this pin depends on the **Dual-Purpose Pin** settings.
DATA[7..1]	I/O	Parallel configuration schemes (FPP)	Inputs	Data inputs. Byte-wide configuration data is presented to the target device on DATA[7..0]. In serial configuration schemes, they function as user I/O pins during configuration, which means they are tri-stated. After configuration, DATA[7..1] are available as user I/O pins and the state of these pin depends on the **Dual-Purpose Pin** settings.

Note to Table 11–14:

(1) To tri-state AS configuration pins in AS configuration scheme, turn on **Enable input tri-state on active configuration pins in user mode** option from the **Device and Pin Options** dialog box. This tri-states DCLK, nCSO, Data0, and ASDO pins. Dual-purpose Pins Setting for Data0 is ignored. To set Data0 to a different setting, for example to use Data0 pin as a regular I/O in user mode, turn off **Enable input tri-state on active configuration pins in user mode** option and set your desired setting from the Dual-purpose Pins Setting menu.

15. SEU Mitigation in Stratix III Devices

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This chapter describes how to use the error detection cyclical redundancy check (CRC) feature when a Stratix® III device is in user mode and recovers from CRC errors. The purpose of the error detection CRC feature is to detect a flip in any of the configuration CRAM bits in Stratix III devices due to a soft error. By using the error detection circuitry, you can continuously verify the integrity of the configuration CRAM bits.

In critical applications such as avionics, telecommunications, system control, and military applications, it is important to be able to do the following:

- Confirm that the configuration data stored in a Stratix III device is correct.
- Alert the system to the occurrence of a configuration error.

The error detection feature has been enhanced in the Stratix III device family. In addition, the error detection and recovery time for single event upset (SEU) in Stratix III devices is reduced compared to Stratix II devices.

For Stratix III devices, use of the error detection CRC feature is provided in the Quartus® II software version 6.1 and onwards.

Stratix III devices only support the error detection CRC feature at 1.1 V for V_{CCL}. This feature is not supported in Stratix III devices operating at 0.9 V for V_{CCL}.

Dedicated circuitry is built into Stratix III devices and consists of a CRC error detection feature that can optionally check for SEUs continuously and automatically.

This section describes how to activate and use the error detection CRC feature when your Stratix III device is in user mode and describes how to recover from configuration errors caused by CRC errors.

Information about SEU is located on the Products page of the Altera® website at www.altera.com.

For more information regarding the test methodology for the enhanced error detection in Stratix III, refer to *AN 539: Test Methodology of Error Detection and Recovery using CRC in Altera FPGA Devices*.

For more information, refer to the *Robust SEU Mitigation with Stratix III FPGAs White Paper*.

Using CRC error detection for the Stratix III family has no impact on fitting or performance of your device.