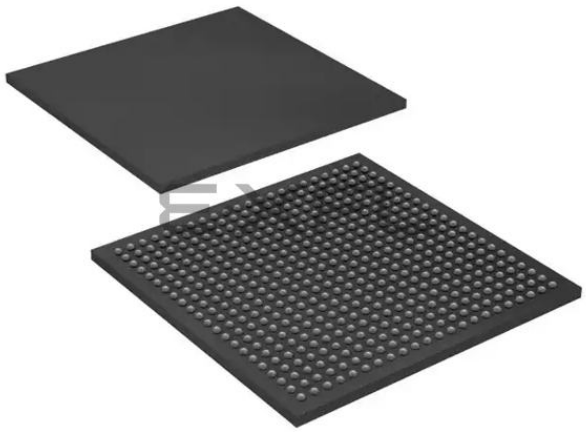

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1900
Number of Logic Elements/Cells	47500
Total RAM Bits	2184192
Number of I/O	296
Number of Gates	-
Voltage - Supply	0.86V ~ 1.15V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA, FCBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep3sl50f484c3n

MultiTrack Interconnect

In the Stratix III architecture, connections between ALMs, TriMatrix memory, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive technology. The MultiTrack interconnect consists of continuous, performance-optimized row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities. The MultiTrack interconnect provides 1-hop connection to 34 adjacent LABs, 2-hop connections to 96 adjacent LABs and 3-hop connections to 160 adjacent LABs.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement in the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the reoptimization cycles that typically follow design changes and additions. The Quartus II Compiler also automatically places critical design paths on faster interconnects to improve design performance.

For more information, refer to the *MultiTrack Interconnect in Stratix III Devices* chapter.

TriMatrix Embedded Memory Blocks

TriMatrix embedded memory blocks provide three different sizes of embedded SRAM to efficiently address the needs of Stratix III FPGA designs. TriMatrix memory includes the following blocks:

- 320-bit MLAB blocks optimized to implement filter delay lines, small FIFO buffers, and shift registers
- 9-Kbit M9K blocks that can be used for general purpose memory applications
- 144-Kbit M144K blocks that are ideal for processor code storage, packet and video frame buffering

Each embedded memory block can be independently configured to be a single- or dual-port RAM, ROM, or shift register via the Quartus II MegaWizard™ Plug-In Manager. Multiple blocks of the same type can also be stitched together to produce larger memories with minimal timing penalty. TriMatrix memory provides up to 16,272 Kbits of embedded SRAM at up to 600 MHz operation.

For more information about TriMatrix memory blocks, modes, features, and design considerations, refer to the *TriMatrix Embedded Memory Blocks in Stratix III Devices* chapter.

DSP Blocks

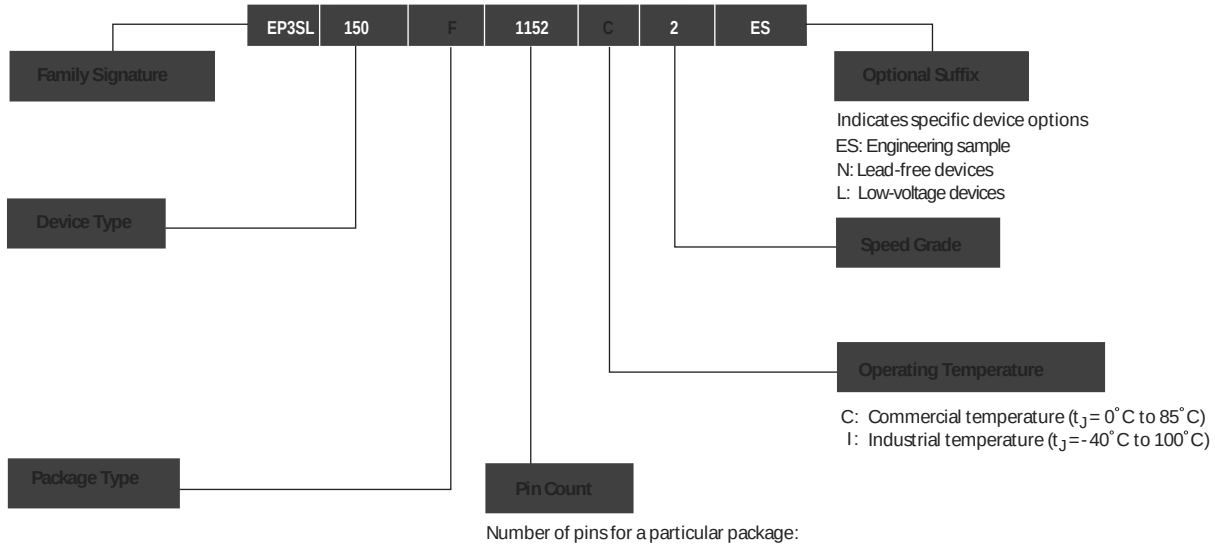
Stratix III devices have dedicated high-performance digital signal processing (DSP) blocks optimized for DSP applications requiring high data throughput. Stratix III devices provide you with the ability to implement various high-performance DSP functions easily. Complex systems such as WiMAX, 3GPP WCDMA, CDMA2000, voice over Internet Protocol (VoIP), H.264 video compression, and high-definition television (HDTV) require high-performance DSP blocks to process data. These system designs typically use DSP blocks to implement finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, and discrete cosine transform (DCT) functions.

Ordering Information

Figure 1–1 shows the ordering codes for Stratix III devices.

For more information about a specific package, refer to the *Stratix III Device Package Information* chapter.

Figure 1–1. Stratix III Device Packaging Ordering Information



Chapter Revision History

Table 1–6 lists the revision history for this chapter.

Table 1–6. Chapter Revision History (Part 1 of 2)

Date	Version	Changes Made
March 2010	1.8	Updated for the Quartus II software version 9.1 SP2 release: ■ Updated Table 1–2. ■ Updated "I/O Banks and I/O Structure" section.
May 2009	1.7	Updated "Software" and "Signal Integrity" sections.
February 2009	1.6	■ Updated "Features" section. ■ Updated Table 1–1. ■ Removed "Referenced Documents" section.
October 2008	1.5	■ Updated "Features" section. ■ Updated Table 1–1 and Table 1–5. ■ Updated New Document Format.

2. Logic Array Blocks and Adaptive Logic Modules in Stratix III Devices

SIII51002-1.5

Introduction

This chapter describes the features of the logic array block (LAB) in the Stratix® III core fabric. The logic array block is composed of basic building blocks known as adaptive logic modules (ALMs) that can be configured to implement logic functions, arithmetic functions, and register functions.

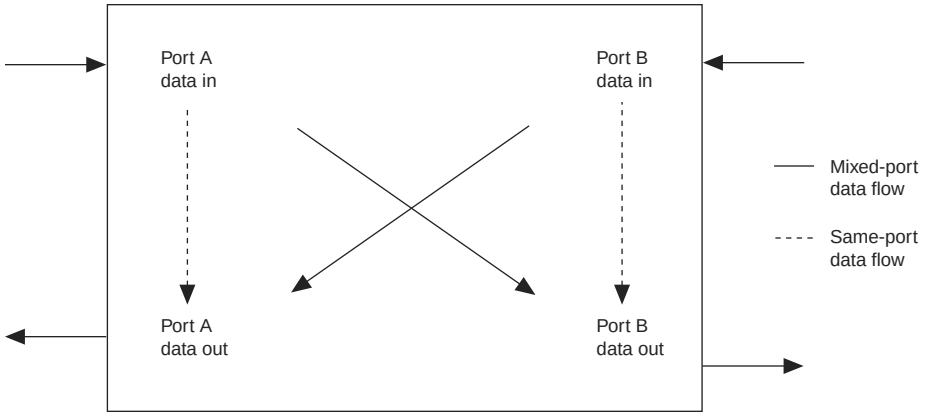
Logic Array Blocks

Each LAB consists of ten ALMs, carry chains, shared arithmetic chains, LAB control signals, local interconnect, and register chain connection lines. The local interconnect transfers signals between ALMs in the same LAB. The direct link interconnect allows a LAB to drive into the local interconnect of its left and right neighbors. Register chain connections transfer the output of the ALM register to the adjacent ALM register in an LAB. The Quartus® II Compiler places associated logic in an LAB or adjacent LABs, allowing the use of local, shared arithmetic chain, and register chain connections for performance and area efficiency. Figure 2–1 shows the Stratix III LAB structure and the LAB interconnects.

Read During Write

You can customize the read-during-write behavior of the Stratix III TriMatrix memory blocks to suit your design needs. Two types of read-during-write operations are available: same port and mixed port. Figure 4–18 shows the difference between the two types.

Figure 4–18. Stratix III Read-During-Write Data Flow

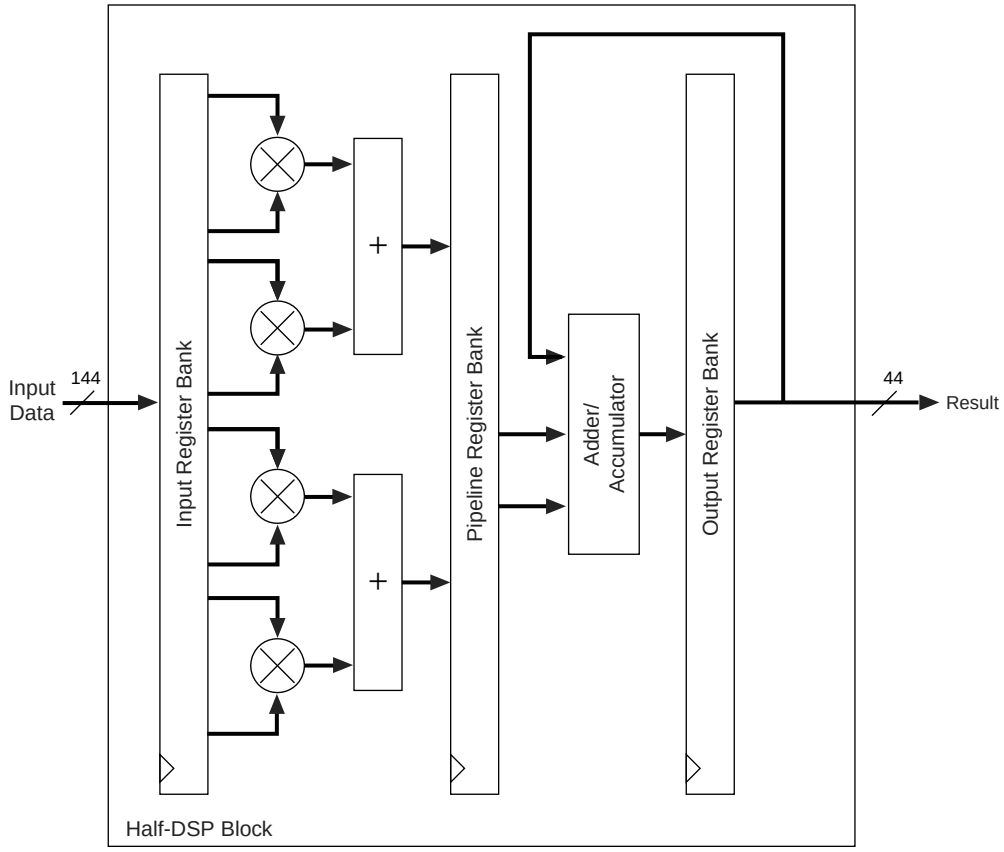


Same-Port Read-During-Write Mode

This mode applies to either a single-port RAM or the same port of a true dual-port RAM. In same-port read-during-write mode, three output choices are available: new data mode (or flow-through), old data mode, or don't care mode. In new data mode, the new data is available on the rising edge of the same clock cycle on which it was written. In old data mode, the RAM outputs reflect the old data at that address before the write operation proceeds. In don't care mode, the RAM outputs don't care values for a read-during-write operation.

If you are not using the new data mode or old data mode, you should select the don't care mode. Using the don't care mode increases the flexibility in the type of memory block used, provided you do not assign block type when instantiating a memory block. You may also get potential performance gain by selecting the don't care mode.

Figure 5–3. Four-Multiplier Adder and Accumulation Capability



To support commonly found FIR-like structures efficiently, a major addition to the DSP block in Stratix III is the ability to propagate the result of one Half-Block to the next Half-Block completely within the DSP block without additional soft logic overhead. This is achieved by the inclusion of a dedicated addition unit and routing that adds the 44-bit result of a previous Half-Block with the 44-bit result of the current block. The 44-bit result is fed either to the next Half-Block or out of the DSP block through the output register stage. This is shown in Figure 5–4. Detailed examples are described in later sections.

The combination of a fast, low-latency Four-Multiplier Adder unit and the "chained cascade" capability of the output-chaining adder provide an optimal FIR and vector multiplication capability.

To support single-channel type FIR filters efficiently, you can configure one of the multiplier input's registers to form a tap delay line input, saving resources and providing higher system performance.

Figure 5–9. 12-Bit Independent Multiplier Mode for Half-DSP Block

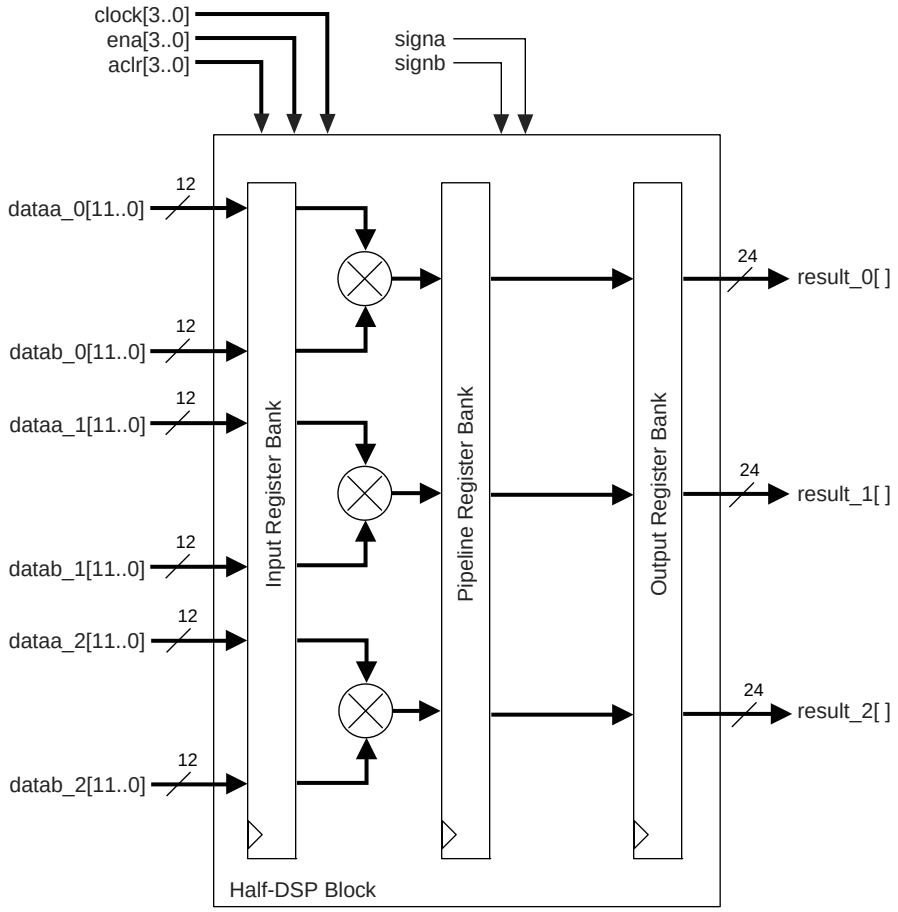


Figure 5–20. Shift Operation Mode for Half-DSP Block

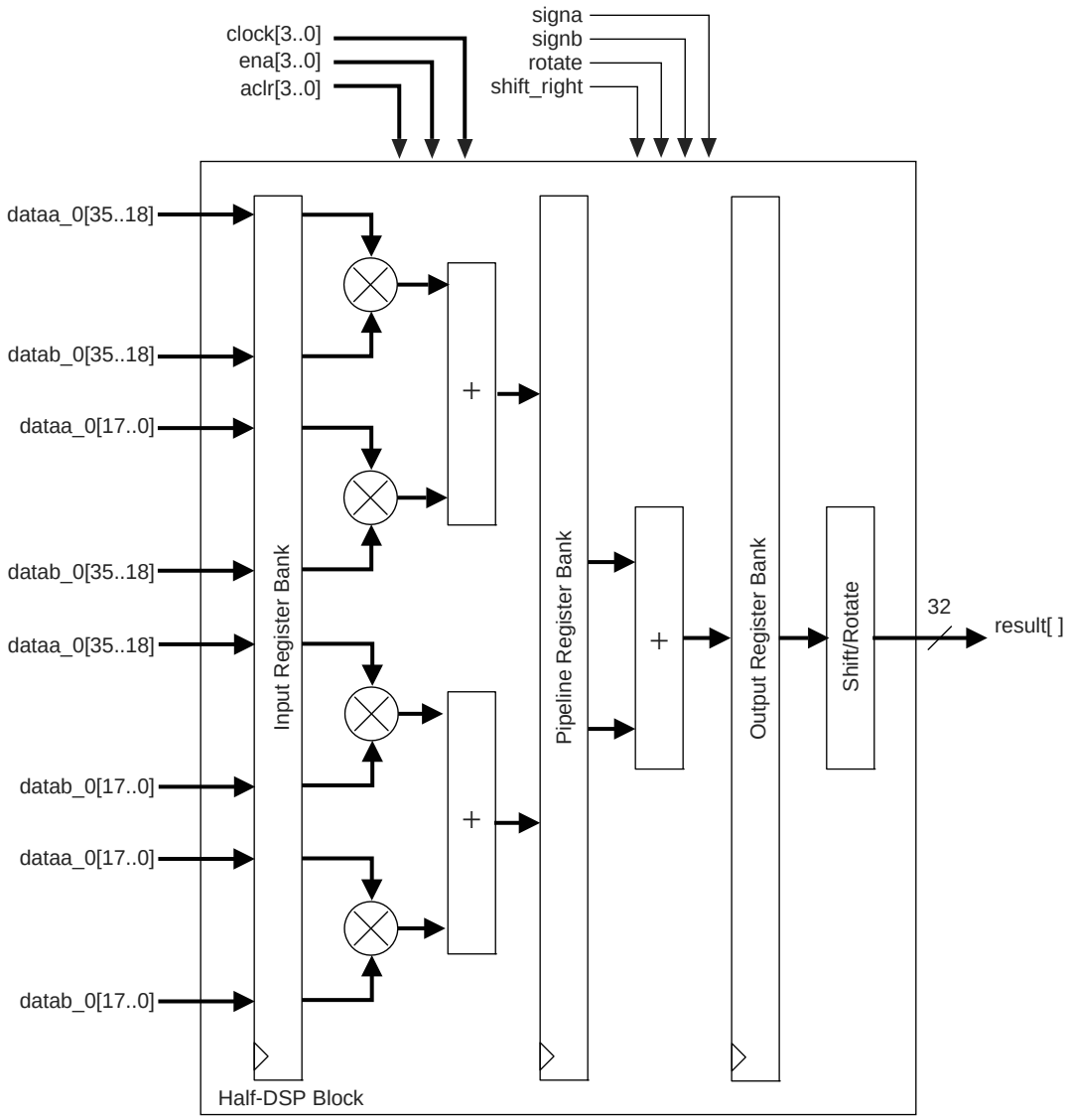
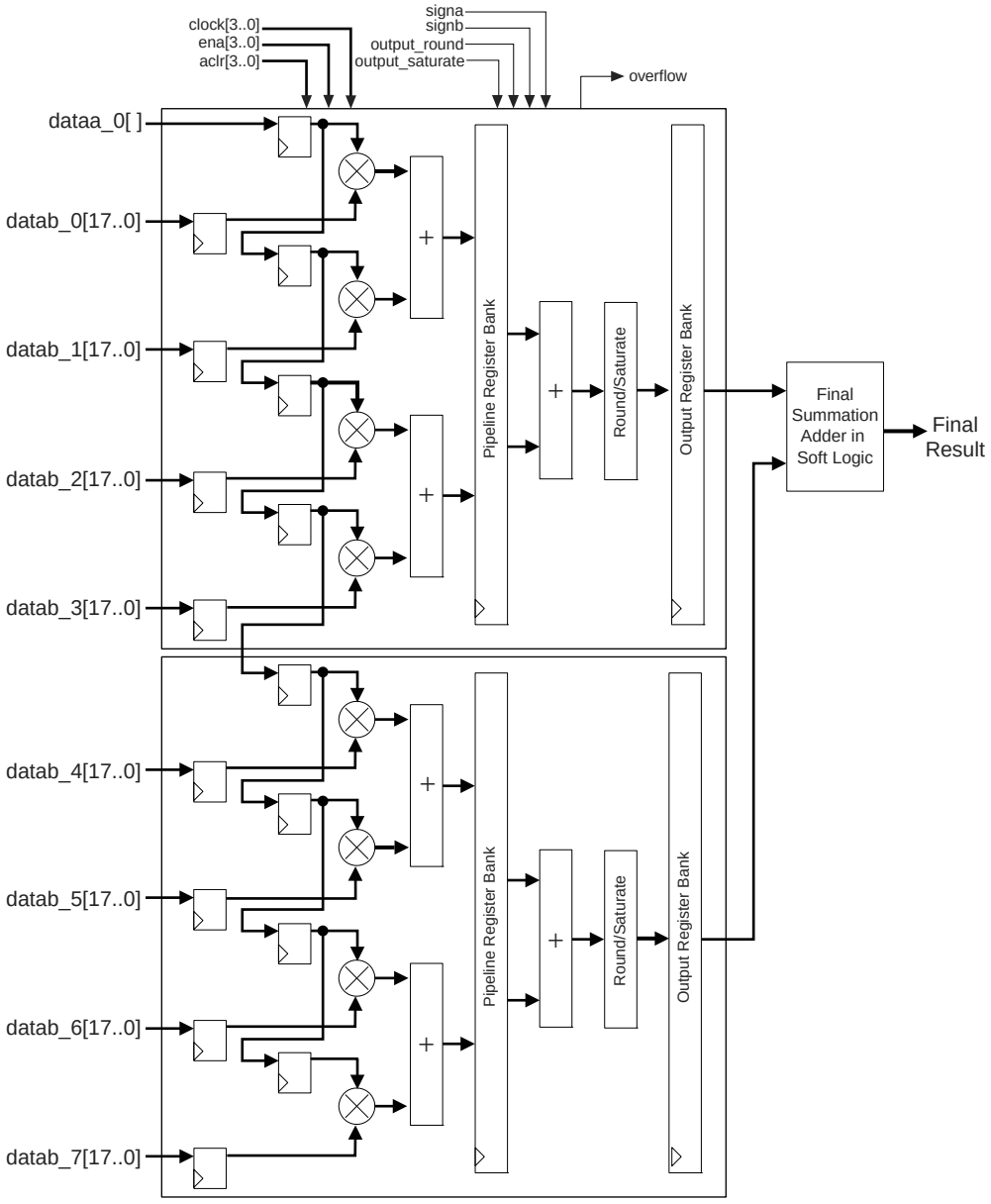


Figure 5–22. FIR Filter Using Tap-Delay Line Input and Tree Summation of Final Result



For faster and more efficient chained cascade summation, the DSP block can implement the chainout function in the cascade mode. This mode uses the second-stage 44-bit adder to add the current Four-Multiplier Adder of the half DSP block to the adjacent half DSP block of the Four-Multiplier Adder as shown in Figure 5–23.

This scheme is possible because each half DSP block has two second-stage adders. One of the two second-stage adders is used to add the current Four-Multiplier Adder. The second second-stage adder takes the output of the first second-stage adder and adds it to the adjacent half DSP block of the Four-Multiplier Adder result.

6. Clock Networks and PLLs in Stratix III Devices

SIII51006-2.0

This chapter describes the hierarchical clock networks and multiple phase-locked loops (PLLs) with advanced features in Stratix® III devices. The large number of clocking resources, in combination with the clock synthesis precision provided by the PLLs, provide a complete clock management solution. The Altera® Quartus® II software compiler automatically turns off clock networks not used in the design, thereby reducing the overall power consumption of the device.

Stratix III devices deliver abundant PLL resources with up to 12 PLLs per device and up to 10 outputs per PLL. You can independently program every output, creating a unique, customizable clock frequency. Inherent jitter filtration and fine granularity control over multiply, divide ratios, and dynamic phase shift reconfiguration provide the high performance precision required in today's high-speed applications. Stratix III device PLLs are feature-rich, supporting advanced capabilities such as clock switchover, dynamic phase shifting, PLL reconfiguration, and reconfigurable bandwidth. Stratix III PLLs also support external feedback mode, spread-spectrum tracking, and post-scale counter cascading features.

The Quartus II software enables the PLLs and their features without requiring any external devices. The following sections describe the Stratix III clock networks and PLLs in detail.

Clock Networks in Stratix III Devices

The global clock networks (GCLKs), regional clock networks (RCLKs), and periphery clock networks (PCLKs) available in Stratix III devices are organized into hierarchical clock structures that provide up to 220 unique clock domains (16 GCLKs + 88 RCLKs + 116 PCLKs) within the Stratix III device and allow up to 67 unique GCLK, RCLK, and PCLK clock sources (16 GCLKs + 22 RCLKs + 29 PCLKs) per device quadrant.

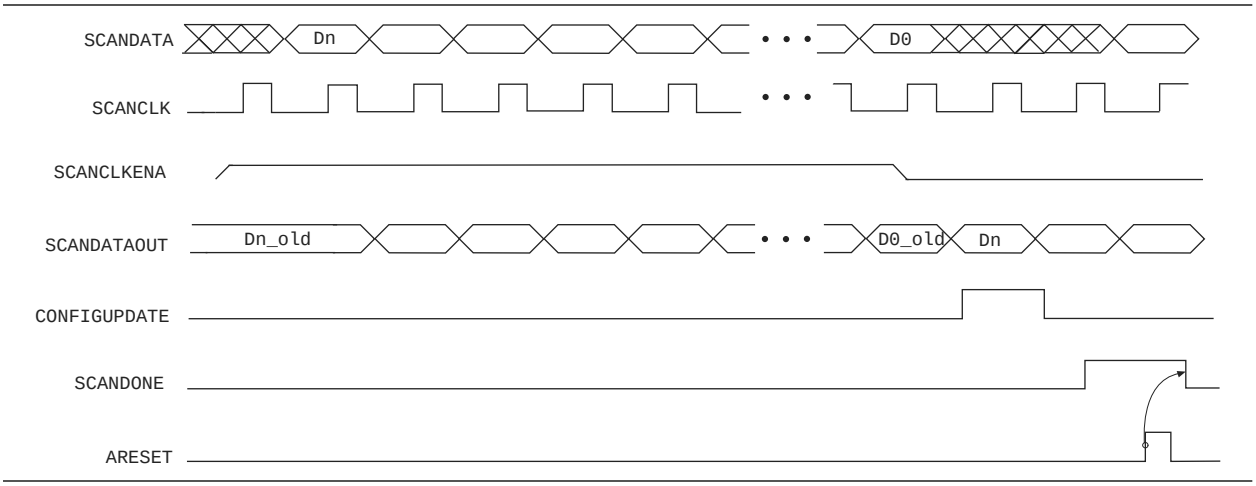
Table 6–1 lists the clock resources available in Stratix III devices.

Table 6–1. Clock Resources in Stratix III Devices (Part 1 of 2)

Clock Resource	# of Resources Available	Source of Clock Resource
Clock input pins	32 Single-ended (16 Differential)	`CLK[0..15]p` and `CLK[0..15]n` pins
Global clock networks	16	`CLK[0..15]p/n` pins, PLL clock outputs, and logic array
Regional clock networks	64/88 *(1)*	`CLK[0..15]p/n` pins, PLL clock outputs, and logic array
Peripheral clock networks	116 (29 per device quadrant) *(2)*	DPA clock outputs, horizontal I/O pins, and logic array
GCLKs/RCLKs per quadrant	32/38 *(3)*	16 GCLKs + 16 RCLKs/ 16 GCLKs + 22 RCLKs

Figure 6–41 shows a functional simulation of the PLL reconfiguration feature.

Figure 6–41. PLL Reconfiguration Waveform



When you reconfigure the counter clock frequency, you cannot reconfigure the corresponding counter phase shift settings using the same interface. Instead, reconfigure the phase shifts in real time using the dynamic phase shift reconfiguration interface. If you reconfigure the counter frequency, but wish to keep the same non-zero phase shift setting (for example, 90 degrees) on the clock output, you must reconfigure the phase shift immediately after reconfiguring the counter clock frequency.

Post-Scale Counters (C0 to C9)

The multiply or divide values and duty cycle of post-scale counters can be reconfigured in real time. Each counter has an 8-bit high-time setting and an 8-bit low-time setting. The duty cycle is the ratio of output high- or low-time to the total cycle time, which is the sum of the two. Additionally, these counters have two control bits, `rbypass`, for bypassing the counter, and `rselodd`, to select the output clock duty cycle.

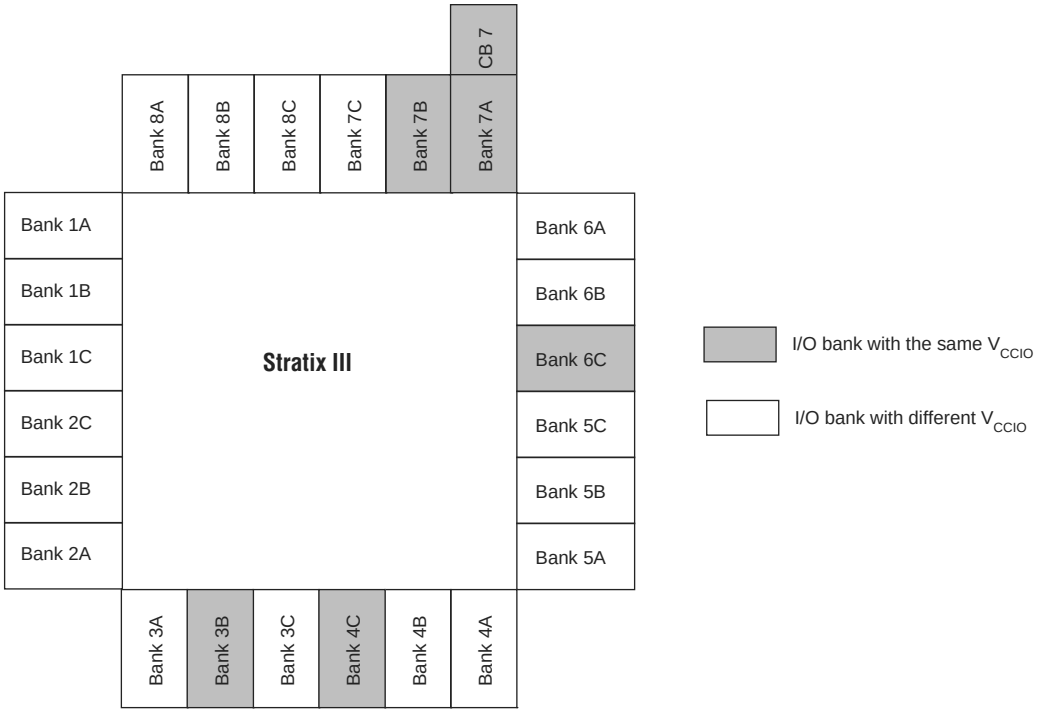
When the `rbypass` bit is set to 1, it bypasses the counter, resulting in a divide by 1. When this bit is set to 0, the high- and low-time counters are added to compute the effective division of the VCO output frequency. For example, if the post-scale divide factor is 10, the high- and low-count values could be set to 5 and 5, respectively, to achieve a 50-50% duty cycle. The PLL implements this duty cycle by transitioning the output clock from high to low on the rising edge of the VCO output clock. However, a 4 and 6 setting for the high- and low-count values, respectively, would produce an output clock with 40-60% duty cycle.

Sharing an OCT Calibration Block in Multiple I/O Banks

An OCT calibration block has the same V_{CCIO} as the I/O bank that contains the block. OCT R_S calibration is supported on all I/O banks with different V_{CCIO} voltage standards, up to the number of available OCT calibration blocks. You can configure I/O banks to receive calibrated codes from any OCT calibration block with the same V_{CCIO}. All I/O banks with the same V_{CCIO} can share one OCT calibration block, even if that particular I/O bank has an OCT calibration block.

For example, Figure 7–16 shows a group of I/O banks that have the same V_{CCIO} voltage. If a group of I/O banks have the same V_{CCIO} voltage, you can use one OCT calibration block to calibrate the group of I/O banks placed around the periphery. Because 3B, 4C, 6C, and 7B have the same V_{CCIO} as bank 7A, you can calibrate all four I/O banks (3B, 4C, 6C, and 7B) with the OCT calibration block located in bank 7A. You can enable this by serially shifting out OCT R_S calibration codes from the OCT calibration block located in bank 7A to the I/O banks located around the periphery.

Figure 7–16. Example of Sharing Multiple I/O Banks with One OCT Calibration Block *(Note 1)*



Note to Figure 7–16:

(1) Figure 7–16 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

OCT Calibration Block Modes of Operation

Stratix III devices support calibration OCT R_S and OCT R_T in all I/O banks. The calibration can occur in either power-up mode or user mode.

Power-Up Mode

In power-up mode, OCT calibration is automatically performed at power up and calibrated codes are shifted to selected I/O buffers before transitioning to user mode.

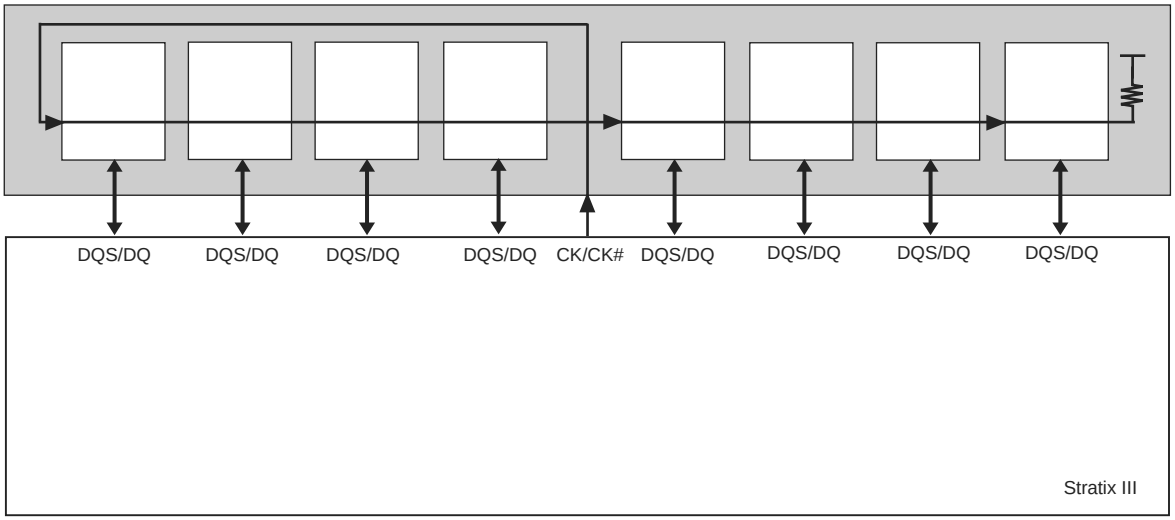
You must pick your DQS and DQ pins manually for the ×8, ×16/×18, or ×32/×36 DQS/DQ group whose members are being used for RUP and RDN because the Quartus II software might not be able to place this correctly when there are no specific pin assignments and might give you a "no-fit" instead.

Table 8–2 lists the maximum number of DQS/DQ groups per side of the Stratix III device. For a more detailed listing of the number of DQS/DQ groups available per bank in each Stratix III device, refer to Figure 8–3 through Figure 8–7. These figures represent the package bottom view of the Stratix III device.

Table 8–2. Number of DQS/DQ Groups in Stratix III Devices per Side (Part 1 of 2)

Device	Package	Side	×4 *(1)*	×8/×9	×16/×18	×32/×36 *(2)*
EP3SE50 EP3SL50 EP3SL70	484-pin FineLine BGA	Left/ Right	12	4	0	0
		Top/ Bottom	5	2	0	0
	780-pin FineLine BGA	Left/ Right	14	6	2	0
		Top/ Bottom	17	8	2	0
EP3SE80 EP3SE110 EP3SL110 EP3SL150	780-pin FineLine BGA	Left/ Right	14	6	2	0
		Top/ Bottom	17	8	2	0
	1152-pin FineLine BGA	Left/ Right	26	12	4	0
		Top/ Bottom	26	12	4	0
EP3SL200	780-pin Hybrid FineLine BGA	Left/ Right	14	6	2	0
		Top/ Bottom	17	8	2	0
	1152-pin FineLine BGA	Left/ Right	26	12	4	0
		Top/ Bottom	26	12	4	0
	1517-pin FineLine BGA	Left/ Right	34	16	6	0
		Top/ Bottom	38	18	8	4
EP3SE260	780-pin Hybrid FineLine BGA	Left/ Right	14	6	2	0
		Top/ Bottom	17	8	2	0
	1152-pin FineLine BGA	Left/ Right	26	12	4	0
		Top/ Bottom	26	12	4	0
	1517-pin FineLine BGA	Left/ Right	34	16	6	0
		Top/ Bottom	38	18	8	4

Figure 8–16. DDR3 SDRAM Unbuffered Module Clock Topology



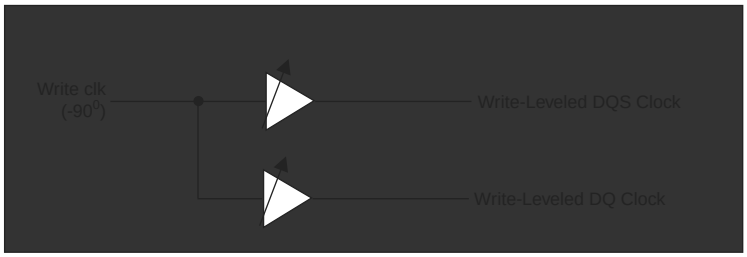
Because the data and read strobe signals are still point-to-point, special consideration must be taken to ensure that the timing relationship between CK/CK# and DQS signals (t_{DQSS}) during a write is met at every device on the modules. Furthermore, read data coming back into the FPGA from the memory is also staggered in a similar way.

Stratix III FPGAs have leveling circuitry to take care of these two requirements. There is one group of leveling circuitry per I/O bank, with the same I/O number (for example, there is one leveling circuitry shared between I/O bank 1A, 1B, and 1C) located in the middle of the I/O bank. These delay chains are PVT-compensated by the same DQS delay settings as the DLL and DQS delay chains. For frequencies equal to and above 400 MHz, the DLL uses eight delay chains such that each delay chain generates a 45° delay.

The generated clock phases are distributed to every DQS logic block that is available in the I/O bank. The delay chain taps, then feeds a multiplexer controlled by the ALTMEMPHY megafunction to select which clock phases are to be used for that ×4 or ×8 DQS group. Each group can use a different tap output from the read-leveling and write-leveling delay chains to compensate for the different CK/CK# delay going into each device on the module.

Figure 8–17 illustrates the Stratix III write leveling circuitry.

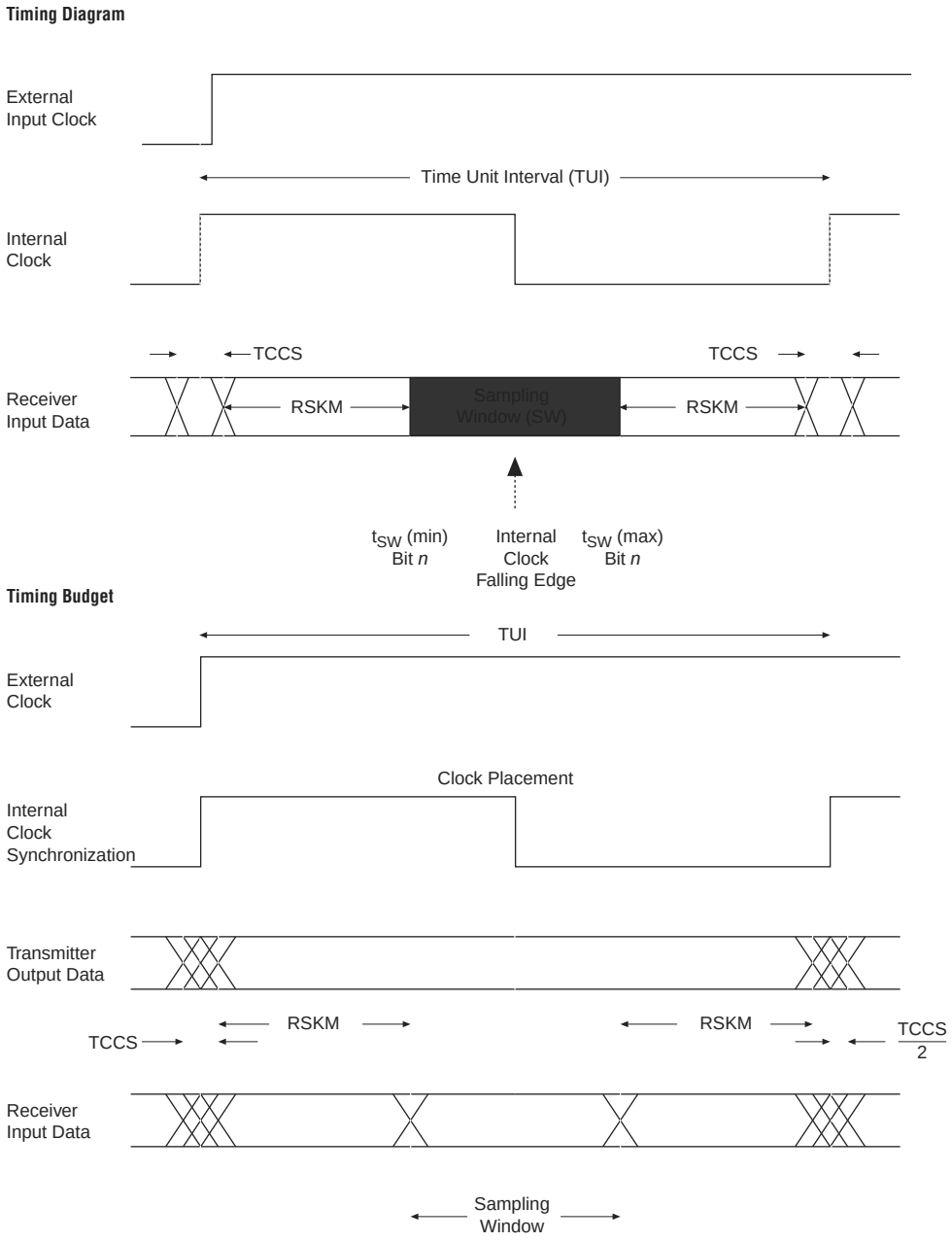
Figure 8–17. Stratix III Write Leveling Delay Chains and Multiplexers *(Note 1)*



Note to Figure 8–17:

(1) There is only one leveling delay chain per I/O bank with the same I/O number (for example, I/O banks 1A, 1B, and 1C). You can only have one memory controller in these I/O banks when you use leveling delay chains.

Figure 9–17. Differential High-Speed Timing Diagram and Timing Budget for Non-DPA



If you have enabled the **Auto-restart configuration after error** option, the nSTATUS pin transitions from high to low and back again to high when a configuration error is detected. This appears as a low pulse at the nSTATUS pin with a minimum pulse width of 10 µs to a maximum pulse width of 500 µs, as defined in the t_{STATUS} specification.

When the Stratix III device is in user mode, you can initiate reconfiguration by pulling the nCONFIG pin low. The nCONFIG pin should be low for at least 2 µs. When nCONFIG is pulled low, the device also pulls nSTATUS and CONF_DONE low and all I/O pins are tri-stated. When nCONFIG returns to a logic high level and nSTATUS is released by the Stratix III device, reconfiguration begins.

You can configure multiple Stratix III devices using a single serial configuration device. You can cascade multiple Stratix III devices using the chip-enable (nCE) and chip-enable-out (nCEO) pins. The first device in the chain must have its nCE pin connected to ground. You must connect its nCEO pin to the nCE pin of the next device in the chain. When the first device captures all of its configuration data from the bitstream, it drives the nCEO pin low, enabling the next device in the chain. You must leave the nCEO pin of the last device unconnected. The nCONFIG, nSTATUS, CONF_DONE, DCLK, and DATA0 pins of each device in the chain are connected (refer to Figure 11–9).

This first Stratix III device in the chain is the configuration master and controls configuration of the entire chain. You must connect its MSEL pins to select the AS configuration scheme. The remaining Stratix III devices are configuration slaves. You must connect their MSEL pins to select the PS configuration scheme. Any other Altera device that supports PS configuration can also be part of the chain as a configuration slave. Figure 11–9 shows the pin connections for this setup.

Table 11–14. Dedicated Configuration Pins on the Stratix III Device (Part 4 of 5)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
CONF_DONE	N/A	All	Bi-directional open-drain	Status output. The target device drives the CONF_DONE pin low before and during configuration. After all configuration data is received without error and the initialization cycle starts, the target device releases CONF_DONE. Status input. After all data is received and CONF_DONE goes high, the target device initializes and enters user mode. The CONF_DONE pin must have an external 10-kΩ pull-up resistor in order for the device to initialize. Driving CONF_DONE low after configuration and initialization does not affect the configured device. Do not connect bus holds or ADC to CONF_DONE pin.
nCE	N/A	All	Input	Active-low chip enable. The nCE pin activates the device with a low signal to allow configuration. The nCE pin must be held low during configuration, initialization, and user mode. In single device configuration, it should be tied low. In multi-device configuration, nCE of the first device is tied low while its nCEO pin is connected to nCE of the next device in the chain. The nCE pin must also be held low for successful JTAG programming of the device.
nCEO	N/A	All	Output	Output that drives low when device configuration is complete. In single device configuration, this pin is left floating. In multi-device configuration, this pin feeds the next device's nCE pin. The nCEO of the last device in the chain is left floating. The nCEO pin is powered by V_{CCPGM}.
ASDO *(1)*	N/A	AS	Output	Control signal from the Stratix III device to the serial configuration device in AS mode used to read out configuration data. In AS mode, ASDO has an internal pull-up resistor that is always active.
nCSO *(1)*	N/A	AS	Output	Output control signal from the Stratix III device to the serial configuration device in AS mode that enables the configuration device. In AS mode, nCSO has an internal pull-up resistor that is always active.

Table 12–3. Remote System Upgrade Control Register Contents (Part 2 of 2)

Control Register Bit	Remote System Upgrade Mode	Value *(2)*	Definition
wd_en	Remote update	1'b0	User watchdog timer enable bit
wd_timer[11..0]	Remote update	12'b000000000000	User watchdog time-out value (most significant 12 bits of 29-bit count value: {wd_timer[11..0], 17'b0})

Notes to Table 12–3:

(1) In remote update mode, the remote configuration block does not update the AnF bit automatically (you can update it manually).

(2) This is the default value of the control register bit.

Remote System Upgrade Status Register

The remote system upgrade status register specifies the reconfiguration trigger condition. The various trigger and error conditions include in the following:

- Cyclic redundancy check (CRC) error during application configuration
- nSTATUS assertion by an external device due to an error
- Stratix III device logic array triggers a reconfiguration cycle, possibly after downloading a new application configuration image
- External configuration reset (nCONFIG) assertion
- User watchdog timer time out

Figure 12–7 and Table 12–4 specify the contents of the status register. The numbers in the figure show the bit positions within a 5-bit register.

Figure 12–7. Remote System Upgrade Status Register

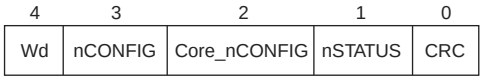


Table 12–4. Remote System Upgrade Status Register Contents

Status Register Bit	Definition	POR Reset Value
CRC (from configuration)	CRC error caused reconfiguration	1 bit '0'
nSTATUS	nSTATUS caused reconfiguration	1 bit '0'
CORE_nCONFIG *(1)*	Device logic array caused reconfiguration	1 bit '0'
nCONFIG	nCONFIG caused reconfiguration	1 bit '0'
wd	Watchdog timer caused reconfiguration	1 bit '0'

Note to Table 12–4:

(1) Logic array reconfiguration forces the system to load the application configuration data into the Stratix III device. This occurs after the factory configuration specifies the appropriate application configuration page address by updating the update register.