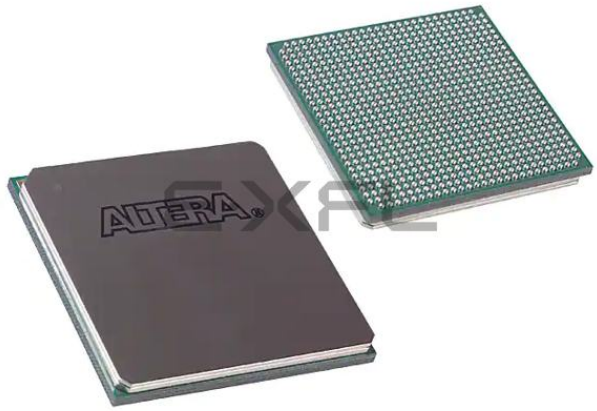

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1900
Number of Logic Elements/Cells	47500
Total RAM Bits	2184192
Number of I/O	488
Number of Gates	-
Voltage - Supply	0.86V ~ 1.15V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep3sl50f780c3n

SIII5V1-2.2

Stratix III devices have up to 112 DSP blocks. The architectural highlights of the Stratix III DSP block are the following:

- High-performance, power optimized, fully pipelined multiplication operations
- Native support for 9-bit, 12-bit, 18-bit, and 36-bit word lengths
- Native support for 18-bit complex multiplications
- Efficient support for floating point arithmetic formats (24-bit for Single Precision and 53-bit for Double Precision)
- Signed and unsigned input support
- Built-in addition, subtraction, and accumulation units to efficiently combine multiplication results
- Cascading 18-bit input bus to form tap-delay lines
- Cascading 44-bit output bus to propagate output results from one block to the next block
- Rich and flexible arithmetic rounding and saturation units
- Efficient barrel shifter support
- Loopback capability to support adaptive filtering

DSP block multipliers can optionally feed an adder/subtractor or accumulator in the block depending on user configuration. This option saves ALM routing resources and increases performance, because all connections and blocks are inside the DSP block. Additionally, the DSP Block input registers can efficiently implement shift registers for FIR filter applications, and the Stratix III DSP blocks support rounding and saturation. The Quartus II software includes megafunctions that control the mode of operation of the DSP blocks based on user parameter settings.

For more information, refer to the *DSP Blocks in Stratix III Devices* chapter.

Clock Networks and PLLs

Stratix III devices provide dedicated Global Clock Networks (GCLKs), Regional Clock Networks (RCLKs), and Periphery Clock Networks (PCLKs). These clocks are organized into a hierarchical clock structure that provides up to 104 unique clock domains (16 GCLK + 88 RCLK) within the Stratix III device and allows for up to 38 (16 GCLK + 22 RCLK) unique GCLK/RCLK clock sources per device quadrant.

Stratix III devices deliver abundant PLL resources with up to 12 PLLs per device and up to 10 outputs per PLL. Every output can be independently programmed, creating a unique, customizable clock frequency. Inherent jitter filtration and fine granularity control over multiply, divide ratios, and dynamic phase-shift reconfiguration provide the high-performance precision required in today's high-speed applications. Stratix III PLLs are feature rich, supporting advanced capabilities such as clock switchover, reconfigurable phase shift, PLL reconfiguration, and reconfigurable bandwidth. PLLs can be used for general-purpose clock management supporting multiplication, phase shifting, and programmable duty cycle. Stratix III PLLs also support external feedback mode, spread-spectrum input clock tracking, and post-scale counter cascading.

Round and Saturation Stage

The round and saturation logic units are located at the output of the 44-bit second-stage adder (round logic unit followed by the saturation logic unit). There are two round and saturation logic units per half DSP block. The input to the round and saturation logic unit can come from one of the following stages:

- Output of the multiplier (independent multiply mode in 18 × 18)
- Output of the first-stage adder (Two-Multiplier Adder)
- Output of the pipeline registers
- Output of the second-stage adder (Four-Multiplier Adder, Multiply-Accumulate Mode in 18 × 18)

These stages are discussed in detail in "Operational Mode Descriptions" on page 5–15.

The round and saturation logic unit is controlled by the dynamic round and saturate signals, respectively. A `logic 1` value on the round, saturate, or both enables the round, saturate, or both logic units.

You can use the round and saturation logic units together or independently.

Second Adder and Output Registers

The second adder register and output register banks are two banks of 44-bit registers that can also be combined to form larger 72-bit banks to support 36 × 36 output results.

The outputs of the different stages in the Stratix III devices are routed to the output registers through an output selection unit. Depending on the operational mode of the DSP block, the output selection unit selects whether the outputs of the DSP blocks comes from the outputs of the multiplier block, first-stage adder, pipeline registers, second-stage adder, or the round and saturation logic unit. The output selection unit is set automatically by the software, based on the DSP block operational mode you specified, and has the option to either drive or bypass the output registers. The exception is when the block is used in shift mode, in which case the user dynamically controls the output-select multiplexer directly.

When the DSP block is configured in "chained cascaded" output mode, both of the second-stage adders are used. The first one is used for performing Four-Multiplier Adder and the second is used for the chainout adder. The outputs of the Four-Multiplier Adder are routed to the second-stage adder registers before it enters the chainout adder. The output of the chainout adder goes to the regular output register bank. Depending on the configuration, the chainout results can be routed to the input of the next half-block's chainout adder input or to the general fabric (functioning as regular output registers). Refer to "Operational Mode Descriptions" on page 5–15 for details.

Table 6–6 lists the connectivity between the dedicated clock input pins and RCLKs in device Quadrant 4. A given clock input pin can drive two adjacent regional clock networks to create a dual-regional clock network.

Table 6–6. Clock Input Pin Connectivity to Regional Clock Networks (Quadrant 4)

Clock Resource	CLK (p/n Pins)															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RCLK6	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK7	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK8	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK9	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—
RCLK10	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK11	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK12	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—
RCLK13	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—
RCLK14	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—
RCLK15	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—
RCLK16	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—
RCLK17	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—
RCLK18	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—
RCLK19	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—
RCLK20	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—
RCLK21	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—

Table 6–7 lists the dedicated clock input pin connectivity to Stratix III device PLLs.

Table 6–7. Stratix III Device PLLs and PLL Clock Pin Drivers (Part 1 of 2) *(Note 1)*

Dedicated Clock Input Pin (CLKp/n pins)	PLL Number											
	L1	L2	L3	L4	B1	B2	R1	R2	R3	R4	T1	T2
CLK0	✓	✓	✓	✓	—	—	—	—	—	—	—	—
CLK1	✓	✓	✓	✓	—	—	—	—	—	—	—	—
CLK2	✓	✓	✓	✓	—	—	—	—	—	—	—	—
CLK3	✓	✓	✓	✓	—	—	—	—	—	—	—	—
CLK4	—	—	—	—	✓	✓	—	—	—	—	—	—
CLK5	—	—	—	—	✓	✓	—	—	—	—	—	—
CLK6	—	—	—	—	✓	✓	—	—	—	—	—	—
CLK7	—	—	—	—	✓	✓	—	—	—	—	—	—
CLK8	—	—	—	—	—	—	✓	✓	✓	✓	—	—
CLK9	—	—	—	—	—	—	✓	✓	✓	✓	—	—
CLK10	—	—	—	—	—	—	✓	✓	✓	✓	—	—
CLK11	—	—	—	—	—	—	✓	✓	✓	✓	—	—
CLK12	—	—	—	—	—	—	—	—	—	—	✓	✓

Programmable Bandwidth

Stratix III PLLs provide advanced control of the PLL bandwidth using the PLL loop's programmable characteristics, including loop filter and charge pump.

Background

PLL bandwidth is the measure of the PLL's ability to track the input clock and its associated jitter. The closed-loop gain 3-dB frequency in the PLL determines the PLL bandwidth. The bandwidth is approximately the unity gain point for open loop PLL response. As Figure 6–37 shows, these points correspond to approximately the same frequency. Stratix III PLLs provide three bandwidth settings—low, medium (default), and high.

Figure 6–37. Open- and Closed-Loop Response Bode Plots

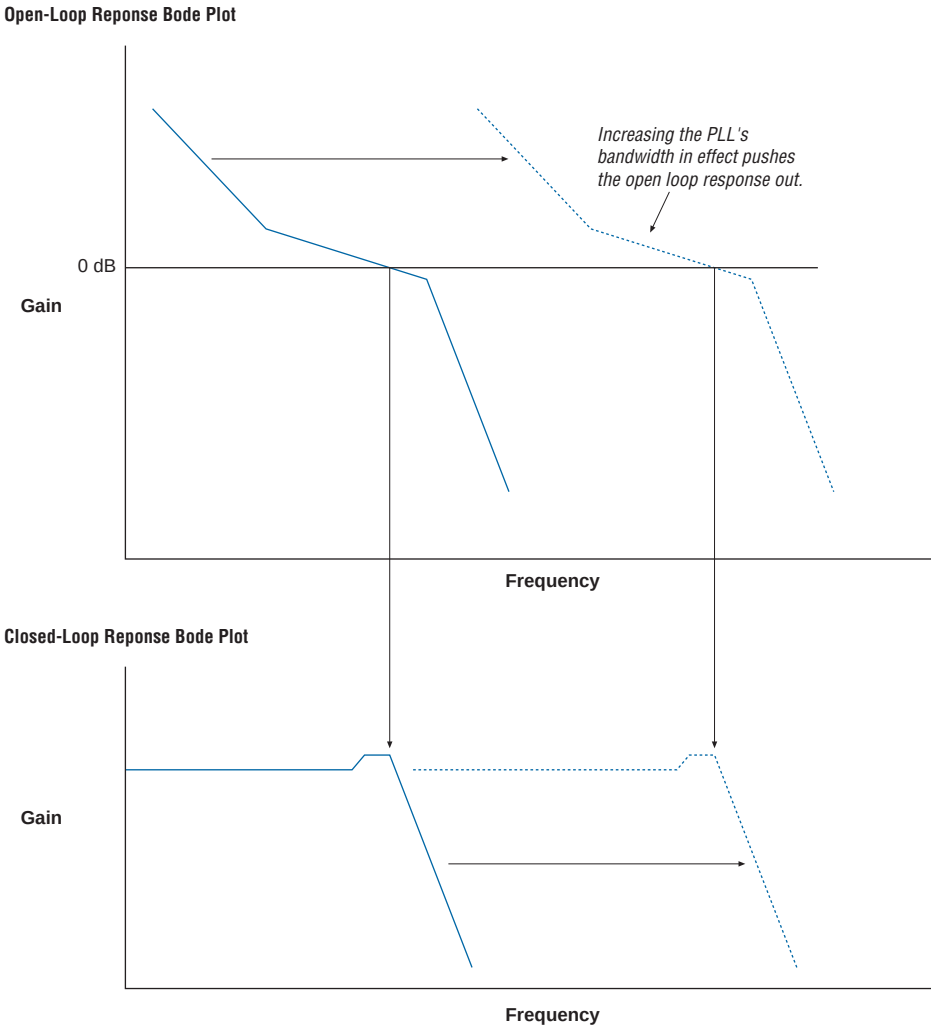
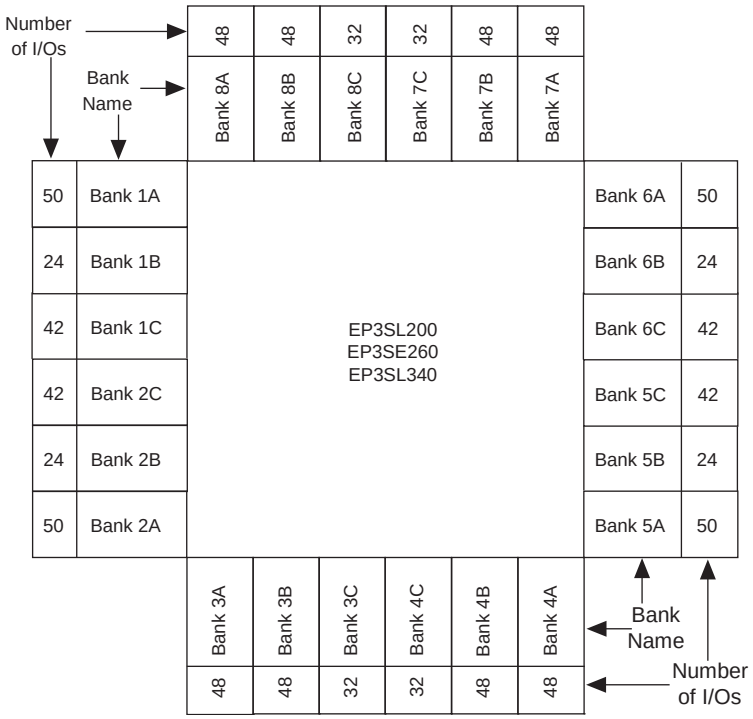


Figure 7–5. Number of I/Os in Each Bank in EP2SL200, EP3SE260, and EP3SL340 Devices in the 1517-Pin FineLine BGA Package *(Note 1)*, *(2)*

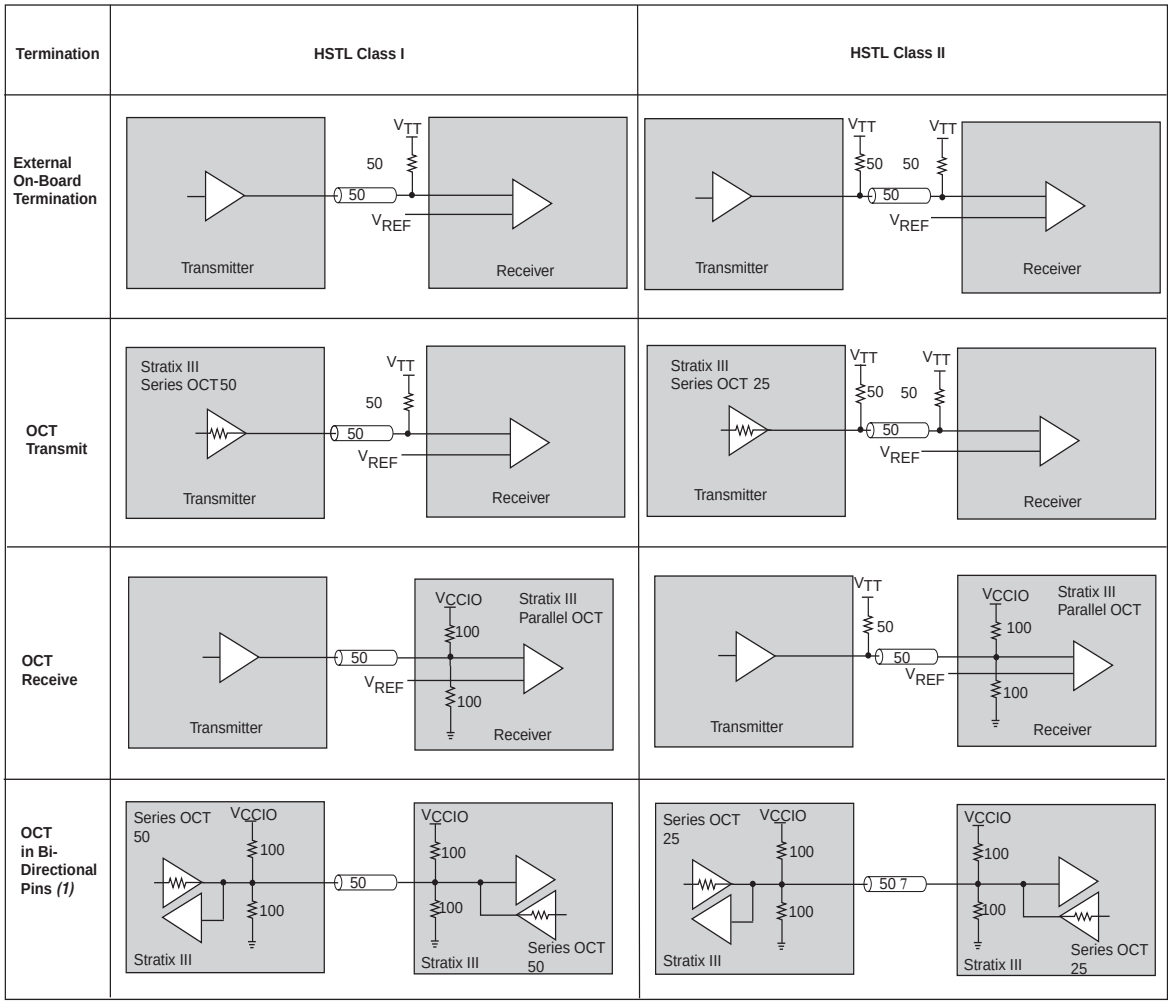


Notes to Figure 7–5:

(1) All I/O pin counts include dedicated clock inputs pins. The pin count includes all general purpose I/O, dedicated clock pins, and dual-purpose configuration pins. Dedicated configuration pins are not included in the pin count.

(2) Figure 7–5 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

Figure 7–21. HSTL I/O Standard Termination for Stratix III Devices



Note to Figure 7–21:

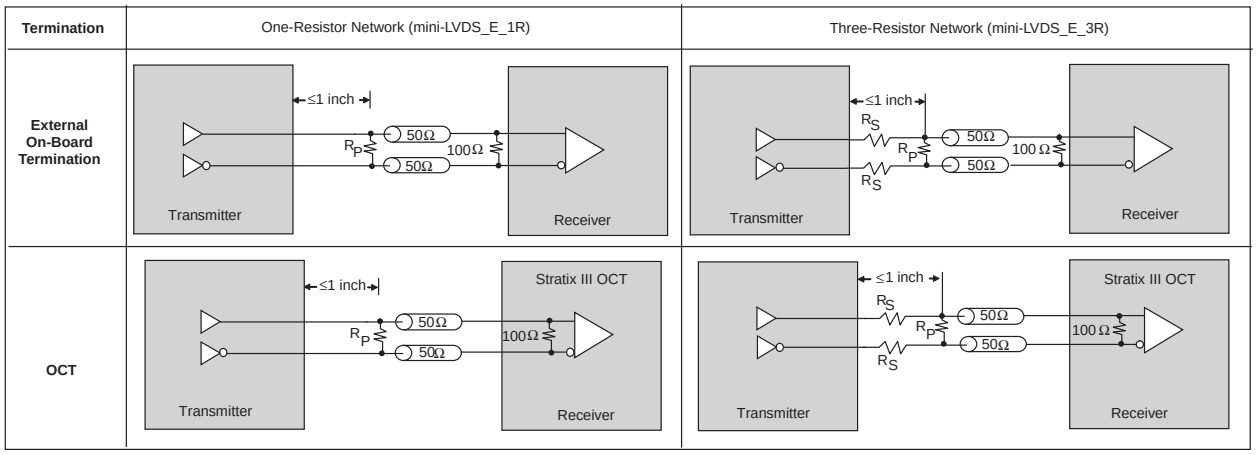
(1) In Stratix III devices, you cannot use simultaneously series and parallel OCT. For more information, refer to "Dynamic OCT" on page 7–25.

Differential I/O Standards Termination

Stratix III devices support differential SSTL-2 and SSTL-18, differential HSTL-18, HSTL-15, HSTL-12, LVDS, LVPECL, RSDS, and mini-LVDS. Figure 7–22 through Figure 7–28 show the details of various differential I/O termination on Stratix III devices.

Differential HSTL and SSTL outputs are not true differential outputs. They use two single-ended outputs with the second output programmed as inverted.

Figure 7–28. Mini-LVDS I/O Standard Termination for Stratix III Devices *(Note 1)*, *(2)*



Notes to Figure 7–28:

(1) R_P=120 Ω for mini-LVDS_E_1R, R_P=170 Ω, and R_S=120 Ω for mini-LVDS_E_3R.

(2) Column and row I/O banks support mini-LVDS_E_1R and mini-LVDS_E_3R I/O standards using two single-ended output buffers.

A resistor network is required to attenuate the LVDS output voltage swing to meet the mini-LVDS specifications. You can modify the three-resistor network values to reduce power or improve the noise margin. The resistor values chosen should satisfy Equation 7–2:

Equation 7–2.

$$\frac{Rs \times \frac{Rp}{2}}{Rs + \frac{Rp}{2}} = 50\Omega$$

Altera recommends that you perform additional simulations using IBIS models to validate that custom resistor values meet the RSDS requirements.

For more information about the mini-LVDS I/O standard, refer to the *mini-LVDS Specification* from the Texas Instruments website.

Design Considerations

While Stratix III devices feature various I/O capabilities for high-performance and high-speed system designs, there are several other considerations that require attention to ensure the success of those designs.

Memory Clock Pins

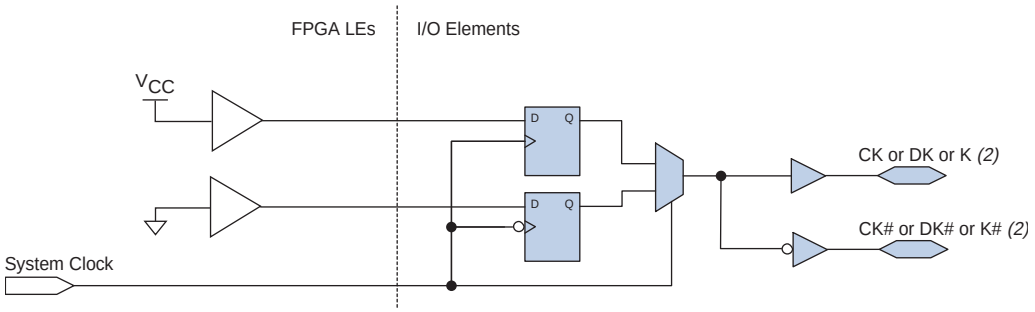
In addition to DQS (and CQn) signals to capture data, DDR3, DDR2, DDR SDRAM, and RLDRAM II use an extra pair of clocks, called CK and CK# signals, to capture the address and control/command signals. The CK/CK# signals must be generated to mimic the write data-strobe using Stratix III DDR I/O registers (DDIOs) to ensure that timing relationships between the CK/CK# and DQS signals (t_{DQSS} in DDR3, DDR2, and DDR SDRAM or t_{CKDK} in RLDRAM II) are met. QDR II+ and QDR II SRAM devices use the same clock (K/K#) to capture data, address, and control/command signals.

Memory clock pins in Stratix III devices are generated with a DDIO register going to differential output pins, marked in the pin table with `DIFFOUT`, `DIFFIO_TX`, and `DIFFIO_RX` prefixes.

For more information about which pins to use for memory clock pins, refer to the *Section I. Device and Pin Planning* chapter in volume 2 of the *External Memory Interface Handbook*.

Figure 8–9 shows the memory clock generation block diagram for Stratix III devices.

Figure 8–9. Memory Clock Generation Block Diagram *(Note 1)*



Notes to Figure 8–9:

(1) For more information about pin location requirements for these pins, refer *Section I. Device and Pin Planning* chapter in volume 2 of the *External Memory Interface Handbook*.

(2) The `mem_clk[0]` and `mem_clk_n[0]` pins for DDR3, DDR2, and DDR SDRAM interfaces use the I/O input buffer for feedback; therefore, bi-directional I/O buffers are used for these pins. For memory interfaces using a differential DQS input, the input feedback buffer is configured as differential input; for memory interfaces using a single-ended DQS input, the input buffer is configured as a single-ended input. Using a single-ended input feedback buffer requires that I/O standard's V_{REF} voltage is provided to that I/O bank's VREF pins.

Stratix III External Memory Interface Features

Stratix III devices are rich with features that allow robust high-performance external memory interfacing. The ALTMEMPHY megafunction allows you to set these external memory interface features and helps set up the physical interface (PHY) best suited for your system. This section describes each Stratix III device feature that is used in external memory interfaces from the DQS phase-shift circuitry, DQS logic block, leveling multiplexers, dynamic OCT control block, IOE registers, IOE features, and PLLs.

10. Hot Socketing and Power-On Reset in Stratix III Devices

SIII51010-1.7

This chapter describes information about hot-socketing specifications, power-on reset (POR) requirements, and their implementation in Stratix® III devices.

Stratix III devices offer hot socketing, also known as hot plug-in or hot swap, and power sequencing support without the use of any external devices. You can insert or remove a Stratix III device or a board in a system during system operation without causing undesirable effects to the running system bus or board that is inserted into the system.

The hot socketing feature also removes some of the difficulty when you use Stratix III devices on PCBs that contain a mixture of 3.3-, 3.0-, 2.5-, 1.8-, 1.5-, and 1.2-V devices. With the Stratix III hot socketing feature, you no longer need to ensure a proper power-up sequence for each device on the board.

The Stratix III hot-socketing feature provides:

- Board or device insertion and removal without external components or board manipulation
- Support for any power-up sequence
- I/O buffers non-intrusive to system buses during hot insertion

This section also describes the POR circuitry in Stratix III devices. POR circuitry keeps the devices in the reset state until the power supplies are within operating range.

Stratix III Hot-Socketing Specifications

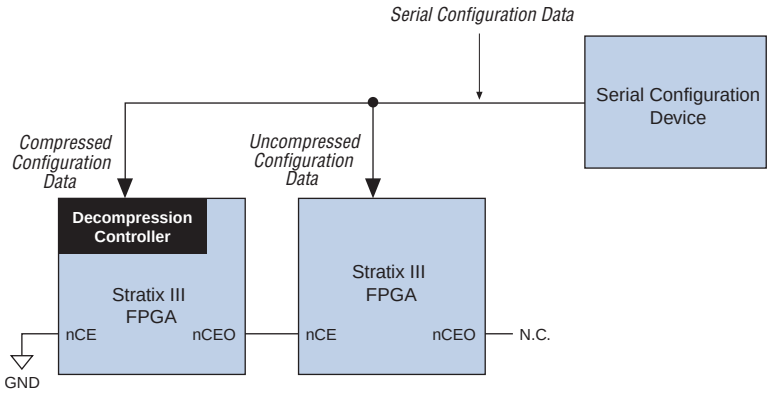
Stratix III devices are hot-socketing compliant without the need for external components or special design requirements. Hot socketing support in Stratix III devices has the following advantages:

- You can drive the device before power-up without damaging it.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby not affecting other buses in operation.
- You can insert a Stratix III device into or remove it from a powered-up system board without damaging or interfering with normal system/board operation.

Stratix III Devices Can Be Driven Before Power Up

You can drive signals into I/O pins, dedicated input pins, and dedicated clock pins of Stratix III devices before or during power up or power down without damaging the device. Stratix III devices support power up or power down of the power supplies in any sequence in order to simplify system-level design.

Figure 11–2. Compressed and Uncompressed Configuration Data in the Same Configuration File



To generate programming files for this setup in the Quartus II software, on the File menu, click **Convert Programming Files**.

Design Security Using Configuration Bitstream Encryption

Stratix III devices support decryption of configuration bitstreams using the advanced encryption standard (AES) algorithm—the most advanced encryption algorithm available today. Both non-volatile and volatile key programming are supported using Stratix III devices. When using the design security feature, a 256-bit security key is stored in the Stratix III device. To successfully configure a Stratix III device that has the design security feature enabled, the device must be configured with a configuration file that was encrypted using the same 256-bit security key. Non-volatile key programming does not require any external devices, such as a battery backup, for storage. However, for certain applications, you can store the security keys in volatile memory in the Stratix III device. An external battery is needed for this volatile key storage.

When using a serial configuration scheme such as PS or fast AS, configuration time is the same whether or not the design security feature is enabled. If the FPP scheme is used with the design security or decompression feature, a ×4 DCLK is required. This results in a slower configuration time when compared to the configuration time of a Stratix III device that has neither the design security nor the decompression feature enabled.

For more information about this feature, refer to the *Design Security in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Stratix III devices have dedicated JTAG pins that always function as JTAG pins. Not only can you perform JTAG testing on Stratix III devices before and after, but also during configuration. While other device families do not support JTAG testing during configuration, Stratix III devices support the bypass, id code, and sample instructions during configuration without interrupting configuration. All other JTAG instructions may only be issued by first interrupting configuration and reprogramming I/O pins using the CONFIG_IO instruction.

The CONFIG_IO instruction allows I/O buffers to be configured by using the JTAG port and when issued, interrupts configuration. This instruction allows you to perform board-level testing prior to configuring the Stratix III device or waiting for a configuration device to complete configuration. When configuration has been interrupted and JTAG testing is complete, you must reconfigure the part by using JTAG (PULSE_CONFIG instruction) or by pulsing nCONFIG low.

The chip-wide reset (DEV_CLRn) and chip-wide output enable (DEV_OE) pins on Stratix III devices do not affect JTAG boundary-scan or programming operations. Toggling these pins does not affect JTAG operations (other than the usual boundary-scan operation).

When designing a board for JTAG configuration of Stratix III devices, consider the dedicated configuration pins. Table 11–12 lists how these pins should be connected during JTAG configuration.

Table 11–12. Dedicated Configuration Pin Connections During JTAG Configuration

Signal	Description
nCE	On all Stratix III devices in the chain, nCE should be driven low by connecting it to ground, pulling it low by using a resistor, or driving it by some control circuitry. For devices that are also in multi-device FPP, AS, or PS configuration chains, the nCE pins should be connected to GND during JTAG configuration or JTAG configured in the same order as the configuration chain.
nCEO	On all Stratix III devices in the chain, you can leave nCEO floating or connected to the nCE of the next device.
MSEL	These pins must not be left floating. These pins support whichever non-JTAG configuration is used in production. If you only use JTAG configuration, tie these pins to ground.
nCONFIG	Driven high by connecting to V_{CCPGM}, pull up by using a resistor, or driven high by some control circuitry.
nSTATUS	Pull to V_{CCPGM} by using a 10-kΩ resistor. When configuring multiple devices in the same JTAG chain, each nSTATUS pin should be pulled up to V_{CCPGM} individually.
CONF_DONE	Pull to V_{CCPGM} by using a 10-kΩ resistor. When configuring multiple devices in the same JTAG chain, each CONF_DONE pin should be pulled up to V_{CCPGM} individually. CONF_DONE going high at the end of JTAG configuration indicates successful configuration.
DCLK	Should not be left floating. Drive low or high, whichever is more convenient on your board.

When programming a JTAG device chain, one JTAG-compatible header is connected to several devices. The number of devices in the JTAG chain is limited only by the drive capability of the download cable. When four or more devices are connected in a JTAG chain, Altera recommends buffering the TCK, TDI, and TMS pins with an on-board buffer.

JTAG-chain device programming is ideal when the system contains multiple devices, or when testing your system using JTAG BST circuitry. Figure 11–20 shows multi-device JTAG configuration.

Chapter Revision History

Table 11–17 lists the revision history for this chapter.

Table 11–17. Chapter Revision History (Part 1 of 2)

Date	Version	Changes Made
March 2011	2.0	■ Updated the "FPP Configuration Using a MAX II Device as an External Host", "Fast Active Serial Configuration (Serial Configuration Devices)", and "PS Configuration Using a MAX II Device as an External Host" ■ Updated Table 11–14.
July 2010	1.9	■ Updated Table 11–14. ■ Updated "FPP Configuration Using a MAX II Device as an External Host" on page 11–8.
March 2010	1.8	Updated for the Quartus II software version 9.1 SP2 release: ■ Added Figure 11–11. ■ Updated Figure 11–6, Figure 11–7, Figure 11–16, Figure 11–19, and Figure 11–20. ■ Updated "Estimating Active Serial Configuration Time" section. ■ Added Table 11–8. ■ Updated Table 11–8, Table 11–13, and Table 11–14. ■ Removed "Conclusion" section.
May 2009	1.7	■ Updated Table 11–1, Table 11–2, Table 11–5, Table 11–6, Table 11–9, and Table 11–13. ■ Updated Figure 11–6, Figure 11–16, Figure 11–17, Figure 11–18, Figure 11–19, and Figure 11–20. ■ Updated "PS Configuration Using a Microprocessor", "PS Configuration Using a Download Cable", and "JTAG Configuration" sections. ■ Removed Figure 11-12 Fast AS Configuration Timing. ■ Removed Table 11-8 Fast AS Timing Parameters for Stratix III devices.
February 2009	1.6	■ Updated Figure 11–6, Figure 11–7, Figure 11–12, and Figure 11–16. ■ Removed "Referenced Documents" section.
October 2008	1.5	■ Updated "FPP Configuration Using a MAX II Device as an External Host", "Fast Active Serial Configuration (Serial Configuration Devices)", "JTAG Configuration", "Power-On Reset Circuit", "PS Configuration Using a MAX II Device as an External Host", and "PS Configuration Using a Download Cable" sections. ■ Updated Table 11–13 and Table 11–14. ■ Updated New Document Format. ■ Updated (Note 3) to Figure 11–17. ■ Updated (Note 3) to Figure 11–18. ■ Updated (Note 3) to Figure 11–19. ■ Updated (Note 3) to Figure 11–20.

Table 12–2. Remote System Upgrade Registers (Part 2 of 2)

Register	Description
Update register	Contains data similar to that in the control register. However, it can only be updated by the factory configuration by shifting data into the shift register and issuing an update operation. When a reconfiguration cycle is triggered by the factory configuration, the control register is updated with the contents of the update register. During a capture in a factory configuration, this register is read into the shift register.
Status register	Written to by the remote system upgrade circuitry on every reconfiguration to record the cause of the reconfiguration. This information is used by the factory configuration to determine the appropriate action following a reconfiguration. During a capture cycle, this register is read into the shift register.

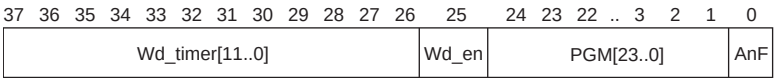
The remote system upgrade control and status registers are clocked by the 10-MHz internal oscillator (the same oscillator that controls the user watchdog timer). However, the remote system upgrade shift and update registers are clocked by the user clock input (RU_CLK).

Remote System Upgrade Control Register

The remote system upgrade control register stores the application configuration page address and user watchdog timer settings. The control register functionality depends on the remote system upgrade mode selection. In remote update mode, the control register page address bits are set to all zeros (24'b0 = 0×000000) at power up in order to load the factory configuration. A factory configuration in remote update mode has write access to this register.

The control register bit positions are shown in Figure 12–6 and defined in Table 12–3. In the figure, the numbers show the bit position of a setting within a register. For example, bit number 8 is the enable bit for the watchdog timer.

Figure 12–6. Remote System Upgrade Control Register



The application-not-factory (AnF) bit indicates whether the current configuration loaded in the Stratix III device is the factory configuration or an application configuration. This bit is set low by the remote system upgrade circuitry when an error condition causes a fall-back to the factory configuration. When the AnF bit is high, the control register access is limited to read operations. When the AnF bit is low, the register allows write operations and disables the watchdog timer.

In remote update mode, factory configuration design sets this bit high (1'b1) when updating the contents of the update register with the application page address and watchdog timer settings.

Table 12–3. Remote System Upgrade Control Register Contents (Part 1 of 2)

Control Register Bit	Remote System Upgrade Mode	Value *(2)*	Definition
AnF *(1)*	Remote update	1'b0	Application not factory
PGM[23..0]	Remote update	24'b0×000000	AS configuration start address (StAdd[23..0])

Security Against Reverse Engineering

Reverse engineering from an encrypted configuration file is very difficult and time consuming because the Stratix III configuration file formats are proprietary and the file contains million of bits which require specific decryption. Reverse engineering the Stratix III device is just as difficult because the device is manufactured on the most advanced 65-nm process technology.

Security Against Tampering

The non-volatile keys are one-time programmable. Once the tamper protection bit is set in the key programming file generated by the Quartus® II software, the Stratix III device can only be configured with configuration files encrypted with the same key.

For more information about why this feature is secured, refer to the *Design Security in Stratix III Devices white paper*.

AES Decryption Block

The main purpose of the AES decryption block is to decrypt the configuration bitstream prior to entering data decompression or configuration.

Prior to receiving encrypted data, you must enter and store the 256-bit security key in the device. You can choose between a non-volatile security key and a volatile security key with battery backup.

The security key is scrambled prior to storing it in key storage in order to make it more difficult for anyone to retrieve the stored key using de-capsulation of the device.

Flexible Security Key Storage

Stratix III devices support two types of security key programming: volatile and non-volatile. Table 14–1 shows the differences between volatile keys and non-volatile keys.

Table 14–1. Security Keys Options

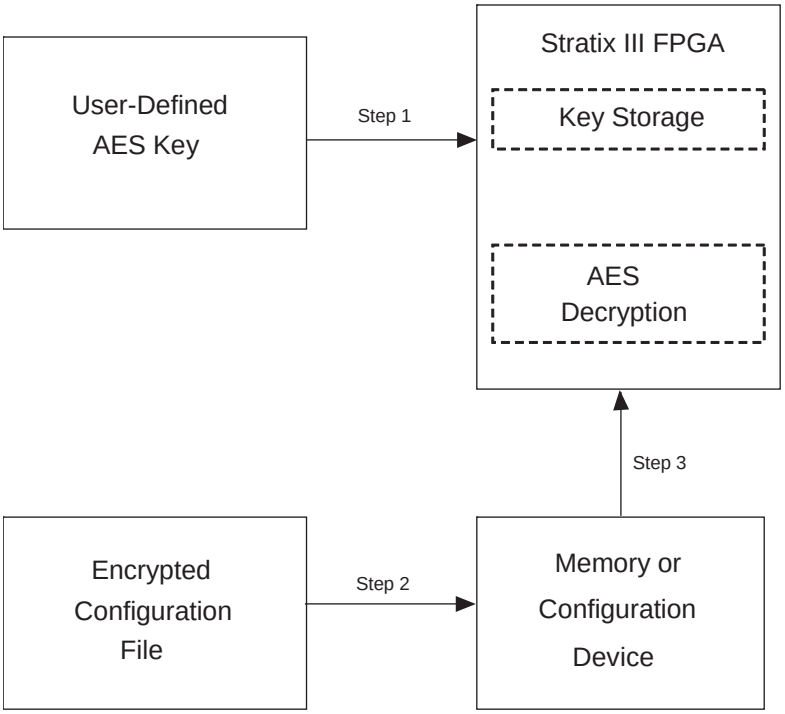
Options	Volatile Key	Non-Volatile Key
Key programmability	Reprogrammable and erasable	One-time programmable
External battery	Required	Not required
Key programming method *(1)*	On-board	On and off board
Design protection	Secure against copying and reverse engineering	Secure against copying and reverse engineering. Tamper resistant if tamper protection bit is set.

Note to Table 14–1:

(1) Key programming is carried out using JTAG interface.

You can program the non-volatile key to the Stratix III device without an external battery. Also, there are no additional requirements to any of the Stratix III power supply inputs.

Figure 14–1. Design Security *(Note 1)*



Note to Figure 14–1:

(1) Step 1, Step 2, and Step 3 correspond to the procedure detailed in the "Stratix III Design Security Solution" section.

Security Modes Available

There are several security modes available on the Stratix III device, which are described as follows:

Volatile Key

Secure operation with volatile key programmed and required external battery—this mode accepts both encrypted and unencrypted configuration bitstreams. Use the unencrypted configuration bitstream support for board-level testing only.

Non-Volatile Key

Secure operation with one time programmable (OTP) security key programmed—this mode accepts both encrypted and unencrypted configuration bitstreams. Use the unencrypted configuration bitstream support for board-level testing only.

Non-Volatile Key with Tamper Protection Bit Set

Secure operation in tamper resistant mode with OTP security key programmed—only encrypted configuration bitstreams are allowed to configure the device.
Tamper protection disables JTAG configuration with unencrypted configuration bitstream.

Figure 15–1. Error Detection Block Diagram

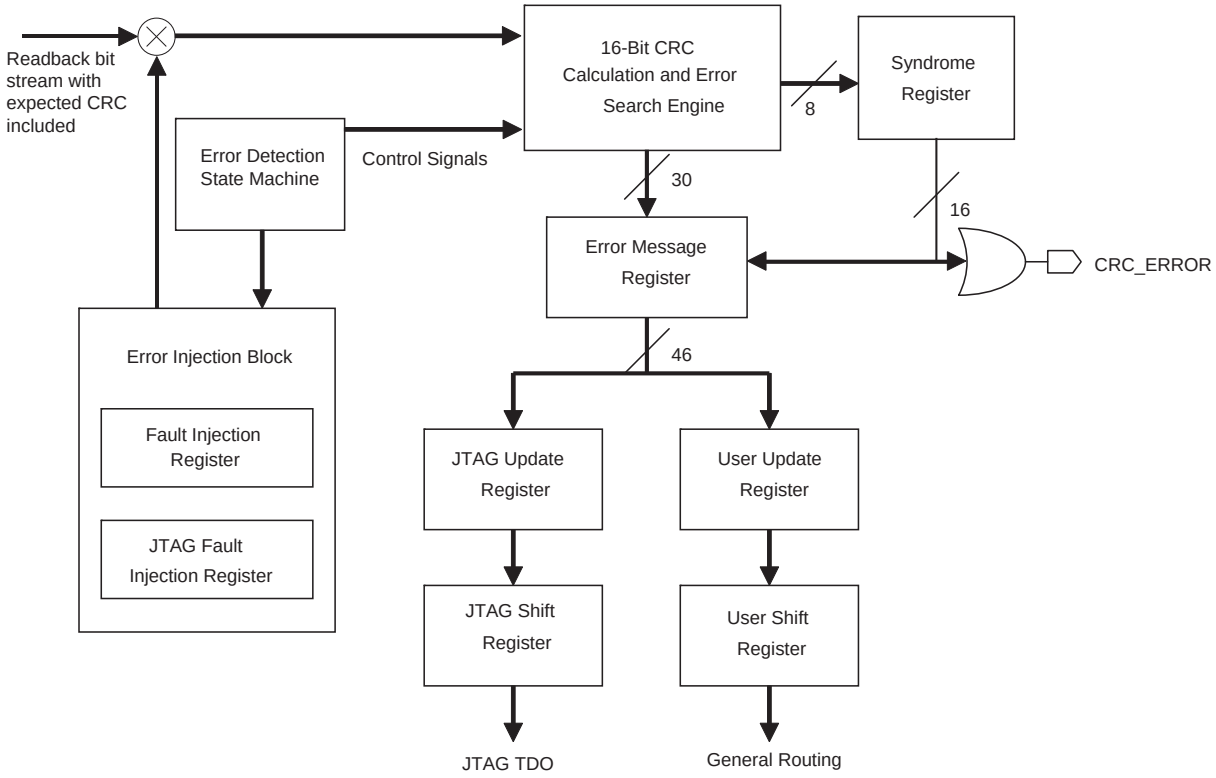


Table 15–5 lists the registers shown in Figure 15–1.

Table 15–4. Error Detection Registers (Part 1 of 2)

Register	Description
Syndrome Register	This register contains the CRC signature of the current frame through the error detection verification cycle. The CRC_ERROR signal is derived from the contents of this register.
Error Message Register	This 46-bit register contains information about the error type, location of the error, and the actual syndrome. The types of errors and location reported are single and double adjacent bit errors. The location bits for other types of errors are not identified by the Error Message Register. You can shift out the content of the register through the JTAG SHIFT_EDERROR_REG instruction or to the core through the core interface.
JTAG Update Register	This register is automatically updated with the contents of the Error Message Register one cycle after the 46-bit register content is validated. It includes a clock enable which needs to be asserted prior to being sampled into the JTAG Shift Register. This requirement ensures that the JTAG Update Register is not being written into by the contents of the Error Message Register at exactly the same time that the JTAG Shift Register is reading its contents.
User Update Register	This register is automatically updated with the contents of the Error Message Register, one cycle after the 46-bit register content is validated. It includes a clock enable which needs to be asserted prior to being sampled into the User Shift Register. This requirement ensures that the User Update Register is not being written into by the contents of the Error Message Register at exactly the same time that the User Shift Register is reading its contents.

16. Programmable Power and Temperature-Sensing Diodes in Stratix III Devices

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Introduction

The total power of an FPGA includes static power and dynamic power. Static power is the power consumed by the FPGA when it is programmed but no clocks are operating. Dynamic power is comprised of switching power when the device is configured and running. Dynamic power is calculated with the Equation 16–1:

Equation 16–1. Dynamic Power Equation

$$P = \frac{1}{2} CV^2 \times \text{frequency} \times \text{toggle rate}$$

Equation 16–1 shows that the frequency and toggle rate are design-dependent. However, voltage can be varied to lower dynamic power consumption by the square value of the voltage difference. Stratix® III devices minimize static and dynamic power with advanced process optimizations, selectable core voltage, and programmable power technology. These technologies enable Stratix III designs to optimally meet design-specific performance requirements with the lowest possible power.

The Quartus® II software optimizes all designs with Stratix III power technology to ensure performance is met at the lowest power consumption. This automatic process allows you to concentrate on the functionality of your design, instead of the power consumption of the design.

Power consumption also affects thermal management. Stratix III offers a temperature sensing diode (TSD), which you can use with external circuitry to monitor the device junction temperature for activities such as controlling air flow to the FPGA.

Stratix III Power Technology

The following section provides details about Stratix III selectable core voltage and programmable power technology.

Selectable Core Voltage

Altera offers a series of low-voltage Stratix products that have the ability to power the core logic of the device with either a 0.9-V or 1.1-V power supply. This power supply, called V_{CCL}, powers the logic array block (LAB), memory logic array block (MLAB), digital signal processing (DSP) blocks, TriMatrix™ memory blocks, clock networks, and routing lines. The periphery, consisting of the I/O registers and their routing connections are powered by V_{CC} with a 1.1-V power supply. You can use the same 1.1-V power supply if you want both V_{CC} and V_{CCL} to be 1.1 V.

Thermal Resistance

For Stratix III devices thermal resistance specifications, refer to the *Stratix Series Device Thermal Resistance Data Sheet*.

Package Outlines

You can download Stratix III device package outlines from the *Device Packaging Specifications* web page.

Chapter Revision History

Table 17–2 lists the revision history for this chapter.

Table 17–2. Chapter Revision History

Date	Version	Changes Made
March 2010	1.7	Updated for the Quartus II software version 9.1 SP2 release: ■ Updated Table 17–1. ■ Minor text edits.
February 2009	1.6	Removed "Referenced Documents" section.
October 2008	1.5	Updated New Document Format.
May 2008	1.4	Updated "Package Outlines" section hyperlink.
November 2007	1.3	Updated Table 17–1.
October 2007	1.2	■ Added new section "Referenced Documents". ■ Added live links for references.
May 2007	1.1	Removed thermal resistance and package outline information and replaced with links referencing this information.
November 2006	1.0	Initial Release.