Table of Contents

1 Summary of Features 4

2 General Device Information 7
2.1 Introduction 7
2.2 Pin Configuration and Definition 8

3 Functional Description 19
3.1 Memory Subsystem and Organization 20
3.2 External Bus Controller 22
3.3 Central Processing Unit (CPU) 24
3.4 Interrupt System 26
3.5 On-Chip Debug Support (OCDS) 31
3.6 Capture/Compare Units (CAPCOM1/2) 32
3.7 General Purpose Timer (GPT12E) Unit 35
3.8 Real Time Clock 39
3.9 A/D Converter 41
3.10 Asynchronous/Synchronous Serial Interfaces (ASC0/ASC1) 42
3.11 High Speed Synchronous Serial Channels (SSC0/SSC1) 43
3.12 Serial Data Link Module (SDLM) 44
3.13 TwinCAN Module 45
3.14 IIC Bus Module 46
3.15 Watchdog Timer 47
3.16 Clock Generation 48
3.17 Parallel Ports 48
3.18 Power Management 50

The EBC also controls accesses to resources connected to the on-chip LXBus. The LXBus is an internal representation of the external bus and allows accessing integrated peripherals and modules in the same way as external components.

The TwinCAN module is connected and accessed via the LXBus.

3.2 External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes[1)], which are as follows:

- 16 … 24-bit Addresses, 16-bit Data, Demultiplexed
- 16 … 24-bit Addresses, 16-bit Data, Multiplexed
- 16 … 24-bit Addresses, 8-bit Data, Multiplexed
- 16 … 24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output. The high order address (segment) lines use Port 4. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes … 64 Kbytes. This is required when interface lines are assigned to Port 4.

Up to 5 external $\overline{CS}$ signals (4 windows plus default) can be generated in order to save external glue logic. External modules can directly be connected to the common address/data bus and their individual select lines.

Access to very slow memories or modules with varying access times is supported via a particular ‘Ready’ function. The active level of the control input signal is selectable.

A $\overline{HOLD}$/$\overline{HLDA}$ protocol is available for bus arbitration and allows the sharing of external resources with other bus masters. The bus arbitration is enabled by software. After enabling, pins P6.7 … P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{HLDA}$ pin is an output. In Slave Mode pin $\overline{HLDA}$ is switched to input. This allows the direct connection of the slave controller to another master controller without glue logic.

Important timing characteristics of the external bus interface have been made programmable (via registers TCONCSx/FCONCSx) to allow the user the adaption of a wide range of different types of memories and external peripherals.

In addition, up to 4 independent address windows may be defined (via registers ADDRSELx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these 4 address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

The external bus timing is related to the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

1) Bus modes are switched dynamically if several address windows with different mode settings are used.

so-called General Purpose Registers (GPRs).
The upper 256 bytes of the DPRAM are directly bitaddressable. When used by a GPR, any location in the DPRAM is bitaddressable.

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XC166 Family. Therefore, they should either not be accessed, or written with zeros, to ensure upward compatibility.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 12 Mbytes (approximately, see **Table 3**) of external RAM and/or ROM can be connected to the microcontroller. The External Bus Interface also provides access to external peripherals.

Table 3 XC161 Memory Map[1)]

Address Area	Start Loc.	End Loc.	Area Size[2)]	Notes
Flash register space	$FF'F000_H$	$FF'FFFF_H$	4 Kbytes	[3)]
Reserved (Access trap)	$F8'0000_H$	$FF'EFFF_H$	< 0.5 Mbytes	Minus Flash registers
Reserved for PSRAM	$E0'0800_H$	$F7'FFFF_H$	< 1.5 Mbytes	Minus PSRAM
Program SRAM	$E0'0000_H$	$E0'07FF_H$	2 Kbytes	Maximum
Reserved for program memory	$C2'0000_H$	$DF'FFFF_H$	< 2 Mbytes	Minus Flash
Program Flash	$C0'0000_H$	$C1'FFFF_H$	128 Kbytes	–
Reserved	$BF'0000_H$	$BF'FFFF_H$	64 Kbytes	–
External memory area	$40'0000_H$	$BE'FFFF_H$	< 8 Mbytes	Minus reserved segment
External IO area[4)]	$20'0800_H$	$3F'FFFF_H$	< 2 Mbytes	Minus TwinCAN
TwinCAN registers	$20'0000_H$	$20'07FF_H$	2 Kbytes	–
External memory area	$01'0000_H$	$1F'FFFF_H$	< 2 Mbytes	Minus segment 0
Data RAMs and SFRs	$00'8000_H$	$00'FFFF_H$	32 Kbytes	Partly used
External memory area	$00'0000_H$	$00'7FFF_H$	32 Kbytes	–

1) Accesses to the shaded areas generate external bus accesses.
2) The areas marked with “<” are slightly smaller than indicated, see column “Notes”.
3) Not defined register locations return a trap code.
4) Several pipeline optimizations are not active within the external IO area. This is necessary to control external peripherals properly.