Infineon Technologies - XC161CJ16F40FBBFXUMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	C166SV2
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, I²C, SLDM, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	99
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	PG-TQFP-144-7
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc161cj16f40fbbfxuma1

2.2 Pin Configuration and Definition

The pins of the XC161 are described in detail in **Table 2**, including all their alternate functions. **Figure 2** summarizes all pins in a condensed way, showing their location on the 4 sides of the package. E*) and C*) mark pins to be used as alternate external interrupt inputs, C*) marks pins that can have CAN/SDLM interface lines assigned to them.

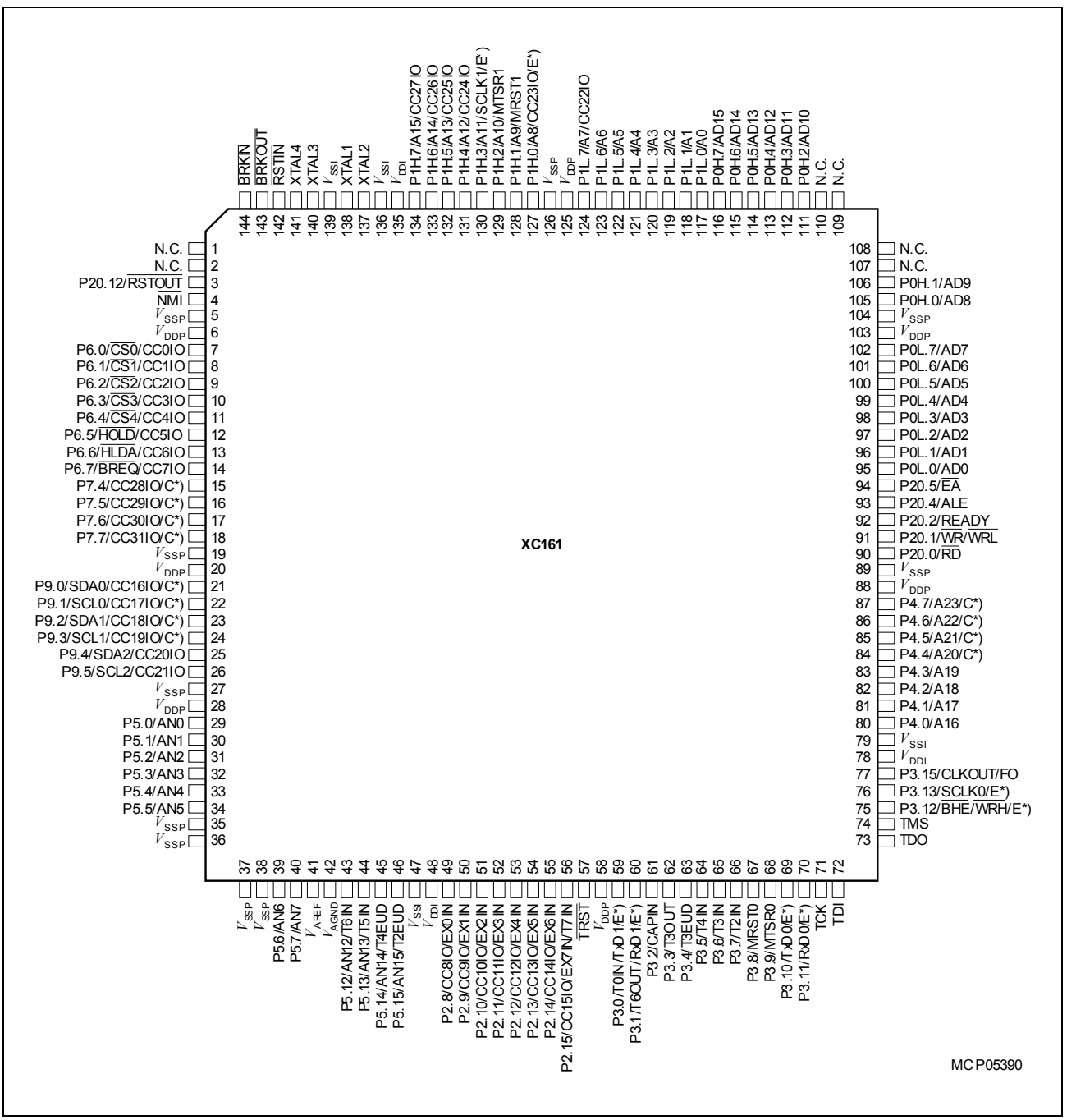

Figure 2 Pin Configuration (top view)

Table 2 Pin Definitions and Functions

Sym-bol	Pin Num.	Input Outp.	Function
P20.12	3	IO	For details, please refer to the description of **P20**.
NMI	4	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the NMI pin must be low in order to force the XC161 into power down mode. If NMI is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin NMI should be pulled high externally.
P6		IO	Port 6 is an 8-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 6 is selectable (standard or special). The Port 6 pins also serve for alternate functions:
P6.0	7	O	CS0 Chip Select 0 Output,
		I/O	CC0IO CAPCOM1: CC0 Capture Inp./Compare Output
P6.1	8	O	CS1 Chip Select 1 Output,
		I/O	CC1IO CAPCOM1: CC1 Capture Inp./Compare Output
P6.2	9	O	CS2 Chip Select 2 Output,
		I/O	CC2IO CAPCOM1: CC2 Capture Inp./Compare Output
P6.3	10	O	CS3 Chip Select 3 Output,
		I/O	CC3IO CAPCOM1: CC3 Capture Inp./Compare Output
P6.4	11	O	CS4 Chip Select 4 Output,
		I/O	CC4IO CAPCOM1: CC4 Capture Inp./Compare Output
P6.5	12	I	HOLD External Master Hold Request Input,
		I/O	CC5IO CAPCOM1: CC5 Capture Inp./Compare Output
P6.6	13	O/I	HLDA Hold Acknowledge Output (master mode) or Input (slave mode),
		I/O	CC6IO CAPCOM1: CC6 Capture Inp./Compare Output
P6.7	14	O	BREQ Bus Request Output,
		I/O	CC7IO CAPCOM1: CC7 Capture Inp./Compare Output

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
P9		IO	Port 9 is a 6-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 9 is selectable (standard or special). The following Port 9 pins also serve for alternate functions:[1)]
P9.0	21	I/O	CC16IO CAPCOM2: CC16 Capture Inp./Compare Outp.,
		I	CAN2_RxD CAN Node 2 Receive Data Input,
		I/O	SDA0 IIC Bus Data Line 0
P9.1	22	I/O	CC17IO CAPCOM2: CC17 Capture Inp./Compare Outp.,
		O	CAN2_TxD CAN Node 2 Transmit Data Output,
		I/O	SCL0 IIC Bus Clock Line 0
P9.2	23	I/O	CC18IO CAPCOM2: CC18 Capture Inp./Compare Outp.,
		I	CAN1_RxD CAN Node 1 Receive Data Input,
		O	SDL_TxD SDLM Transmit Data Output,
		I/O	SDA1 IIC Bus Data Line 1
P9.3	24	I/O	CC19IO CAPCOM2: CC19 Capture Inp./Compare Outp.,
		O	CAN1_TxD CAN Node 1 Transmit Data Output,
		I	SDL_RxD SDLM Receive Data Input,
		I/O	SCL1 IIC Bus Clock Line 1
P9.4	25	I/O	CC20IO CAPCOM2: CC20 Capture Inp./Compare Outp.,
		I/O	SDA2 IIC Bus Data Line 2
P9.5	26	I/O	CC21IO CAPCOM2: CC21 Capture Inp./Compare Outp.,
		I/O	SCL2 IIC Bus Clock Line 2
P5		I	Port 5 is a 12-bit input-only port. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:
P5.0	29	I	AN0
P5.1	30	I	AN1
P5.2	31	I	AN2
P5.3	32	I	AN3
P5.4	33	I	AN4
P5.5	34	I	AN5
P5.6	39	I	AN6
P5.7	40	I	AN7
P5.12	43	I	AN12, T6IN GPT2 Timer T6 Count/Gate Input
P5.13	44	I	AN13, T5IN GPT2 Timer T5 Count/Gate Input
P5.14	45	I	AN14, T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.15	46	I	AN15, T2EUD GPT1 Timer T2 Ext. Up/Down Ctrl. Inp.

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function	
P3		IO	Port 3 is a 15-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 3 is selectable (standard or special). The following Port 3 pins also serve for alternate functions:	
P3.0	59	I	T0IN	CAPCOM1 Timer T0 Count Input,
		O	TxD1	ASC1 Clock/Data Output (Async./Sync),
		I	EX1IN	Fast External Interrupt 1 Input (alternate pin B)
P3.1	60	O	T6OUT	GPT2 Timer T6 Toggle Latch Output,
		I/O	RxD1	ASC1 Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX1IN	Fast External Interrupt 1 Input (alternate pin A)
P3.2	61	I	CAPIN	GPT2 Register CAPREL Capture Input
P3.3	62	O	T3OUT	GPT1 Timer T3 Toggle Latch Output
P3.4	63	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input
P3.5	64	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture Inp
P3.6	65	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	66	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/Capture Inp
P3.8	67	I/O	MRST0	SSC0 Master-Receive/Slave-Transmit In/Out.
P3.9	68	I/O	MTSR0	SSC0 Master-Transmit/Slave-Receive Out/In.
P3.10	69	O	TxD0	ASC0 Clock/Data Output (Async./Sync.),
		I	EX2IN	Fast External Interrupt 2 Input (alternate pin B)
P3.11	70	I/O	RxD0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX2IN	Fast External Interrupt 2 Input (alternate pin A)
P3.12	75	O	$\overline{\text{BHE}}$	External Memory High Byte Enable Signal,
		O	$\overline{\text{WRH}}$	External Memory High Byte Write Strobe,
		I	EX3IN	Fast External Interrupt 3 Input (alternate pin B)
P3.13	76	I/O	SCLK0	SSC0 Master Clock Output/Slave Clock Input.,
		I	EX3IN	Fast External Interrupt 3 Input (alternate pin A)
P3.15	77	O	CLKOUT	Master Clock Output,
		O	FOUT	Programmable Frequency Output
TCK	71	I	Debug System: JTAG Clock Input	
TDI	72	I	Debug System: JTAG Data In	
TDO	73	O	Debug System: JTAG Data Out	
TMS	74	I	Debug System: JTAG Test Mode Selection	

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
PORT0 P0L.0 - P0L.7, P0H.0, P0H.1, P0H.2 - P0H.7	 95 - 102, 105, 106, 111 - 116	IO	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. Each pin can be programmed for input (output driver in high-impedance state) or output. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes:** 8-bit data bus: P0H = I/O, P0L = D7 - D0 16-bit data bus: P0H = D15 - D8, P0L = D7 - D0 **Multiplexed bus modes:** 8-bit data bus: P0H = A15 - A8, P0L = AD7 - AD0 16-bit data bus: P0H = AD15 - AD8, P0L = AD7 - AD0 *Note: At the end of an external reset ($\overline{EA}$ = 0) PORT0 also may input configuration values.*
PORT1 P1L.0 - P1L.6 P1L.7 P1H.0 P1H.1 P1H.2 P1H.3 P1H.4 P1H.5 P1H.6 P1H.7	 117 - 123 124 127 128 129 130 131 132 133 134	IO O I/O I/O I I/O I/O I/O I I/O I/O I/O I/O	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. Each pin can be programmed for input (output driver in high-impedance state) or output. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes (also after switching from a demultiplexed to a multiplexed bus mode). The following PORT1 pins also serve for alt. functions: (A0-6) Address output only CC22IO CAPCOM2: CC22 Capture Inp./Compare Outp. CC23IO CAPCOM2: CC23 Capture Inp./Compare Outp., EX0IN Fast External Interrupt 0 Input (alternate pin B) MRST1 SSC1 Master-Receive/Slave-Transmit In/Outp. MTSR1 SSC1 Master-Transmit/Slave-Receive Out/Inp. SCLK1 SSC1 Master Clock Output/Slave Clock Input, EX0IN Fast External Interrupt 0 Input (alternate pin A) CC24IO CAPCOM2: CC24 Capture Inp./Compare Outp. CC25IO CAPCOM2: CC25 Capture Inp./Compare Outp. CC26IO CAPCOM2: CC26 Capture Inp./Compare Outp. CC27IO CAPCOM2: CC27 Capture Inp./Compare Outp.

Table 4 XC161 Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
CAPCOM Register 29	CC2_CC29IC	xx'0110$_H$	44$_H$ / 68$_D$
CAPCOM Register 30	CC2_CC30IC	xx'0114$_H$	45$_H$ / 69$_D$
CAPCOM Register 31	CC2_CC31IC	xx'0118$_H$	46$_H$ / 70$_D$
CAPCOM Timer 0	CC1_T0IC	xx'0080$_H$	20$_H$ / 32$_D$
CAPCOM Timer 1	CC1_T1IC	xx'0084$_H$	21$_H$ / 33$_D$
CAPCOM Timer 7	CC2_T7IC	xx'00F4$_H$	3D$_H$ / 61$_D$
CAPCOM Timer 8	CC2_T8IC	xx'00F8$_H$	3E$_H$ / 62$_D$
GPT1 Timer 2	GPT12E_T2IC	xx'0088$_H$	22$_H$ / 34$_D$
GPT1 Timer 3	GPT12E_T3IC	xx'008C$_H$	23$_H$ / 35$_D$
GPT1 Timer 4	GPT12E_T4IC	xx'0090$_H$	24$_H$ / 36$_D$
GPT2 Timer 5	GPT12E_T5IC	xx'0094$_H$	25$_H$ / 37$_D$
GPT2 Timer 6	GPT12E_T6IC	xx'0098$_H$	26$_H$ / 38$_D$
GPT2 CAPREL Register	GPT12E_CRIC	xx'009C$_H$	27$_H$ / 39$_D$
A/D Conversion Complete	ADC_CIC	xx'00A0$_H$	28$_H$ / 40$_D$
A/D Overrun Error	ADC_EIC	xx'00A4$_H$	29$_H$ / 41$_D$
ASC0 Transmit	ASC0_TIC	xx'00A8$_H$	2A$_H$ / 42$_D$
ASC0 Transmit Buffer	ASC0_TBIC	xx'011C$_H$	47$_H$ / 71$_D$
ASC0 Receive	ASC0_RIC	xx'00AC$_H$	2B$_H$ / 43$_D$
ASC0 Error	ASC0_EIC	xx'00B0$_H$	2C$_H$ / 44$_D$
ASC0 Autobaud	ASC0_ABIC	xx'017C$_H$	5F$_H$ / 95$_D$
SSC0 Transmit	SSC0_TIC	xx'00B4$_H$	2D$_H$ / 45$_D$
SSC0 Receive	SSC0_RIC	xx'00B8$_H$	2E$_H$ / 46$_D$
SSC0 Error	SSC0_EIC	xx'00BC$_H$	2F$_H$ / 47$_D$
IIC Data Transfer Event	IIC_DTIC	xx'0100$_H$	40$_H$ / 64$_D$
IIC Protocol Event	IIC_PEIC	xx'0104$_H$	41$_H$ / 65$_D$
PLL/OWD	PLLIC	xx'010C$_H$	43$_H$ / 67$_D$
ASC1 Transmit	ASC1_TIC	xx'0120$_H$	48$_H$ / 72$_D$
ASC1 Transmit Buffer	ASC1_TBIC	xx'0178$_H$	5E$_H$ / 94$_D$
ASC1 Receive	ASC1_RIC	xx'0124$_H$	49$_H$ / 73$_D$
ASC1 Error	ASC1_EIC	xx'0128$_H$	4A$_H$ / 74$_D$

3.6 Capture/Compare Units (CAPCOM1/2)

The CAPCOM units support generation and control of timing sequences on up to 32 channels with a maximum resolution of 1 system clock cycle (8 cycles in staggered mode). The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Four 16-bit timers (T0/T1, T7/T8) with reload registers provide two independent time bases for each capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to the application specific requirements. In addition, external count inputs for CAPCOM timers T0 and T7 allow event scheduling for the capture/compare registers relative to external events.

Both of the two capture/compare register arrays contain 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1 (T7 or T8, respectively), and programmed for capture or compare function.
All registers of each module have each one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

Table 6 Compare Modes (CAPCOM1/2)

Compare Modes	Function
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated
Mode 3	Pin set ‘1’ on match; pin reset ‘0’ on compare timer overflow; only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; pin toggles on each compare match; several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; can be used with any compare mode

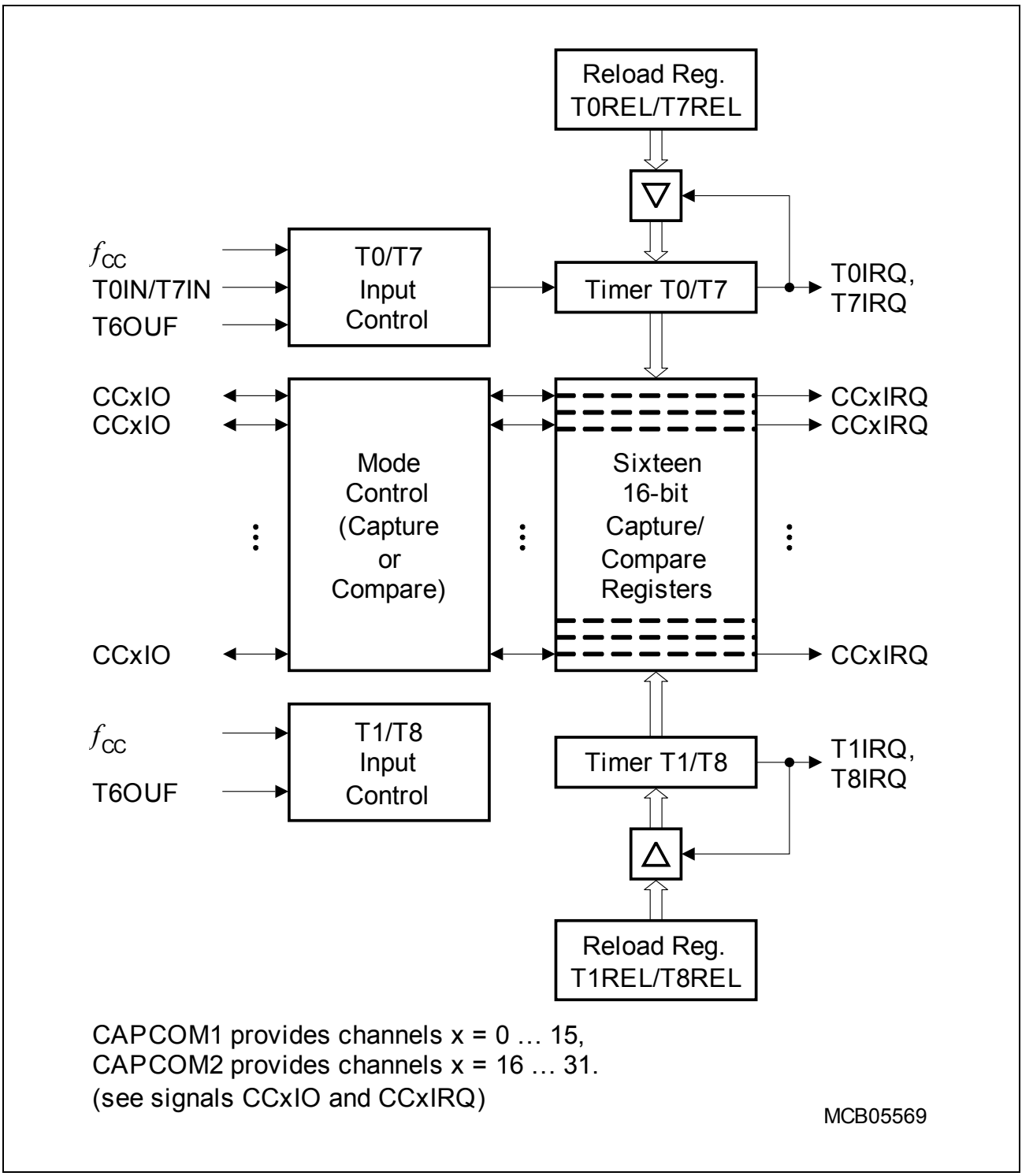

Figure 5 CAPCOM1/2 Unit Block Diagram

3.7 General Purpose Timer (GPT12E) Unit

The GPT12E unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.
Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM1/2 timers, and to cause a reload from the CAPREL register.

The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows the XC161 to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3's inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

3.8 Real Time Clock

The Real Time Clock (RTC) module of the XC161 is directly clocked via a separate clock driver either with the on-chip auxiliary oscillator frequency (f_{RTC} = f_{OSCa}) or with the prescaled on-chip main oscillator frequency (f_{RTC} = f_{OSCm}/32). It is therefore independent from the selected clock generation mode of the XC161.

The RTC basically consists of a chain of divider blocks:

- a selectable 8:1 divider (on - off)
- the reloadable 16-bit timer T14
- the 32-bit RTC timer block (accessible via registers RTCH and RTCL), made of:
  - a reloadable 10-bit timer
  - a reloadable 6-bit timer
  - a reloadable 6-bit timer
  - a reloadable 10-bit timer

All timers count up. Each timer can generate an interrupt request. All requests are combined to a common node request.

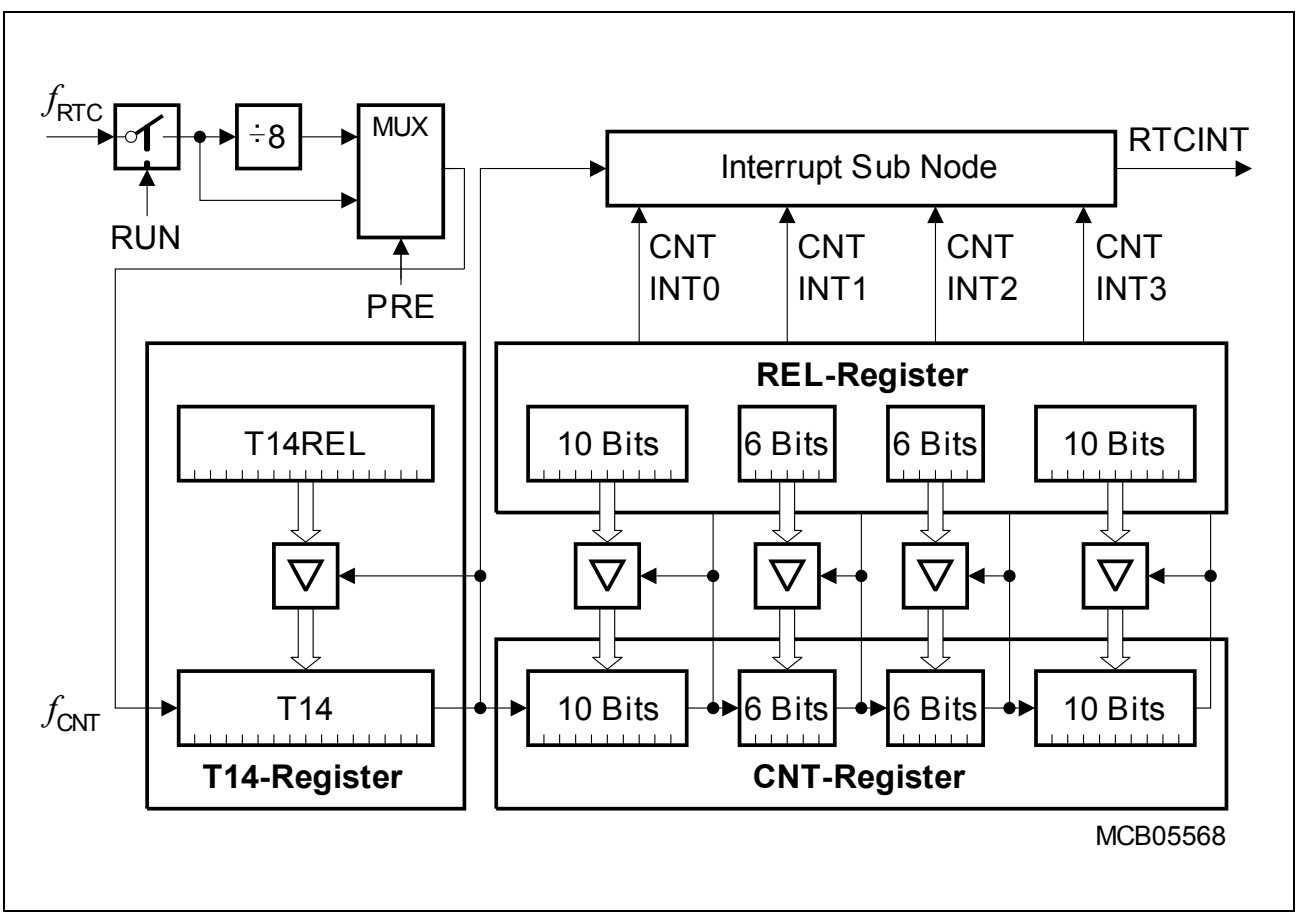

Figure 8 RTC Block Diagram

Note: The registers associated with the RTC are not affected by a reset in order to maintain the correct system time even when intermediate resets are executed.

3.11 High Speed Synchronous Serial Channels (SSC0/SSC1)

The High Speed Synchronous Serial Channels SSC0/SSC1 support full-duplex and half-duplex synchronous communication. It may be configured so it interfaces with serially linked peripheral components, full SPI functionality is supported.

A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling three separate interrupt vectors are provided.

The SSC transmits or receives characters of 2 … 16 bits length synchronously to a shift clock which can be generated by the SSC (master mode) or by an external master (slave mode). The SSC can start shifting with the LSB or with the MSB and allows the selection of shifting and latching clock edges as well as the clock polarity.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. Transmit error and receive error supervise the correct handling of the data buffer. Phase error and baudrate error detect incorrect serial data.

Summary of Features

- Master or Slave mode operation
- Full-duplex or Half-duplex transfers
- Baudrate generation from 20 Mbit/s to 305.18 bit/s (@ 40 MHz)
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: LSB-first or MSB-first
  - Programmable clock polarity: idle low or idle high
  - Programmable clock/data phase: data shift with leading or trailing clock edge
- Loop back option available for testing purposes
- Interrupt generation on transmitter buffer empty condition, receive buffer full condition, error condition (receive, phase, baudrate, transmit error)
- Three pin interface with flexible SSC pin configuration

3.13 TwinCAN Module

The integrated TwinCAN module handles the completely autonomous transmission and reception of CAN frames in accordance with the CAN specification V2.0 part B (active), i.e. the on-chip TwinCAN module can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Two Full-CAN nodes share the TwinCAN module's resources to optimize the CAN bus traffic handling and to minimize the CPU load. The module provides up to 32 message objects, which can be assigned to one of the CAN nodes and can be combined to FIFO-structures. Each object provides separate masks for acceptance filtering.

The flexible combination of Full-CAN functionality and FIFO architecture reduces the efforts to fulfill the real-time requirements of complex embedded control applications. Improved CAN bus monitoring functionality as well as the number of message objects permit precise and comfortable CAN bus traffic handling.

Gateway functionality allows automatic data exchange between two separate CAN bus systems, which reduces CPU load and improves the real time behavior of the entire system.

The bit timing for both CAN nodes is derived from the master clock and is programmable up to a data rate of 1 Mbit/s. Each CAN node uses two pins of Port 4, Port 7, or Port 9 to interface to an external bus transceiver. The interface pins are assigned via software.

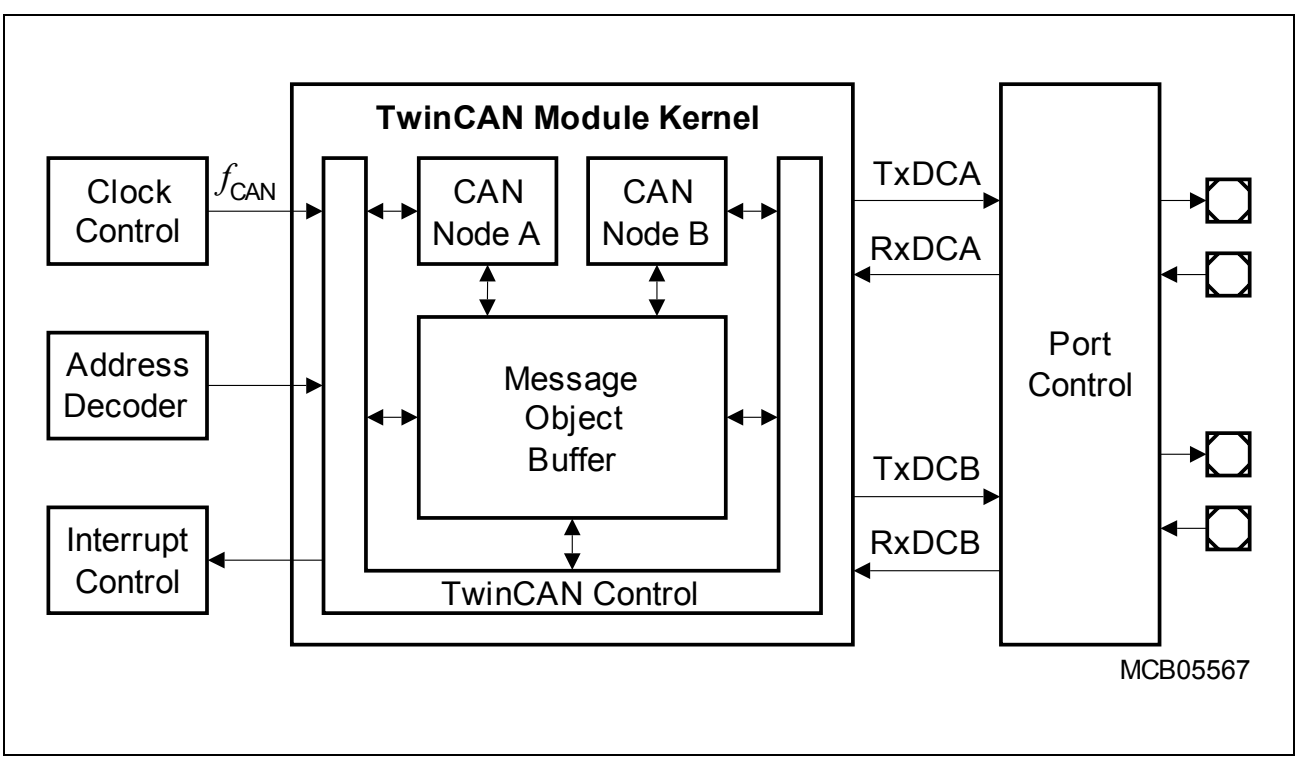

Figure 9 TwinCAN Module Block Diagram

Summary of Features

- CAN functionality according to CAN specification V2.0 B active
- Data transfer rate up to 1 Mbit/s
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality and Basic CAN functionality for each message object
- 32 flexible message objects
  - Assignment to one of the two CAN nodes
  - Configuration as transmit object or receive object
  - Concatenation to a 2-, 4-, 8-, 16-, or 32-message buffer with FIFO algorithm
  - Handling of frames with 11-bit or 29-bit identifiers
  - Individual programmable acceptance mask register for filtering for each object
  - Monitoring via a frame counter
  - Configuration for Remote Monitoring Mode
- Up to eight individually programmable interrupt nodes can be used
- CAN Analyzer Mode for bus monitoring is implemented

Note: When a CAN node has the interface lines assigned to Port 4, the segment address output on Port 4 must be limited. $\overline{CS}$ lines can be used to increase the total amount of addressable external memory.

3.14 IIC Bus Module

The integrated IIC Bus Module handles the transmission and reception of frames over the two-line IIC bus in accordance with the IIC Bus specification. The IIC Module can operate in slave mode, in master mode or in multi-master mode. It can receive and transmit data using 7-bit or 10-bit addressing. Up to 4 send/receive data bytes can be stored in the extended buffers.

Several physical interfaces (port pins) can be established under software control. Data can be transferred at speeds up to 400 kbit/s.

Two interrupt nodes dedicated to the IIC module allow efficient interrupt service and also support operation via PEC transfers.

Note: The port pins associated with the IIC interfaces must be switched to open drain mode, as required by the IIC specification.

Table 7 Summary of the XC161's Parallel Ports

Port	Control	Alternate Functions
PORT0	Pad drivers	Address/Data lines or data lines[1)]
PORT1	Pad drivers	Address lines[2)]
		Capture inputs or compare outputs, Serial interface lines
Port 2	Pad drivers, Open drain, Input threshold	Capture inputs or compare outputs, Timer control signal, Fast external interrupt inputs
Port 3	Pad drivers, Open drain, Input threshold	Timer control signals, serial interface lines, Optional bus control signal $\overline{BHE}$/$\overline{WRH}$, System clock output CLKOUT (or FOUT)
Port 4	Pad drivers, Open drain, Input threshold	Segment address lines[3)]
		CAN/SDLM interface lines[4)]
Port 5	–	Analog input channels to the A/D converter, Timer control signals
Port 6	Open drain, Input threshold	Capture inputs or compare outputs, Bus arbitration signals $\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$, Optional chip select signals
Port 7	Open drain, Input threshold	Capture inputs or compare outputs, CAN/SDLM interface lines[4)]
Port 9	Pad drivers, Open drain, Input threshold	Capture inputs or compare outputs
		CAN/SDLM interface lines[4)], IIC bus interface lines[4)]
Port 20	Pad drivers, Open drain	Bus control signals $\overline{RD}$, $\overline{WR}$/$\overline{WRL}$, READY, ALE, External access enable pin $\overline{EA}$, Reset indication output $\overline{RSTOUT}$

1) For multiplexed bus cycles.

2) For demultiplexed bus cycles.

3) For more than 64 Kbytes of external resources.

4) Can be assigned by software.

Table 12 Current Limits for Port Output Drivers

Port Output Driver Mode	Maximum Output Current (I_{OLmax}, $-I_{OHmax}$)[1]	Nominal Output Current (I_{OLnom}, $-I_{OHnom}$)
Strong driver	10 mA	2.5 mA
Medium driver	4.0 mA	1.0 mA
Weak driver	0.5 mA	0.1 mA

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time. For any group of 16 neighboring port output pins the total output current in each direction (ΣI_{OL} and $\Sigma -I_{OH}$) must remain below 50 mA.

Table 13 Power Consumption (Operating Conditions apply)

Parameter	Sym-bol	Limit Values		Unit	Test Condition
		Min.	Max.		
Power supply current (active) with all peripherals active	I_{DDI}	–	15 + 2.6 × f_{CPU}	mA	f_{CPU} in [MHz][1)2)]
Pad supply current	I_{DDP}	–	5	mA	[3)]
Idle mode supply current with all peripherals active	I_{IDX}	–	15 + 1.2 × f_{CPU}	mA	f_{CPU} in [MHz][2)]
Sleep and Power down mode supply current caused by leakage[4)]	I_{PDL}[5)]	–	128,000 × $e^{-\alpha}$	mA	V_{DDI} = V_{DDImax}[6)] T_J in [°C] α = 4670 / (273 + T_J)
Sleep and Power down mode supply current caused by leakage and the RTC running, clocked by the main oscillator[4)]	I_{PDM}[7)]	–	0.6 + 0.02 × f_{OSC} + I_{PDL}	mA	V_{DDI} = V_{DDImax} f_{OSC} in [MHz]
Sleep and Power down mode supply current caused by leakage and the RTC running, clocked by the auxiliary oscillator at 32 kHz[4)]	I_{PDA}	–	0.1 + I_{PDL}	mA	V_{DDI} = V_{DDImax}

1) During Flash programming or erase operations the supply current is increased by max. 5 mA.

2) The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 10**. These parameters are tested at V_{DDImax} and maximum CPU clock frequency with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

4.3 Analog/Digital Converter Parameters

Table 14 A/D Converter Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Analog reference supply	V_{AREF}	SR	4.5	V_{DDP} + 0.1	V	1)
Analog reference ground	V_{AGND}	SR	V_{SS} - 0.1	V_{SS} + 0.1	V	–
Analog input voltage range	V_{AIN}	SR	V_{AGND}	V_{AREF}	V	2)
Basic clock frequency	f_{BC}		0.5	20	MHz	3)
Conversion time for 10-bit result[4]	t_{C10P}	CC	$52 \times t_{BC} + t_S + 6 \times t_{SYS}$		–	Post-calibr. on
	t_{C10}	CC	$40 \times t_{BC} + t_S + 6 \times t_{SYS}$		–	Post-calibr. off
Conversion time for 8-bit result[4]	t_{C8P}	CC	$44 \times t_{BC} + t_S + 6 \times t_{SYS}$		–	Post-calibr. on
	t_{C8}	CC	$32 \times t_{BC} + t_S + 6 \times t_{SYS}$		–	Post-calibr. off
Calibration time after reset	t_{CAL}	CC	484	11,696	t_{BC}	5)
Total unadjusted error	TUE	CC	–	±2	LSB	1)
Total capacitance of an analog input	C_{AINT}	CC	–	15	pF	6)
Switched capacitance of an analog input	C_{AINS}	CC	–	10	pF	6)
Resistance of the analog input path	R_{AIN}	CC	–	2	kΩ	6)
Total capacitance of the reference input	C_{AREFT}	CC	–	20	pF	6)
Switched capacitance of the reference input	C_{AREFS}	CC	–	15	pF	6)
Resistance of the reference input path	R_{AREF}	CC	–	1	kΩ	6)

1) TUE is tested at $V_{AREF} = V_{DDP} + 0.1$ V, $V_{AGND} = 0$ V. It is verified by design for all other voltages within the defined voltage range.
If the analog reference supply voltage drops below 4.5 V (and $V_{AREF} \geq 4.0$ V) or exceeds the power supply voltage by up to 0.2 V (i.e. $V_{AREF} \leq V_{DDP} + 0.2$ V) the maximum TUE is increased to ±3 LSB. This range is not subject to production test.
The specified TUE is guaranteed only, if the absolute sum of input overload currents on Port 5 pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the respective period of time. During the reset calibration sequence the maximum TUE may be ±4 LSB.

2) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

Table 22 External Bus Cycle Timing (Operating Conditions apply)

Parameter	Symbol		Limits		Unit
			Min.	Max.	
Output valid delay for: RD, WR(L/H)	tc_{10}	CC	1	13	ns
Output valid delay for: BHE, ALE	tc_{11}	CC	-1	7	ns
Output valid delay for: A23 … A16, A15 … A0 (on PORT1)	tc_{12}	CC	1	16	ns
Output valid delay for: A15 … A0 (on PORT0)	tc_{13}	CC	3	16	ns
Output valid delay for: CS	tc_{14}	CC	1	14	ns
Output valid delay for: D15 … D0 (write data, MUX-mode)	tc_{15}	CC	3	17	ns
Output valid delay for: D15 … D0 (write data, DEMUX-mode)	tc_{16}	CC	3	17	ns
Output hold time for: RD, WR(L/H)	tc_{20}	CC	-3	3	ns
Output hold time for: BHE, ALE	tc_{21}	CC	0	8	ns
Output hold time for: A23 … A16, A15 … A0 (on PORT0)	tc_{23}	CC	1	13	ns
Output hold time for: CS	tc_{24}	CC	-3	3	ns
Output hold time for: D15 … D0 (write data)	tc_{25}	CC	1	13	ns
Input setup time for: READY, D15 … D0 (read data)	tc_{30}	SR	24	–	ns
Input hold time READY, D15 … D0 (read data)[1)]	tc_{31}	SR	-5	–	ns

1) Read data are latched with the same (internal) clock edge that triggers the address change and the rising edge of RD. Therefore address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can be removed after the rising edge of RD.

Note: The shaded parameters have been verified by characterization. They are not subject to production test.

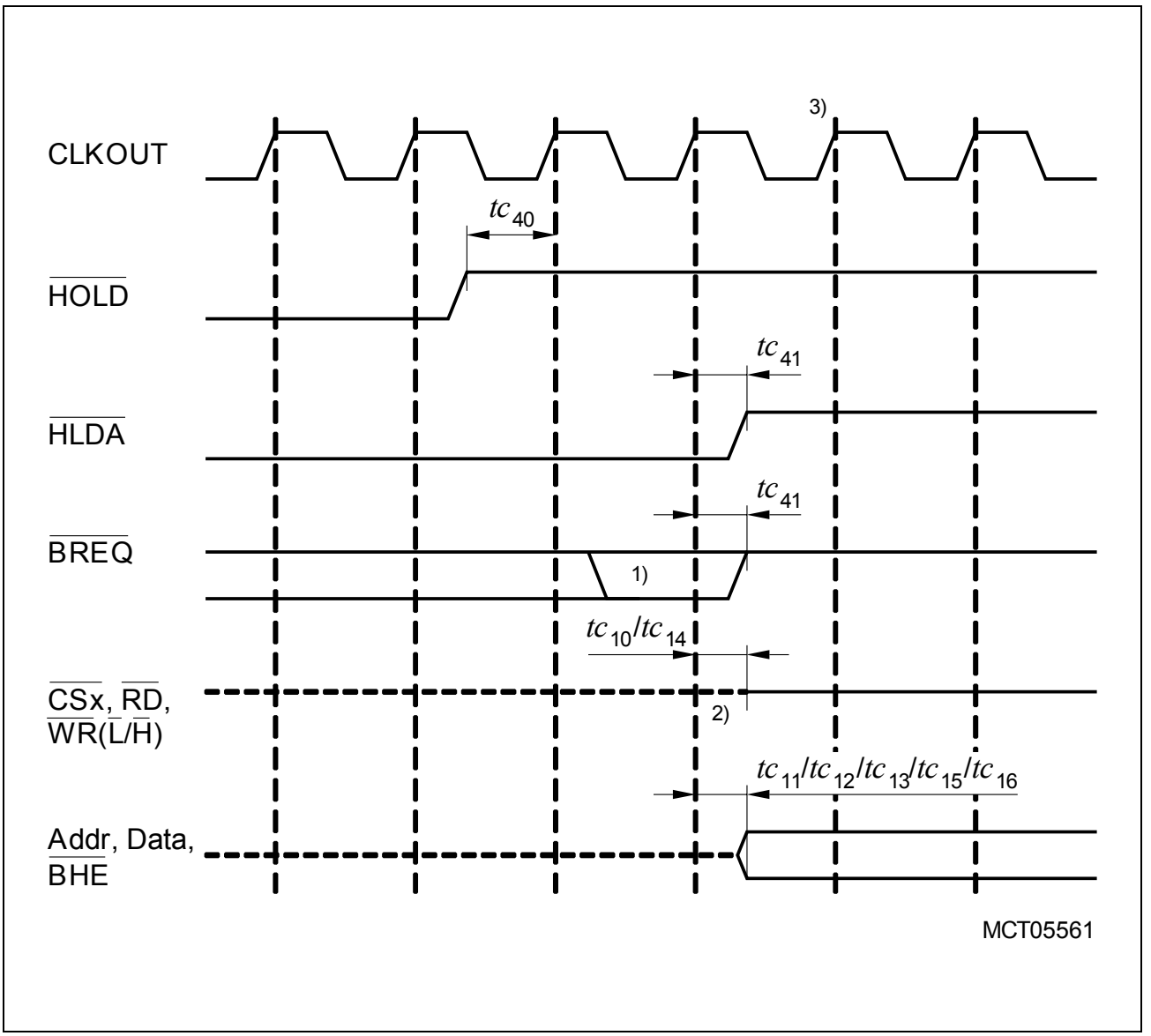

Figure 24 External Bus Arbitration, Regaining the Bus

Notes

1. *This is the last chance for $\overline{BREQ}$ to trigger the indicated regain-sequence. Even if $\overline{BREQ}$ is activated earlier, the regain-sequence is initiated by $\overline{HOLD}$ going high. Please note that $\overline{HOLD}$ may also be deactivated without the XC161 requesting the bus.*
2. *The control outputs will be resistive high (pull-up) before being driven inactive (ALE will be low).*
3. *The next XC161 driven bus cycle may start here.*

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