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Details

Product Status	Last Time Buy
Core Processor	C166SV2
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, I ² C, SLDM, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	99
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	PG-TQFP-144-7
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc161cj16f40fbbkxuma1

Summary of Features
Table 1 XC161 Derivative Synopsis

Derivative¹⁾	Temp. Range	Program Memory	On-Chip RAM	Interfaces
SAK-XC161CJ-16F40F, SAK-XC161CJ-16F20F	-40 °C to 125 °C	128 Kbytes Flash	2 Kbytes DPRAM, 4 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1, SDLM, IIC
SAF-XC161CJ-16F40F, SAF-XC161CJ-16F20F	-40 °C to 85 °C	128 Kbytes Flash	2 Kbytes DPRAM, 4 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1, SDLM, IIC

1) This Data Sheet is valid for devices starting with and including design step BB.

General Device Information
Table 2 Pin Definitions and Functions (cont'd)

Sym- bol	Pin Num.	Input Outp.	Function
P3		IO	Port 3 is a 15-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 3 is selectable (standard or special). The following Port 3 pins also serve for alternate functions:
P3.0	59	I	T0IN CAPCOM1 Timer T0 Count Input,
		O	TxD1 ASC1 Clock/Data Output (Async./Sync),
		I	EX1IN Fast External Interrupt 1 Input (alternate pin B)
P3.1	60	O	T6OUT GPT2 Timer T6 Toggle Latch Output,
		I/O	RxD1 ASC1 Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX1IN Fast External Interrupt 1 Input (alternate pin A)
P3.2	61	I	CAPIN GPT2 Register CAPREL Capture Input
P3.3	62	O	T3OUT GPT1 Timer T3 Toggle Latch Output
P3.4	63	I	T3EUD GPT1 Timer T3 External Up/Down Control Input
P3.5	64	I	T4IN GPT1 Timer T4 Count/Gate/Reload/Capture Inp
P3.6	65	I	T3IN GPT1 Timer T3 Count/Gate Input
P3.7	66	I	T2IN GPT1 Timer T2 Count/Gate/Reload/Capture Inp
P3.8	67	I/O	MRST0 SSC0 Master-Receive/Slave-Transmit In/Out.
P3.9	68	I/O	MTSR0 SSC0 Master-Transmit/Slave-Receive Out/In.
P3.10	69	O	TxD0 ASC0 Clock/Data Output (Async./Sync.),
		I	EX2IN Fast External Interrupt 2 Input (alternate pin B)
P3.11	70	I/O	RxD0 ASC0 Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX2IN Fast External Interrupt 2 Input (alternate pin A)
P3.12	75	O	<u>BHE</u> External Memory High Byte Enable Signal,
		O	<u>WRH</u> External Memory High Byte Write Strobe,
		I	EX3IN Fast External Interrupt 3 Input (alternate pin B)
P3.13	76	I/O	SCLK0 SSC0 Master Clock Output/Slave Clock Input.,
		I	EX3IN Fast External Interrupt 3 Input (alternate pin A)
P3.15	77	O	CLKOUT Master Clock Output,
		O	FOUT Programmable Frequency Output
TCK	71	I	Debug System: JTAG Clock Input
TDI	72	I	Debug System: JTAG Data In
TDO	73	O	Debug System: JTAG Data Out
TMS	74	I	Debug System: JTAG Test Mode Selection

3 Functional Description

The architecture of the XC161 combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a very well-balanced way. In addition, the on-chip memory blocks allow the design of compact systems-on-silicon with maximum performance (computing, control, communication).

The on-chip memory blocks (program code-memory and SRAM, dual-port RAM, data SRAM) and the set of generic peripherals are connected to the CPU via separate buses. Another bus, the LXBus, connects additional on-chip resources as well as external resources (see [Figure 3](#)).

This bus structure enhances the overall system performance by enabling the concurrent operation of several subsystems of the XC161.

The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the XC161.

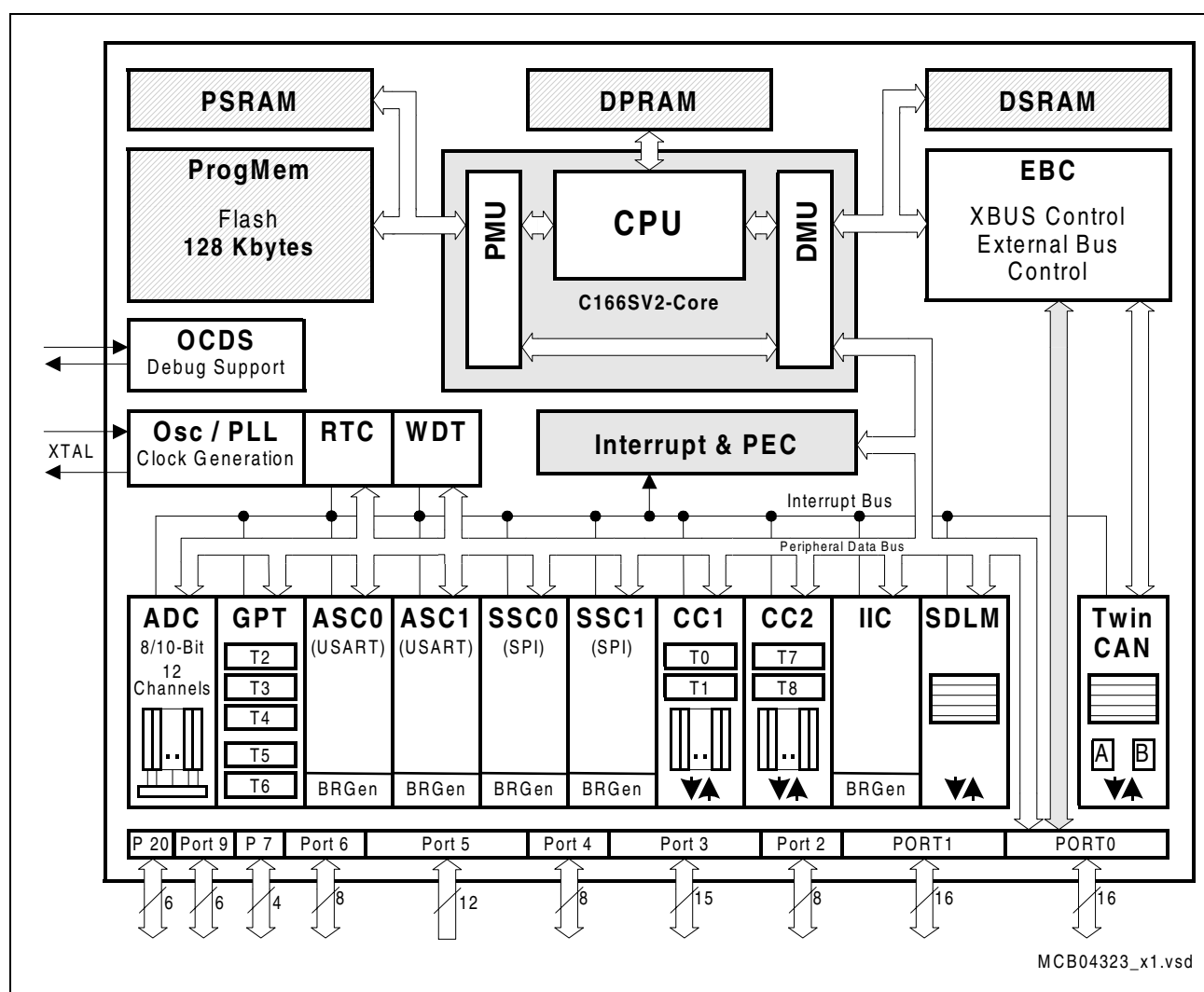


Figure 3 Block Diagram

3.3 Central Processing Unit (CPU)

The main core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply and divide unit, a bit-mask generator, and a barrel shifter.

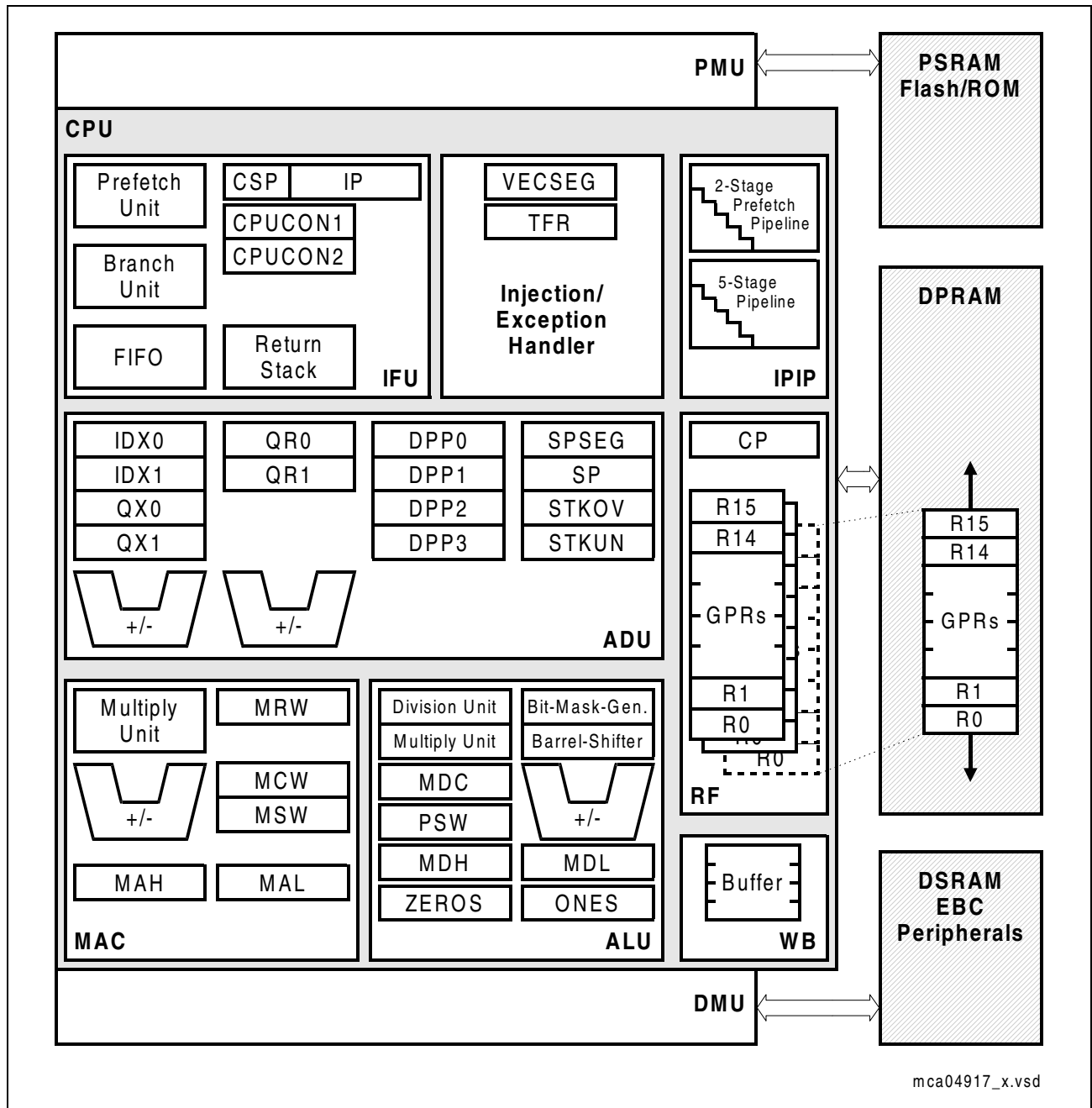


Figure 4 CPU Block Diagram

Based on these hardware provisions, most of the XC161's instructions can be executed in just one machine cycle which requires 25 ns at 40 MHz CPU clock. For example, shift

3.4 Interrupt System

With an interrupt response time of typically 8 CPU clocks (in case of internal program execution), the XC161 is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the XC161 supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source, or the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The XC161 has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt nodes. Via its related register, each node can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt nodes has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge, or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

Table 4 shows all of the possible XC161 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not assigned to peripherals (unassigned nodes), may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

Functional Description
Table 4 XC161 Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location¹⁾	Trap Number
CAPCOM Register 29	CC2_CC29IC	xx'0110 _H	44 _H / 68 _D
CAPCOM Register 30	CC2_CC30IC	xx'0114 _H	45 _H / 69 _D
CAPCOM Register 31	CC2_CC31IC	xx'0118 _H	46 _H / 70 _D
CAPCOM Timer 0	CC1_T0IC	xx'0080 _H	20 _H / 32 _D
CAPCOM Timer 1	CC1_T1IC	xx'0084 _H	21 _H / 33 _D
CAPCOM Timer 7	CC2_T7IC	xx'00F4 _H	3D _H / 61 _D
CAPCOM Timer 8	CC2_T8IC	xx'00F8 _H	3E _H / 62 _D
GPT1 Timer 2	GPT12E_T2IC	xx'0088 _H	22 _H / 34 _D
GPT1 Timer 3	GPT12E_T3IC	xx'008C _H	23 _H / 35 _D
GPT1 Timer 4	GPT12E_T4IC	xx'0090 _H	24 _H / 36 _D
GPT2 Timer 5	GPT12E_T5IC	xx'0094 _H	25 _H / 37 _D
GPT2 Timer 6	GPT12E_T6IC	xx'0098 _H	26 _H / 38 _D
GPT2 CAPREL Register	GPT12E_CRIC	xx'009C _H	27 _H / 39 _D
A/D Conversion Complete	ADC_CIC	xx'00A0 _H	28 _H / 40 _D
A/D Overrun Error	ADC_EIC	xx'00A4 _H	29 _H / 41 _D
ASC0 Transmit	ASC0_TIC	xx'00A8 _H	2A _H / 42 _D
ASC0 Transmit Buffer	ASC0_TBIC	xx'011C _H	47 _H / 71 _D
ASC0 Receive	ASC0_RIC	xx'00AC _H	2B _H / 43 _D
ASC0 Error	ASC0_EIC	xx'00B0 _H	2C _H / 44 _D
ASC0 Autobaud	ASC0_ABIC	xx'017C _H	5F _H / 95 _D
SSC0 Transmit	SSC0_TIC	xx'00B4 _H	2D _H / 45 _D
SSC0 Receive	SSC0_RIC	xx'00B8 _H	2E _H / 46 _D
SSC0 Error	SSC0_EIC	xx'00BC _H	2F _H / 47 _D
IIC Data Transfer Event	IIC_DTIC	xx'0100 _H	40 _H / 64 _D
IIC Protocol Event	IIC_PEIC	xx'0104 _H	41 _H / 65 _D
PLL/OWD	PLLIC	xx'010C _H	43 _H / 67 _D
ASC1 Transmit	ASC1_TIC	xx'0120 _H	48 _H / 72 _D
ASC1 Transmit Buffer	ASC1_TBIC	xx'0178 _H	5E _H / 94 _D
ASC1 Receive	ASC1_RIC	xx'0124 _H	49 _H / 73 _D
ASC1 Error	ASC1_EIC	xx'0128 _H	4A _H / 74 _D

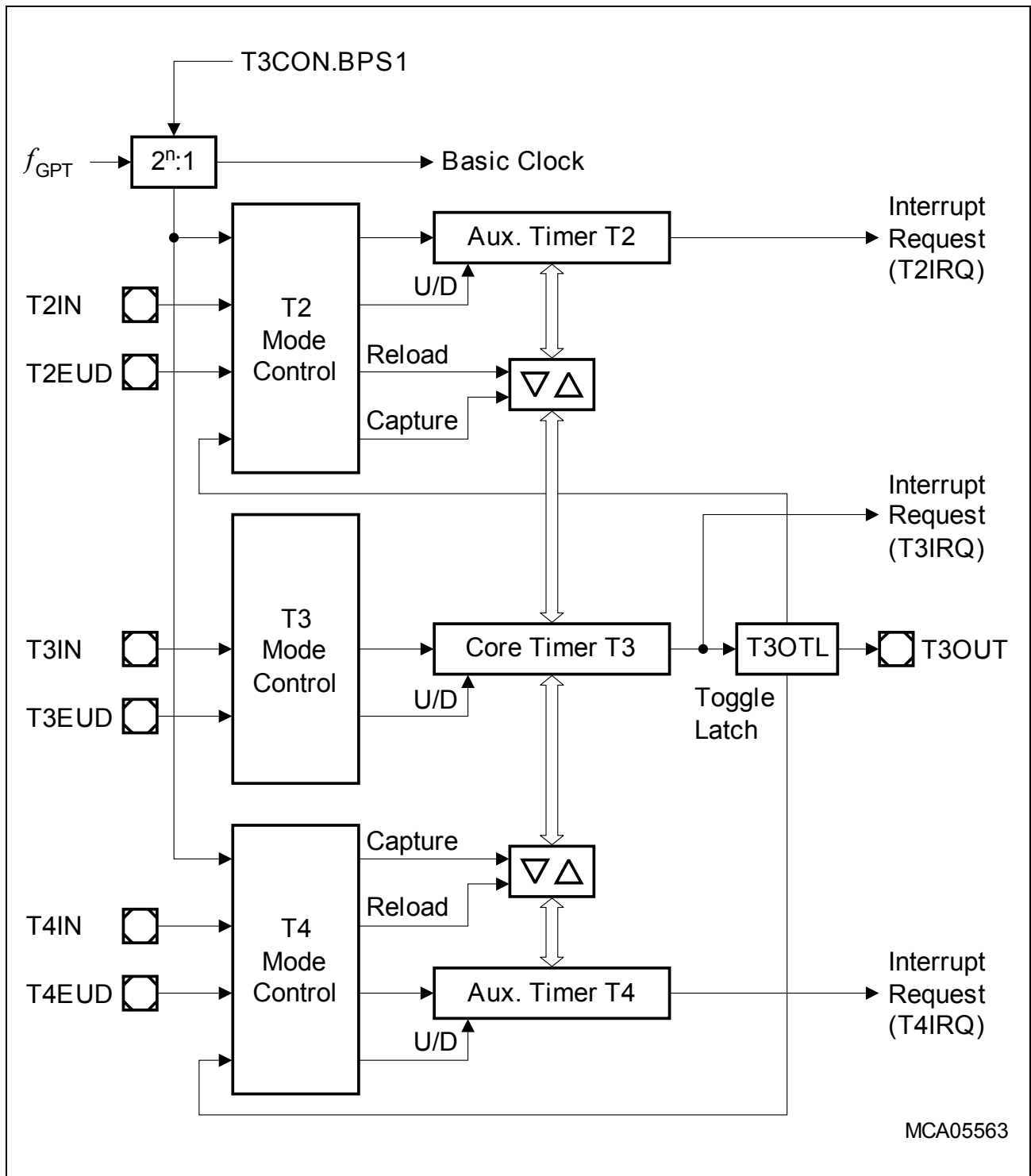


Figure 6 Block Diagram of GPT1

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The

3.16 Clock Generation

The Clock Generation Unit uses a programmable on-chip PLL with multiple prescalers to generate the clock signals for the XC161 with high flexibility. The master clock f_{MC} is the reference clock signal, and is used for TwinCAN and is output to the external system. The CPU clock f_{CPU} and the system clock f_{SYS} are derived from the master clock either directly (1:1) or via a 2:1 prescaler ($f_{SYS} = f_{CPU} = f_{MC} / 2$). See also [Section 4.4.1](#).

The on-chip oscillator can drive an external crystal or accepts an external clock signal. The oscillator clock frequency can be multiplied by the on-chip PLL (by a programmable factor) or can be divided by a programmable prescaler factor.

If the bypass mode is used (direct drive or prescaler) the PLL can deliver an independent clock to monitor the clock signal generated by the on-chip oscillator. This PLL clock is independent from the XTAL1 clock. When the expected oscillator clock transitions are missing the Oscillator Watchdog (OWD) activates the PLL Unlock/OWD interrupt node and supplies the CPU with an emergency clock, the PLL clock signal. Under these circumstances the PLL will oscillate with its basic frequency.

The oscillator watchdog can be disabled by switching the PLL off. This reduces power consumption, but also no interrupt request will be generated in case of a missing oscillator clock.

Note: At the end of an external reset ($\overline{EA} = '0'$) the oscillator watchdog may be disabled via hardware by (externally) pulling the \overline{RD} line low upon a reset, similar to the standard reset configuration.

3.17 Parallel Ports

The XC161 provides up to 99 I/O lines which are organized into nine input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of some I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs (except for pin RSTOUT).

The edge characteristics (shape) and driver characteristics (output current) of the port drivers can be selected via registers POCONx.

The input threshold of some ports is selectable (TTL or CMOS like), where the special CMOS like input threshold reduces noise sensitivity due to the input hysteresis. The input threshold may be selected individually for each byte of the respective ports.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

Functional Description
Table 7 Summary of the XC161's Parallel Ports

Port	Control	Alternate Functions
PORT0	Pad drivers	Address/Data lines or data lines ¹⁾
PORT1	Pad drivers	Address lines ²⁾
		Capture inputs or compare outputs, Serial interface lines
Port 2	Pad drivers, Open drain, Input threshold	Capture inputs or compare outputs, Timer control signal, Fast external interrupt inputs
Port 3	Pad drivers, Open drain, Input threshold	Timer control signals, serial interface lines, Optional bus control signal $\overline{\text{BHE}}/\overline{\text{WRH}}$, System clock output CLKOUT (or FOUT)
Port 4	Pad drivers, Open drain, Input threshold	Segment address lines ³⁾
		CAN/SDLM interface lines ⁴⁾
Port 5	–	Analog input channels to the A/D converter, Timer control signals
Port 6	Open drain, Input threshold	Capture inputs or compare outputs, Bus arbitration signals $\overline{\text{BREQ}}$, $\overline{\text{HLDA}}$, $\overline{\text{HOLD}}$, Optional chip select signals
Port 7	Open drain, Input threshold	Capture inputs or compare outputs, CAN/SDLM interface lines ⁴⁾
Port 9	Pad drivers, Open drain, Input threshold	Capture inputs or compare outputs
		CAN/SDLM interface lines ⁴⁾ , IIC bus interface lines ⁴⁾
Port 20	Pad drivers, Open drain	Bus control signals $\overline{\text{RD}}$, $\overline{\text{WR}}/\overline{\text{WRL}}$, $\overline{\text{READY}}$, $\overline{\text{ALE}}$, External access enable pin $\overline{\text{EA}}$, Reset indication output $\overline{\text{RSTOUT}}$

1) For multiplexed bus cycles.

2) For demultiplexed bus cycles.

3) For more than 64 Kbytes of external resources.

4) Can be assigned by software.

Functional Description
Table 8 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

Electrical Parameters

- 3) The pad supply voltage pins (V_{DDP}) mainly provide the current consumed by the pin output drivers. This output driver current is not covered by parameter I_{DDP} . A small amount of current is consumed even though no outputs are driven, because the drivers' input stages are switched and also the Flash module draws some power from the V_{DDP} supply.
- 4) The total supply current in Sleep and Power down mode is the sum of the temperature dependent leakage current and the frequency dependent current for RTC and main oscillator or auxiliary oscillator (if active).
- 5) This parameter is determined mainly by the transistor leakage currents. This current heavily depends on the junction temperature (see [Figure 12](#)). The junction temperature T_J is the same as the ambient temperature T_A if no current flows through the port output drivers. Otherwise, the resulting temperature difference must be taken into account.
- 6) All inputs (including JTAG pins and pins configured as inputs) at 0 V to 0.1 V or at $V_{DDP} - 0.1$ V to V_{DDP} , all outputs (including pins configured as outputs) disconnected. This parameter is tested at 25 °C and is valid for $T_J \geq 25$ °C.
- 7) This parameter is determined mainly by the current consumed by the oscillator switched to low gain mode (see [Figure 11](#)). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The given values refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

4.3 Analog/Digital Converter Parameters

Table 14 A/D Converter Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Analog reference supply	V_{AREF}	SR	4.5	$V_{DDP} + 0.1$	V	¹⁾
Analog reference ground	V_{AGND}	SR	$V_{SS} - 0.1$	$V_{SS} + 0.1$	V	—
Analog input voltage range	V_{AIN}	SR	V_{AGND}	V_{AREF}	V	²⁾
Basic clock frequency	f_{BC}		0.5	20	MHz	³⁾
Conversion time for 10-bit result ⁴⁾	t_{C10P}	CC	$52 \times t_{BC} + t_S + 6 \times t_{SYS}$		—	Post-calibr. on
	t_{C10}	CC	$40 \times t_{BC} + t_S + 6 \times t_{SYS}$		—	Post-calibr. off
Conversion time for 8-bit result ⁴⁾	t_{C8P}	CC	$44 \times t_{BC} + t_S + 6 \times t_{SYS}$		—	Post-calibr. on
	t_{C8}	CC	$32 \times t_{BC} + t_S + 6 \times t_{SYS}$		—	Post-calibr. off
Calibration time after reset	t_{CAL}	CC	484	11,696	t_{BC}	⁵⁾
Total unadjusted error	TUE	CC	—	± 2	LSB	¹⁾
Total capacitance of an analog input	C_{AINT}	CC	—	15	pF	⁶⁾
Switched capacitance of an analog input	C_{AINS}	CC	—	10	pF	⁶⁾
Resistance of the analog input path	R_{AIN}	CC	—	2	k Ω	⁶⁾
Total capacitance of the reference input	C_{AREFT}	CC	—	20	pF	⁶⁾
Switched capacitance of the reference input	C_{AREFS}	CC	—	15	pF	⁶⁾
Resistance of the reference input path	R_{AREF}	CC	—	1	k Ω	⁶⁾

1) TUE is tested at $V_{AREF} = V_{DDP} + 0.1$ V, $V_{AGND} = 0$ V. It is verified by design for all other voltages within the defined voltage range.

If the analog reference supply voltage drops below 4.5 V (and $V_{AREF} \geq 4.0$ V) or exceeds the power supply voltage by up to 0.2 V (i.e. $V_{AREF} \leq V_{DDP} + 0.2$ V) the maximum TUE is increased to ± 3 LSB. This range is not subject to production test.

The specified TUE is guaranteed only, if the absolute sum of input overload currents on Port 5 pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the respective period of time. During the reset calibration sequence the maximum TUE may be ± 4 LSB.

2) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be X000_H or X3FF_H, respectively.

Electrical Parameters

- 3) The limit values for f_{BC} must not be exceeded when selecting the peripheral frequency and the ADCTC setting.
- 4) This parameter includes the sample time t_S , the time for determining the digital result and the time to load the result register with the conversion result ($t_{SYS} = 1/f_{SYS}$).

Values for the basic clock t_{BC} depend on programming and can be taken from [Table 15](#).

When the post-calibration is switched off, the conversion time is reduced by $12 \times t_{BC}$.

- 5) The actual duration of the reset calibration depends on the noise on the reference signal. Conversions executed during the reset calibration increase the calibration time. The TUE for those conversions may be increased.
- 6) Not subject to production test - verified by design/characterization.

The given parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) reduced values can be used for calculations. At room temperature and nominal supply voltage the following typical values can be used:

$C_{AINTtyp} = 12 \text{ pF}$, $C_{AINStyp} = 7 \text{ pF}$, $R_{AINTyp} = 1.5 \text{ k}\Omega$, $C_{AREFTyp} = 15 \text{ pF}$, $C_{AREFStyp} = 13 \text{ pF}$, $R_{AREFTyp} = 0.7 \text{ k}\Omega$.

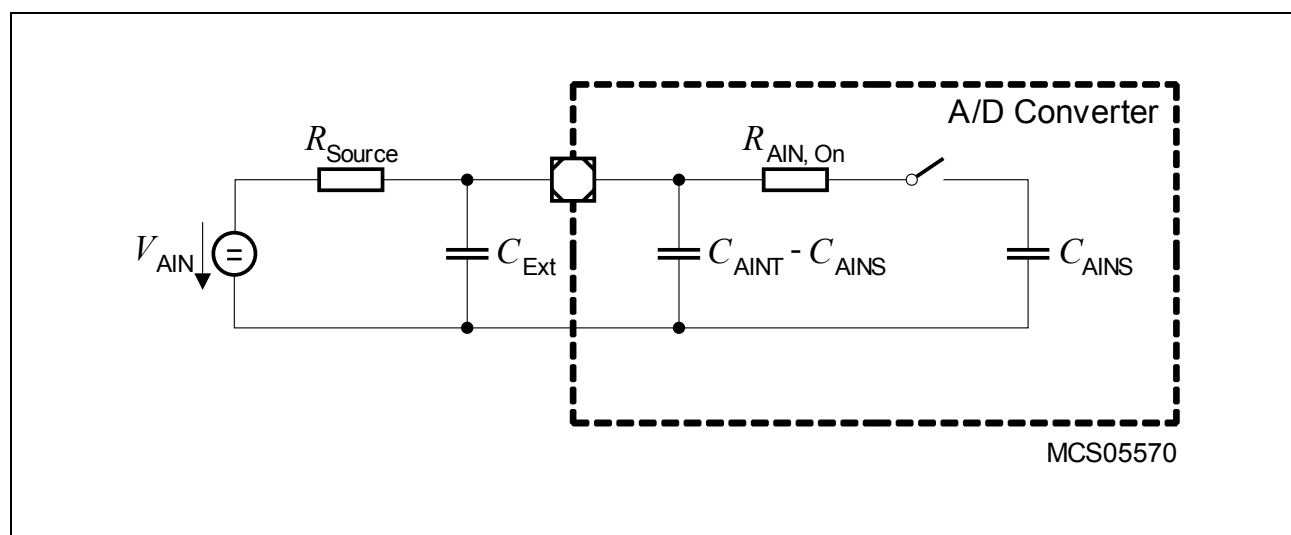


Figure 13 **Equivalent Circuitry for Analog Inputs**

Electrical Parameters

Sample time and conversion time of the XC161's A/D Converter are programmable. In compatibility mode, the above timing can be calculated using [Table 15](#). The limit values for f_{BC} must not be exceeded when selecting ADCTC.

Table 15 A/D Converter Computation Table¹⁾

ADCON.15 14 (ADCTC)	A/D Converter Basic Clock f_{BC}	ADCON.13 12 (ADSTC)	Sample Time t_s
00	$f_{SYS} / 4$	00	$t_{BC} \times 8$
01	$f_{SYS} / 2$	01	$t_{BC} \times 16$
10	$f_{SYS} / 16$	10	$t_{BC} \times 32$
11	$f_{SYS} / 8$	11	$t_{BC} \times 64$

1) These selections are available in compatibility mode. An improved mechanism to control the ADC input clock can be selected.

Converter Timing Example:

Assumptions: $f_{SYS} = 40$ MHz (i.e. $t_{SYS} = 25$ ns), ADCTC = '01', ADSTC = '00'

Basic clock $f_{BC} = f_{SYS} / 2 = 20$ MHz, i.e. $t_{BC} = 50$ ns

Sample time $t_s = t_{BC} \times 8 = 400$ ns

Conversion 10-bit:

With post-calibr. $t_{C10P} = 52 \times t_{BC} + t_s + 6 \times t_{SYS} = (2600 + 400 + 150)$ ns = 3.15 μ s

Post-calibr. off $t_{C10} = 40 \times t_{BC} + t_s + 6 \times t_{SYS} = (2000 + 400 + 150)$ ns = 2.55 μ s

Conversion 8-bit:

With post-calibr. $t_{C8P} = 44 \times t_{BC} + t_s + 6 \times t_{SYS} = (2200 + 400 + 150)$ ns = 2.75 μ s

Post-calibr. off $t_{C8} = 32 \times t_{BC} + t_s + 6 \times t_{SYS} = (1600 + 400 + 150)$ ns = 2.15 μ s

Table 16 VCO Bands for PLL Operation¹⁾

PLLCON.PLLVB	VCO Frequency Range	Base Frequency Range
00	100 ... 150 MHz	20 ... 80 MHz
01	150 ... 200 MHz	40 ... 130 MHz
10	200 ... 250 MHz	60 ... 180 MHz
11	Reserved	

1) Not subject to production test - verified by design/characterization.

4.4.4 Testing Waveforms

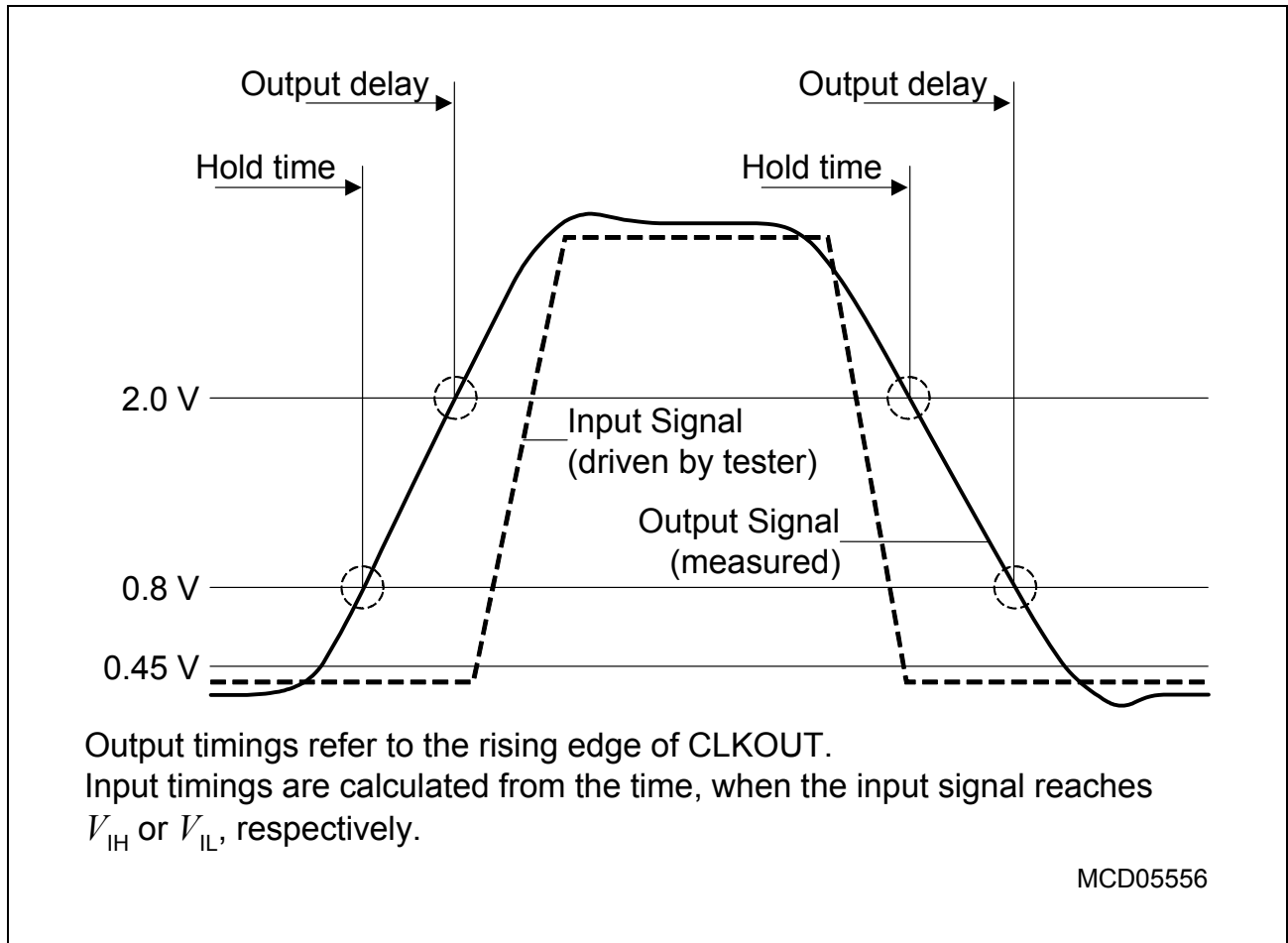


Figure 17 Input Output Waveforms

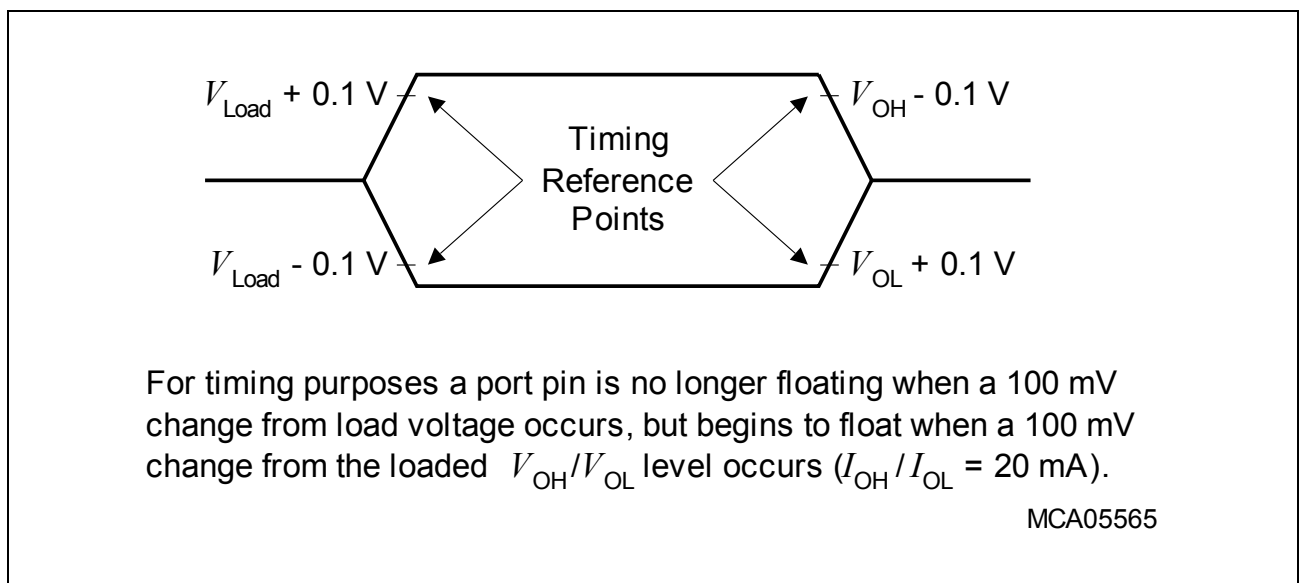


Figure 18 Float Waveforms

Bus Cycle Control via READY Input

The duration of an external bus cycle can be controlled by the external circuitry via the READY input signal. The polarity of this input signal can be selected.

Synchronous READY permits the shortest possible bus cycle but requires the input signal to be synchronous to the reference signal CLKOUT.

Asynchronous READY puts no timing constraints on the input signal but incurs one waitstate minimum due to the additional synchronization stage. The minimum duration of an asynchronous READY signal to be safely synchronized must be one CLKOUT period plus the input setup time.

An active READY signal can be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).

If the next following bus cycle is READY-controlled, an active READY signal must be disabled before the first valid sample point for the next bus cycle. This sample point depends on the programmed phases of the next following cycle.

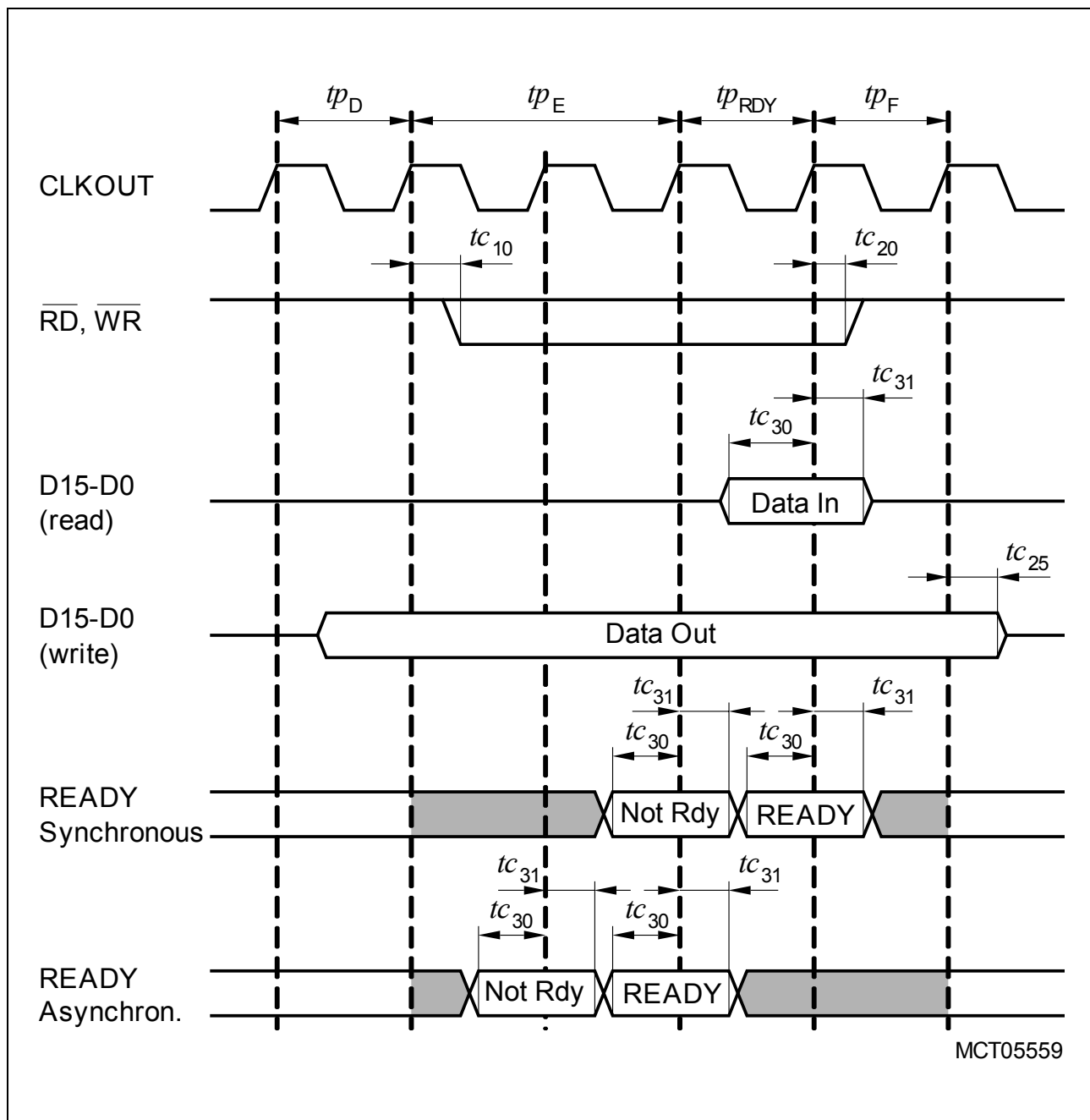


Figure 22 **READY Timing**

Note: If the READY input is sampled inactive at the indicated sampling point ("Not Rdy") a READY-controlled waitstate is inserted (tp_{RDY}), sampling the READY input active at the indicated sampling point ("Ready") terminates the currently running bus cycle.

Note the different sampling points for synchronous and asynchronous READY. This example uses one mandatory waitstate (see tp_E) before the READY input is evaluated.

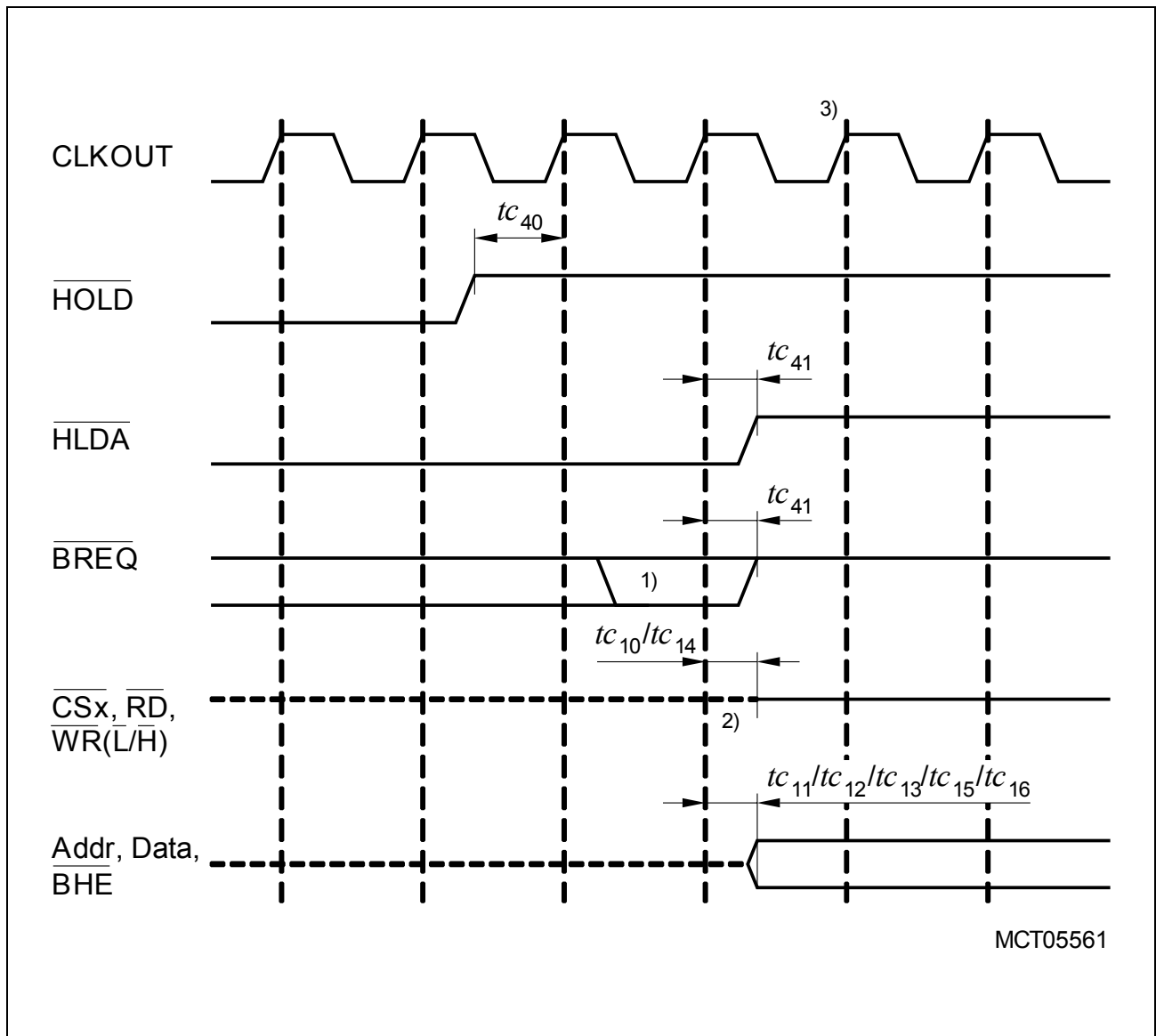


Figure 24 External Bus Arbitration, Regaining the Bus

Notes

1. This is the last chance for \overline{BREQ} to trigger the indicated regain-sequence. Even if \overline{BREQ} is activated earlier, the regain-sequence is initiated by \overline{HOLD} going high. Please note that \overline{HOLD} may also be deactivated without the XC161 requesting the bus.
2. The control outputs will be resistive high (pull-up) before being driven inactive (ALE will be low).
3. The next XC161 driven bus cycle may start here.

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