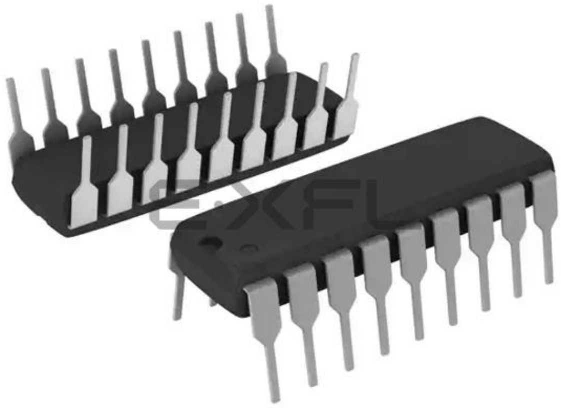

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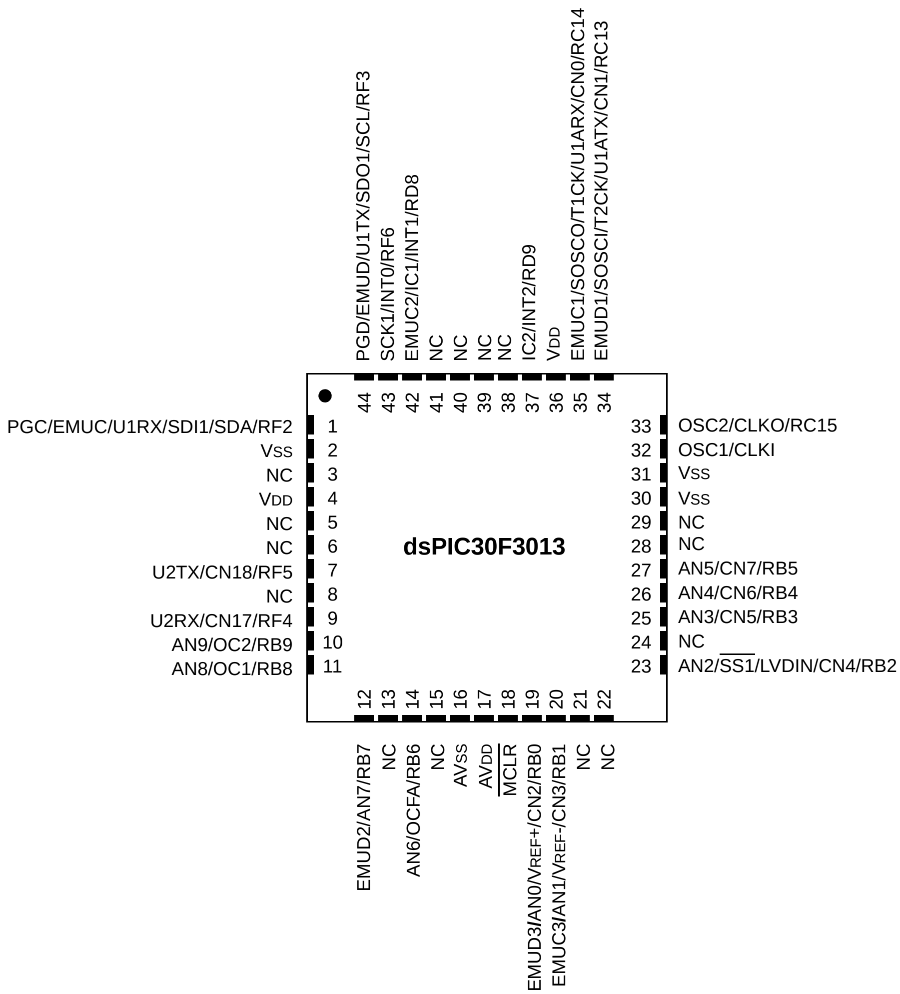
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	20 MIPS
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	12KB (4K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic30f2011-20e-p

Pin Diagrams

44-Pin QFN(1)



Note 1: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

FIGURE 1-4: dsPIC30F3013 BLOCK DIAGRAM

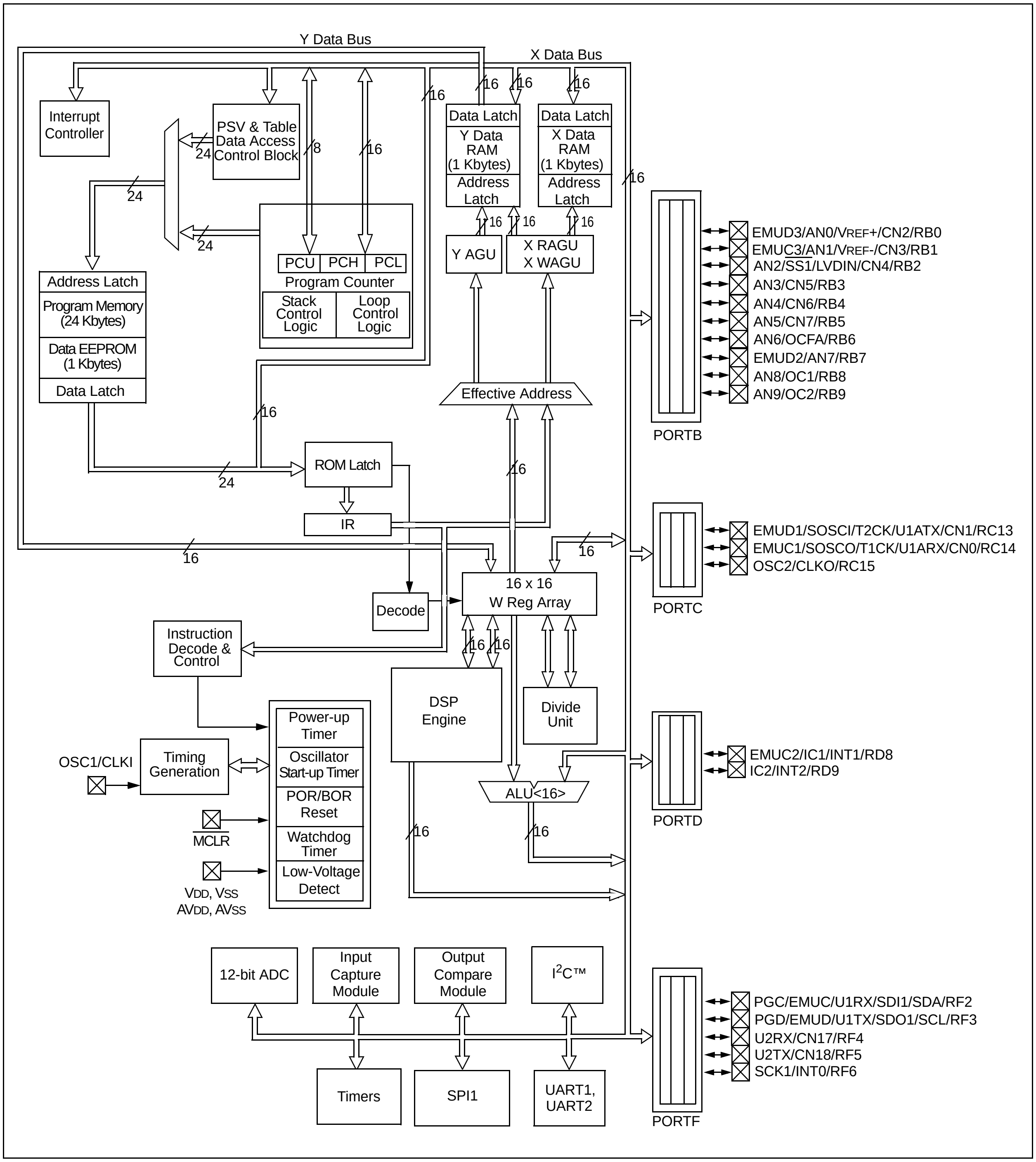
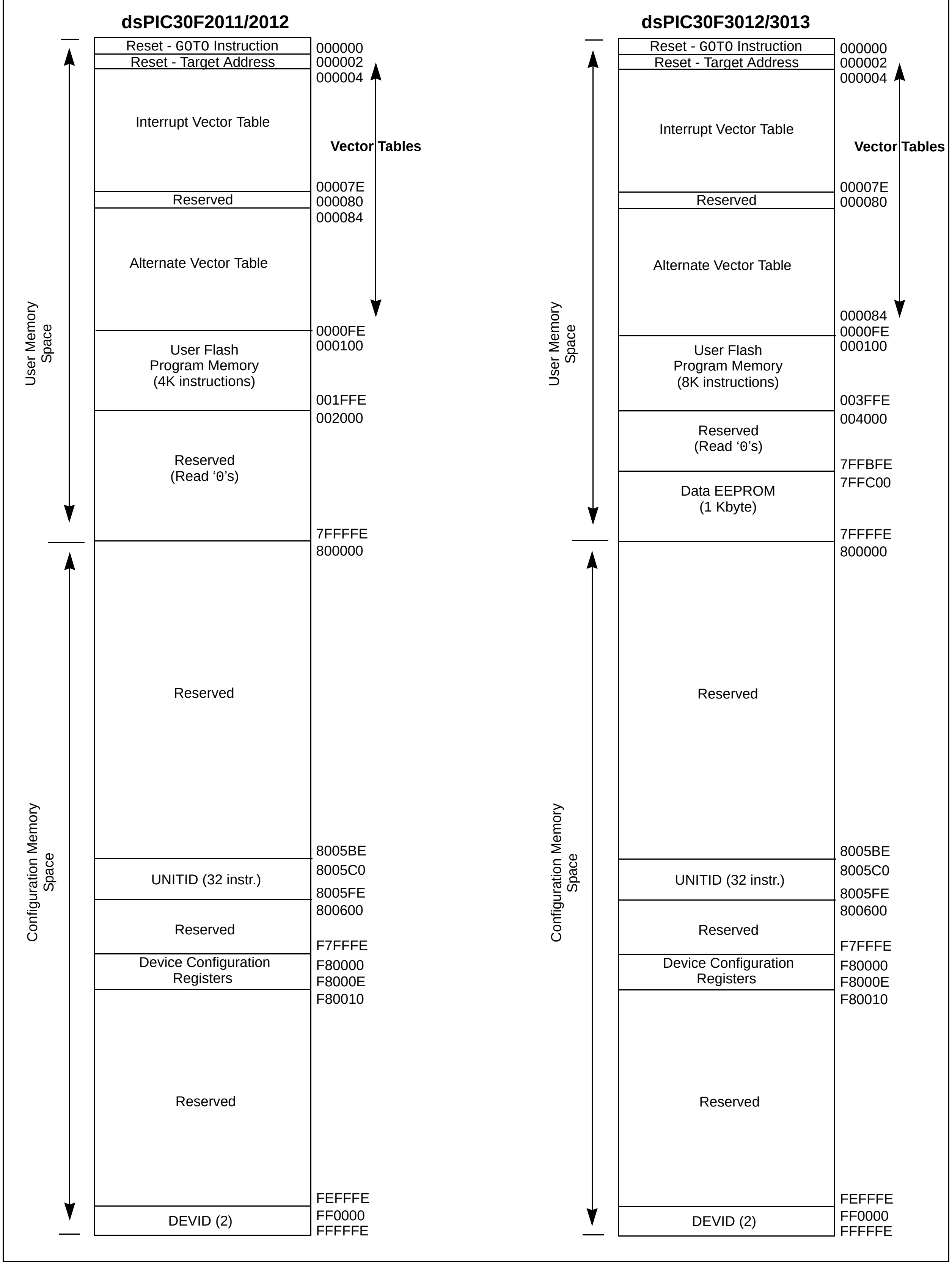


FIGURE 3-1: PROGRAM SPACE MEMORY MAPS



NOTES:

4.2.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and an ending address be specified and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 3-3).

> **Note:** Y space Modulo Addressing EA calculations assume word-sized data (LSb of every EA is always clear).

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding Start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

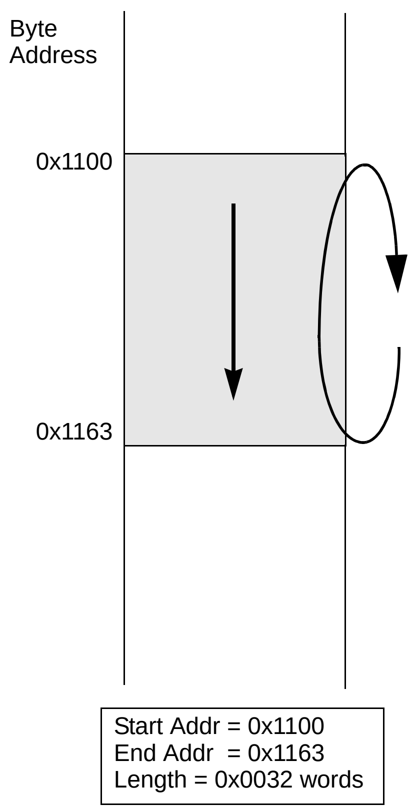
4.2.2 W ADDRESS REGISTER SELECTION

The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags as well as a W register field to specify the W address registers. The XWM and YWM fields select which registers operate with Modulo Addressing. If XWM = 15, X RAGU and X WAGU Modulo Addressing is disabled. Similarly, if YWM = 15, Y AGU Modulo Addressing is disabled.

The X Address Space Pointer W register (XWM), to which Modulo Addressing is to be applied, is stored in MODCON<3:0> (see Table 3-3). Modulo Addressing is enabled for X data space when XWM is set to any value other than '15' and the XMODEN bit is set at MODCON<15>.

The Y Address Space Pointer W register (YWM), to which Modulo Addressing is to be applied, is stored in MODCON<7:4>. Modulo Addressing is enabled for Y data space when YWM is set to any value other than '15' and the YMODEN bit is set at MODCON<14>.

FIGURE 4-1: MODULO ADDRESSING OPERATION EXAMPLE




```
MOV    #0x1100,W0
MOV    W0,XMODSRT    ;set modulo start address
MOV    #0x1163,W0
MOV    W0,MODEND     ;set modulo end address
MOV    #0x8001,W0
MOV    W0,MODCON     ;enable W1, X AGU for modulo

MOV    #0x0000,W0    ;W0 holds buffer fill value

MOV    #0x1110,W1    ;point W1 to buffer

DO     AGAIN,#0x31   ;fill the 50 buffer locations
MOV    W0,[W1++]     ;fill the next location
AGAIN: INC  W0,W0    ;increment the fill value
```

FIGURE 8-1: TRAP VECTORS

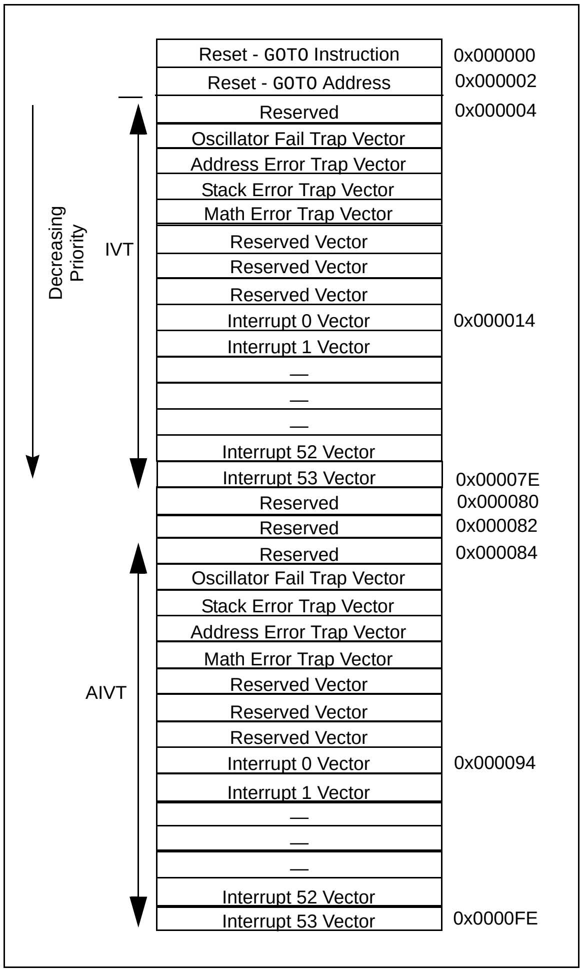
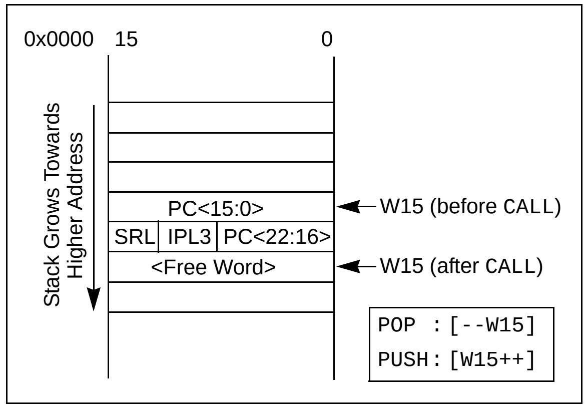


FIGURE 8-2: INTERRUPT STACK FRAME



Note 1:	The user can always lower the priority level by writing a new value into SR. The Interrupt Service Routine must clear the interrupt flag bits in the IFSx register before lowering the processor interrupt priority, in order to avoid recursive interrupts.
2:	The IPL3 bit (CORCON<3>) is always clear when interrupts are being processed. It is set only during execution of traps.

The RETFIE (return from interrupt) instruction unstacks the program counter and STATUS registers to return the processor to its state prior to the interrupt sequence.

8.4 Interrupt Sequence

All interrupt event flags are sampled in the beginning of each instruction cycle by the IFSx registers. A pending Interrupt Request (IRQ) is indicated by the flag bit being equal to a ‘1’ in an IFSx register. The IRQ causes an interrupt to occur if the corresponding bit in the Interrupt Enable (IECx) register is set. For the remainder of the instruction cycle, the priorities of all pending interrupt requests are evaluated.

If there is a pending IRQ with a priority level greater than the current processor priority level in the IPL bits, the processor is interrupted.

The processor then stacks the current program counter and the low byte of the processor STATUS register (SRL), as shown in Figure 8-2. The low byte of the STATUS register contains the processor priority level at the time prior to the beginning of the interrupt cycle. The processor then loads the priority level for this interrupt into the STATUS register. This action disables all lower priority interrupts until the completion of the Interrupt Service Routine (ISR).

8.5 Alternate Vector Table

In program memory, the Interrupt Vector Table (IVT) is followed by the Alternate Interrupt Vector Table (AIVT), as shown in Figure 8-1. Access to the alternate vector table is provided by the ALTIVT bit in the INTCON2 register. If the ALTIVT bit is set, all interrupt and exception processes use the alternate vectors instead of the default vectors. The alternate vectors are organized in the same manner as the default vectors. The AIVT supports emulation and debugging efforts by providing a means to switch between an application and a support environment without requiring the interrupt vectors to be reprogrammed. This feature also enables switching between applications for evaluation of different software algorithms at run time.

If the AIVT is not required, the program memory allocated to the AIVT may be used for other purposes. AIVT is not a protected section and may be freely programmed by the user.

8.6 Fast Context Saving

A context saving option is available using shadow registers. Shadow registers are provided for the DC, N, OV, Z and C bits in SR, and the registers W0 through W3. The shadows are only one level deep. The shadow registers are accessible using the `PUSH.S` and `POP.S` instructions only.

When the processor vectors to an interrupt, the `PUSH.S` instruction can be used to store the current value of the aforementioned registers into their respective shadow registers.

If an ISR of a certain priority uses the `PUSH.S` and `POP.S` instructions for fast context saving, then a higher priority ISR should not include the same instructions. Users must save the key registers in software during a lower priority interrupt if the higher priority ISR uses fast context saving.

8.7 External Interrupt Requests

The interrupt controller supports three external interrupt request signals, INT0-INT2. These inputs are edge sensitive; they require a low-to-high or a high-to-low transition to generate an interrupt request. The INTCON2 register has three bits, INT0EP-INT2EP, that select the polarity of the edge detection circuitry.

8.8 Wake-up from Sleep and Idle

The interrupt controller may be used to wake-up the processor from either Sleep or Idle modes, if Sleep or Idle mode is active when the interrupt is generated.

If an enabled interrupt request of sufficient priority is received by the interrupt controller, then the standard interrupt request is presented to the processor. At the same time, the processor wakes up from Sleep or Idle and begins execution of the ISR needed to process the interrupt request.

12.0 OUTPUT COMPARE MODULE

Note:	This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046).

This section describes the output compare module and associated operational modes. The features provided by this module are useful in applications requiring operational modes, such as:

- Generation of Variable Width Output Pulses
- Power Factor Correction

Figure 12-1 depicts a block diagram of the output compare module.

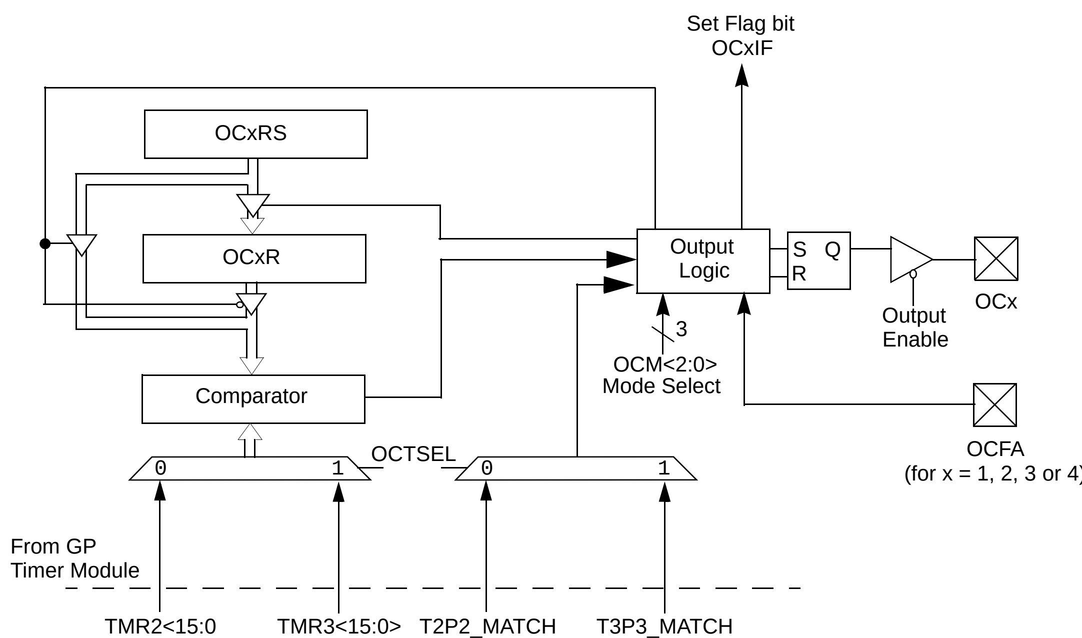
The key operational features of the output compare module include:

- Timer2 and Timer3 Selection mode
- Simple Output Compare Match mode
- Dual Output Compare Match mode
- Simple PWM mode
- Output Compare During Sleep and Idle modes
- Interrupt on Output Compare/PWM Event

These operating modes are determined by setting the appropriate bits in the 16-bit OC1CON and OC2CON registers. The dsPIC30F2011/2012/3012/3013 devices have 2 compare channels.

OCxRS and OCxR in Figure 12-1 represent the Dual Compare registers. In the Dual Compare mode, the OCxR register is used for the first compare and OCxRS is used for the second compare.

FIGURE 12-1: OUTPUT COMPARE MODE BLOCK DIAGRAM(1)



Note 1: Where 'x' is shown, reference is made to the registers associated with the respective output compare channel (1 or 2).

12.5 Output Compare Operation During CPU Sleep Mode

When the CPU enters Sleep mode, all internal clocks are stopped. Therefore, when the CPU enters the Sleep state, the output compare channel drives the pin to the active state that was observed prior to entering the CPU Sleep state.

For example, if the pin was high when the CPU entered the Sleep state, the pin remains high. Likewise, if the pin was low when the CPU entered the Sleep state, the pin remains low. In either case, the output compare module resumes operation when the device wakes up.

12.6 Output Compare Operation During CPU Idle Mode

When the CPU enters the Idle mode, the output compare module can operate with full functionality.

The output compare channel operates during the CPU Idle mode if the OCSIDL bit (OCxCON<13>) is at logic ‘0’ and the selected time base (Timer2 or Timer3) is enabled and the TSIDL bit of the selected timer is set to logic ‘0’.

12.7 Output Compare Interrupts

The output compare channels have the ability to generate an interrupt on a compare match, for whichever Match mode has been selected.

For all modes except the PWM mode, when a compare event occurs, the respective interrupt flag (OCxIF) is asserted and an interrupt is generated if enabled. The OCxIF bit is located in the corresponding IFS register and must be cleared in software. The interrupt is enabled via the respective compare interrupt enable (OCxIE) bit located in the corresponding IEC Control register.

For the PWM mode, when an event occurs, the respective timer interrupt flag (T2IF or T3IF) is asserted and an interrupt is generated if enabled. The IF bit is located in the IFS0 register and must be cleared in software. The interrupt is enabled via the respective timer interrupt enable bit (T2IE or T3IE) located in the IEC0 Control register. The output compare interrupt flag is never set during the PWM mode of operation.

FIGURE 13-1: SPI BLOCK DIAGRAM

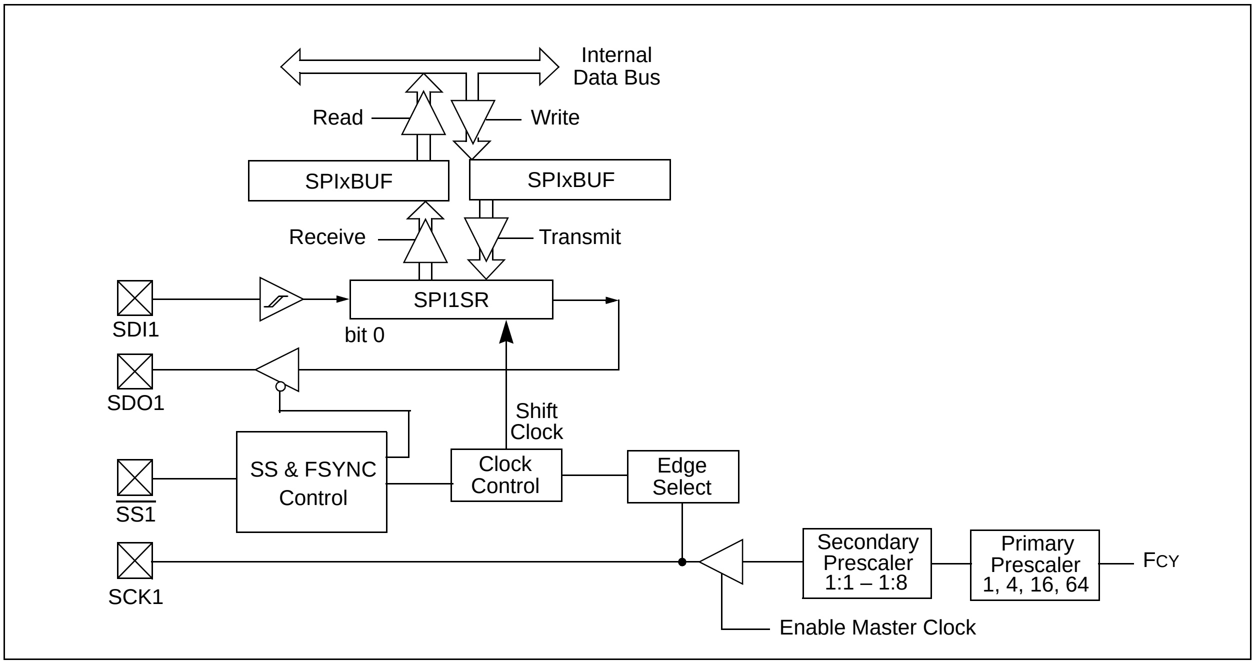


Figure 13-2 depicts the a master/slave connection between two processors. In Master mode, the clock is generated by prescaling the system clock. Data is transmitted as soon as a value is written to SPI1BUF. The interrupt is generated at the middle of the transfer of the last bit.

In Slave mode, data is transmitted and received as external clock pulses appear on SCK. Again, the interrupt is generated when the last bit is latched. If $\overline{\text{SS1}}$ control is enabled, then transmission and reception are enabled only when $\overline{\text{SS1}}$ = low. The SDO1 output will be disabled in $\overline{\text{SS1}}$ mode with $\overline{\text{SS1}}$ high.

The clock provided to the module is (FOSC/4). This clock is then prescaled by the primary (PPRE<1:0>) and the secondary (SPRE<2:0>) prescale factors. The CKE bit determines whether transmit occurs on transition from active clock state to Idle clock state, or vice versa. The CKP bit selects the Idle state (high or low) for the clock.

13.1.1 WORD AND BYTE COMMUNICATION

A control bit, MODE16 (SPI1CON<10>), allows the module to communicate in either 16-bit or 8-bit mode. 16-bit operation is identical to 8-bit operation except that the number of bits transmitted is 16 instead of 8.

The user software must disable the module prior to changing the MODE16 bit. The SPI module is reset when the MODE16 bit is changed by the user.

A basic difference between 8-bit and 16-bit operation is that the data is transmitted out of bit 7 of the SPI1SR for 8-bit operation, and data is transmitted out of bit 15 of the SPI1SR for 16-bit operation. In both modes, data is shifted into bit 0 of the SPI1SR.

13.1.2 SDO1 DISABLE

A control bit, DISSDO, is provided to the SPI1CON register to allow the SDO1 output to be disabled. This will allow the SPI module to be connected in an input only configuration. SDO1 can also be used for general purpose I/O.

13.2 Framed SPI Support

The module supports a basic framed SPI protocol in Master or Slave mode. The control bit, FRMEN, enables framed SPI support and causes the $\overline{\text{SS1}}$ pin to perform the Frame Synchronization Pulse (FSYNC) function. The control bit, SPIFSD, determines whether the $\overline{\text{SS1}}$ pin is an input or an output (i.e., whether the module receives or generates the Frame Synchronization Pulse). The frame pulse is an active-high pulse for a single SPI clock cycle. When Frame Synchronization is enabled, the data transmission starts only on the subsequent transmit edge of the SPI clock.

14.2 I²C Module Addresses

The I2CADD register contains the Slave mode addresses. The register is a 10-bit register.

If the A10M bit (I2CCON<10>) is ‘0’, the address is interpreted by the module as a 7-bit address. When an address is received, it is compared to the 7 LSb of the I2CADD register.

If the A10M bit is ‘1’, the address is assumed to be a 10-bit address. When an address is received, it will be compared with the binary value ‘11110 A9 A8’ (where A9 and A8 are two Most Significant bits of I2CADD). If that value matches, the next address will be compared with the Least Significant 8 bits of I2CADD, as specified in the 10-bit addressing protocol.

The 7-bit I²C Slave Addresses supported by the dsPIC30F are shown in Table 14-1.

TABLE 14-1: 7-BIT I²C™ SLAVE ADDRESSES

0x00	General call address or start byte
0x01-0x03	Reserved
0x04-0x07	Hs-mode Master codes
0x04-0x77	Valid 7-bit addresses
0x78-0x7b	Valid 10-bit addresses (lower 7 bits)
0x7c-0x7f	Reserved

14.3 I²C 7-bit Slave Mode Operation

Once enabled (I2CEN = 1), the slave module will wait for a Start bit to occur (i.e., the I²C module is ‘Idle’). Following the detection of a Start bit, 8 bits are shifted into I2CRSR and the address is compared against I2CADD. In 7-bit mode (A10M = 0), bits I2CADD<6:0> are compared against I2CRSR<7:1> and I2CRSR<0> is the R_W bit. All incoming bits are sampled on the rising edge of SCL.

If an address match occurs, an acknowledgement will be sent, and the slave event interrupt flag (SI2CIF) is set on the falling edge of the ninth ($\overline{\text{ACK}}$) bit. The address match does not affect the contents of the I2CRCV buffer or the RBF bit.

14.3.1 SLAVE TRANSMISSION

If the R_W bit received is a ‘1’, then the serial port will go into Transmit mode. It will send $\overline{\text{ACK}}$ on the ninth bit and then hold SCL to ‘0’ until the CPU responds by writing to I2CTRN. SCL is released by setting the SCLREL bit, and 8 bits of data are shifted out. Data bits are shifted out on the falling edge of SCL, such that SDA is valid during SCL high. The interrupt pulse is sent on the falling edge of the ninth clock pulse, regardless of the status of the $\overline{\text{ACK}}$ received from the master.

14.3.2 SLAVE RECEPTION

If the R_W bit received is a ‘0’ during an address match, then Receive mode is initiated. Incoming bits are sampled on the rising edge of SCL. After 8 bits are received, if I2CRCV is not full or I2COV is not set, I2CRSR is transferred to I2CRCV. $\overline{\text{ACK}}$ is sent on the ninth clock.

If the RBF flag is set, indicating that I2CRCV is still holding data from a previous operation (RBF = 1), then $\overline{\text{ACK}}$ is not sent; however, the interrupt pulse is generated. In the case of an overflow, the contents of the I2CRSR are not loaded into the I2CRCV.

> **Note:** The I2CRCV will be loaded if the I2COV bit = 1 and the RBF flag = 0. In this case, a read of the I2CRCV was performed but the user did not clear the state of the I2COV bit before the next receive occurred. The acknowledgement is not sent ($\overline{\text{ACK}}$ = 1) and the I2CRCV is updated.

14.4 I²C 10-bit Slave Mode Operation

In 10-bit mode, the basic receive and transmit operations are the same as in the 7-bit mode. However, the criteria for address match is more complex.

The I²C specification dictates that a slave must be addressed for a write operation with two address bytes following a Start bit.

The A10M bit is a control bit that signifies that the address in I2CADD is a 10-bit address rather than a 7-bit address. The address detection protocol for the first byte of a message address is identical for 7-bit and 10-bit messages, but the bits being compared are different.

I2CADD holds the entire 10-bit address. Upon receiving an address following a Start bit, I2CRSR <7:3> is compared against a literal ‘11110’ (the default 10-bit address) and I2CRSR<2:1> are compared against I2CADD<9:8>. If a match occurs and if R_W = 0, the interrupt pulse is sent. The ADD10 bit will be cleared to indicate a partial address match. If a match fails or R_W = 1, the ADD10 bit is cleared and the module returns to the Idle state.

The low byte of the address is then received and compared with I2CADD<7:0>. If an address match occurs, the interrupt pulse is generated and the ADD10 bit is set, indicating a complete 10-bit address match. If an address match did not occur, the ADD10 bit is cleared and the module returns to the Idle state.

TABLE 14-2: I²C REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
I2CRCV	0200	—	—	—	—	—	—	—	—	Receive Register								0000 0000 0000 0000
I2CTRN	0202	—	—	—	—	—	—	—	—	Transmit Register								0000 0000 1111 1111
I2CBRG	0204	—	—	—	—	—	—	—	Baud Rate Generator									0000 0000 0000 0000
I2CCON	0206	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0001 0000 0000 0000
I2CSTAT	0208	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000 0000 0000 0000
I2CADD	020A	—	—	—	—	—	—	Address Register										0000 0000 0000 0000

Legend: — = unimplemented bit, read as ‘0’

Note: Refer to the “*dsPIC30F Family Reference Manual*” (DS70046) for descriptions of register bit fields.

The configuration procedures in the next section provide the required setup values for the conversion speeds above 100 ksps.

16.7.1 200 KSPS CONFIGURATION GUIDELINE

The following configuration items are required to achieve a 200 ksps conversion rate.

- Comply with conditions provided in Table 16-1.
- Connect external $V_{REF}+$ and $V_{REF}-$ pins following the recommended circuit shown in Figure 16-2.
- Set SSRC<2.0> = `111` in the ADCON1 register to enable the auto convert option.
- Enable automatic sampling by setting the ASAM control bit in the ADCON1 register.
- Write the SMPI<3.0> control bits in the ADCON2 register for the desired number of conversions between interrupts.
- Configure the ADC clock period to be:

$$\frac{1}{(14 + 1) \times 200{,}000} = 334 \text{ ns}$$

  by writing to the ADCS<5:0> control bits in the ADCON3 register.
- Configure the sampling time to be 1 T_{AD} by writing: SAMC<4:0> = `00001`.

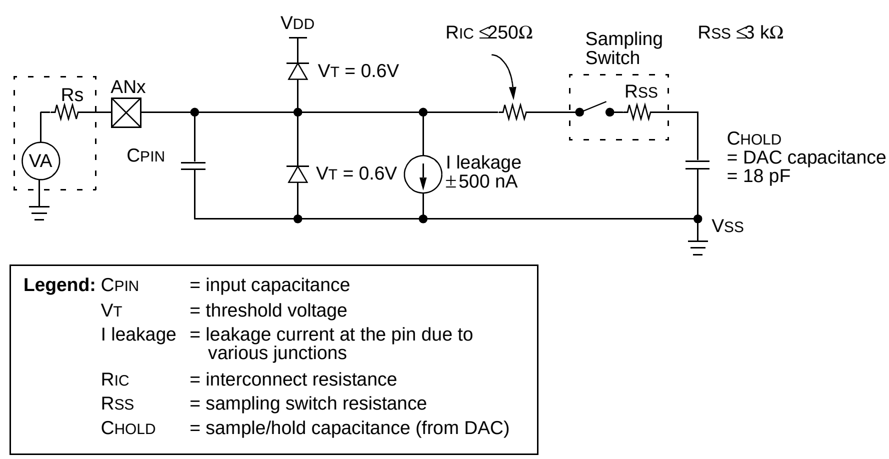
The following figure shows the timing diagram of the ADC running at 200 ksps. The T_{AD} selection in conjunction with the guidelines described above allows a conversion speed of 200 ksps. See Example 16-1 for code example.

16.8 A/D Acquisition Requirements

The analog input model of the 12-bit ADC is shown in Figure 16-3. The total sampling time for the A/D is a function of the internal amplifier settling time and the holding capacitor charge time.

For the ADC to meet its specified accuracy, the charge holding capacitor (C_{HOLD}) must be allowed to fully charge to the voltage level on the analog input pin. The source impedance (R_S), the interconnect impedance (R_{IC}) and the internal sampling switch (R_{SS}) impedance combine to directly affect the time required to charge the capacitor C_{HOLD}. The combined impedance of the analog sources must therefore be small enough to fully charge the holding capacitor within the chosen sample time. To minimize the effects of pin leakage currents on the accuracy of the ADC, the maximum recommended source impedance, R_S, is 2.5 kΩ. After the analog input channel is selected (changed), this sampling function must be completed prior to starting the conversion. The internal holding capacitor will be in a discharged state prior to each sample operation.

FIGURE 16-3: 12-BIT A/D CONVERTER ANALOG INPUT MODEL



Note: C_{PIN} value depends on device package and is not tested. Effect of C_{PIN} negligible if Rs ≤2.5 kΩ.

17.0 SYSTEM INTEGRATION

> **Note:** This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046). For more information on the device instruction set and programming, refer to the "*16-bit MCU and DSC Programmer's Reference Manual*" (DS70157).

There are several features intended to maximize system reliability, minimize cost through elimination of external components, provide Power Saving Operating modes and offer code protection:

- Oscillator Selection
- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Programmable Brown-out Reset (BOR)
- Watchdog Timer (WDT)
- Low-Voltage Detect
- Power-Saving Modes (Sleep and Idle)
- Code Protection
- Unit ID Locations
- In-Circuit Serial Programming (ICSP)

dsPIC30F devices have a Watchdog Timer which is permanently enabled via the Configuration bits or can be software controlled. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT) which provides a delay on power-up only, designed to keep the part in Reset while the power supply stabilizes. With these two timers on-chip, most applications need no external Reset circuitry.

Sleep mode is designed to offer a very low current Power-Down mode. The user can wake-up from Sleep through external Reset, Watchdog Timer Wake-up, or through an interrupt. Several oscillator options are also made available to allow the part to fit a wide variety of applications. In the Idle mode, the clock sources are still active but the CPU is shut-off. The RC oscillator option saves system cost while the LP crystal option saves power.

17.1 Oscillator System Overview

The dsPIC30F oscillator system has the following modules and features:

- Various external and internal oscillator options as clock sources
- An on-chip PLL to boost internal operating frequency
- A clock switching mechanism between various clock sources
- Programmable clock postscaler for system power savings
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and takes fail-safe measures
- Clock Control register (OSCCON)
- Configuration bits for main oscillator selection

Configuration bits determine the clock source upon Power-on Reset (POR) and Brown-out Reset (BOR). Thereafter, the clock source can be changed between permissible clock sources. The OSCCON register controls the clock switching and reflects system clock related status bits.

Table 17-1 provides a summary of the dsPIC30F Oscillator Operating modes. A simplified diagram of the oscillator system is shown in Figure 17-1.

Table 17-5 shows the Reset conditions for the RCON register. Since the control bits within the RCON register are R/W, the information in the table means that all the bits are negated prior to the action specified in the condition column.

TABLE 17-5: INITIALIZATION CONDITION FOR RCON REGISTER: CASE 1

Condition	Program Counter	TRAPR	IOPUWR	EXTR	SWR	WDTO	IDLE	SLEEP	POR	BOR
Power-on Reset	0x000000	0	0	0	0	0	0	0	1	1
Brown-out Reset	0x000000	0	0	0	0	0	0	0	0	1
$\overline{\text{MCLR}}$ Reset during normal operation	0x000000	0	0	1	0	0	0	0	0	0
Software Reset during normal operation	0x000000	0	0	0	1	0	0	0	0	0
$\overline{\text{MCLR}}$ Reset during Sleep	0x000000	0	0	1	0	0	0	1	0	0
$\overline{\text{MCLR}}$ Reset during Idle	0x000000	0	0	1	0	0	1	0	0	0
WDT Time-out Reset	0x000000	0	0	0	0	1	0	0	0	0
WDT Wake-up	PC + 2	0	0	0	0	1	0	1	0	0
Interrupt Wake-up from Sleep	PC + 2(1)	0	0	0	0	0	0	1	0	0
Clock Failure Trap	0x000004	0	0	0	0	0	0	0	0	0
Trap Reset	0x000000	1	0	0	0	0	0	0	0	0
Illegal Operation Trap	0x000000	0	1	0	0	0	0	0	0	0

Note 1: When the wake-up is due to an enabled interrupt, the PC is loaded with the corresponding interrupt vector.

Table 17-6 shows a second example of the bit conditions for the RCON register. In this case, it is not assumed the user has set/cleared specific bits prior to action specified in the condition column.

TABLE 17-6: INITIALIZATION CONDITION FOR RCON REGISTER: CASE 2

Condition	Program Counter	TRAPR	IOPUWR	EXTR	SWR	WDTO	IDLE	SLEEP	POR	BOR
Power-on Reset	0x000000	0	0	0	0	0	0	0	1	1
Brown-out Reset	0x000000	u	u	u	u	u	u	u	0	1
$\overline{\text{MCLR}}$ Reset during normal operation	0x000000	u	u	1	0	0	0	0	u	u
Software Reset during normal operation	0x000000	u	u	0	1	0	0	0	u	u
$\overline{\text{MCLR}}$ Reset during Sleep	0x000000	u	u	1	u	0	0	1	u	u
$\overline{\text{MCLR}}$ Reset during Idle	0x000000	u	u	1	u	0	1	0	u	u
WDT Time-out Reset	0x000000	u	u	0	0	1	0	0	u	u
WDT Wake-up	PC + 2	u	u	u	u	1	u	1	u	u
Interrupt Wake-up from Sleep	PC + 2(1)	u	u	u	u	u	u	1	u	u
Clock Failure Trap	0x000004	u	u	u	u	u	u	u	u	u
Trap Reset	0x000000	1	u	u	u	u	u	u	u	u
Illegal Operation Reset	0x000000	u	1	u	u	u	u	u	u	u

Legend: u = unchanged

Note 1: When the wake-up is due to an enabled interrupt, the PC is loaded with the corresponding interrupt vector.

TABLE 18-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
9	BTG	`BTG f,#bit4`	Bit Toggle f	1	1	None
		`BTG Ws,#bit4`	Bit Toggle Ws	1	1	None
10	BTSC	`BTSC f,#bit4`	Bit Test f, Skip if Clear	1	1 (2 or 3)	None
		`BTSC Ws,#bit4`	Bit Test Ws, Skip if Clear	1	1 (2 or 3)	None
11	BTSS	`BTSS f,#bit4`	Bit Test f, Skip if Set	1	1 (2 or 3)	None
		`BTSS Ws,#bit4`	Bit Test Ws, Skip if Set	1	1 (2 or 3)	None
12	BTST	`BTST f,#bit4`	Bit Test f	1	1	Z
		`BTST.C Ws,#bit4`	Bit Test Ws to C	1	1	C
		`BTST.Z Ws,#bit4`	Bit Test Ws to Z	1	1	Z
		`BTST.C Ws,Wb`	Bit Test Ws<Wb> to C	1	1	C
		`BTST.Z Ws,Wb`	Bit Test Ws<Wb> to Z	1	1	Z
13	BTSTS	`BTSTS f,#bit4`	Bit Test then Set f	1	1	Z
		`BTSTS.C Ws,#bit4`	Bit Test Ws to C, then Set	1	1	C
		`BTSTS.Z Ws,#bit4`	Bit Test Ws to Z, then Set	1	1	Z
14	CALL	`CALL lit23`	Call subroutine	2	2	None
		`CALL Wn`	Call indirect subroutine	1	2	None
15	CLR	`CLR f`	f = 0x0000	1	1	None
		`CLR WREG`	WREG = 0x0000	1	1	None
		`CLR Ws`	Ws = 0x0000	1	1	None
		`CLR Acc,Wx,Wxd,Wy,Wyd,AWB`	Clear Accumulator	1	1	OA,OB,SA,SB
16	CLRWDT	`CLRWDT`	Clear Watchdog Timer	1	1	WDTO,Sleep
17	COM	`COM f`	f = $\overline{f}$	1	1	N,Z
		`COM f,WREG`	WREG = $\overline{f}$	1	1	N,Z
		`COM Ws,Wd`	Wd = $\overline{Ws}$	1	1	N,Z
18	CP	`CP f`	Compare f with WREG	1	1	C,DC,N,OV,Z
		`CP Wb,#lit5`	Compare Wb with lit5	1	1	C,DC,N,OV,Z
		`CP Wb,Ws`	Compare Wb with Ws (Wb - Ws)	1	1	C,DC,N,OV,Z
19	CP0	`CP0 f`	Compare f with 0x0000	1	1	C,DC,N,OV,Z
		`CP0 Ws`	Compare Ws with 0x0000	1	1	C,DC,N,OV,Z
20	CPB	`CPB f`	Compare f with WREG, with Borrow	1	1	C,DC,N,OV,Z
		`CPB Wb,#lit5`	Compare Wb with lit5, with Borrow	1	1	C,DC,N,OV,Z
		`CPB Wb,Ws`	Compare Wb with Ws, with Borrow (Wb - Ws - $\overline{C}$)	1	1	C,DC,N,OV,Z
21	CPSEQ	`CPSEQ Wb, Wn`	Compare Wb with Wn, skip if =	1	1 (2 or 3)	None
22	CPSGT	`CPSGT Wb, Wn`	Compare Wb with Wn, skip if >	1	1 (2 or 3)	None
23	CPSLT	`CPSLT Wb, Wn`	Compare Wb with Wn, skip if <	1	1 (2 or 3)	None
24	CPSNE	`CPSNE Wb, Wn`	Compare Wb with Wn, skip if ≠	1	1 (2 or 3)	None
25	DAW	`DAW Wn`	Wn = decimal adjust Wn	1	1	C
26	DEC	`DEC f`	f = f -1	1	1	C,DC,N,OV,Z
		`DEC f,WREG`	WREG = f -1	1	1	C,DC,N,OV,Z
		`DEC Ws,Wd`	Wd = Ws - 1	1	1	C,DC,N,OV,Z
27	DEC2	`DEC2 f`	f = f -2	1	1	C,DC,N,OV,Z
		`DEC2 f,WREG`	WREG = f -2	1	1	C,DC,N,OV,Z
		`DEC2 Ws,Wd`	Wd = Ws - 2	1	1	C,DC,N,OV,Z
28	DISI	`DISI #lit14`	Disable Interrupts for k instruction cycles	1	1	None

FIGURE 20-1: LOW-VOLTAGE DETECT CHARACTERISTICS

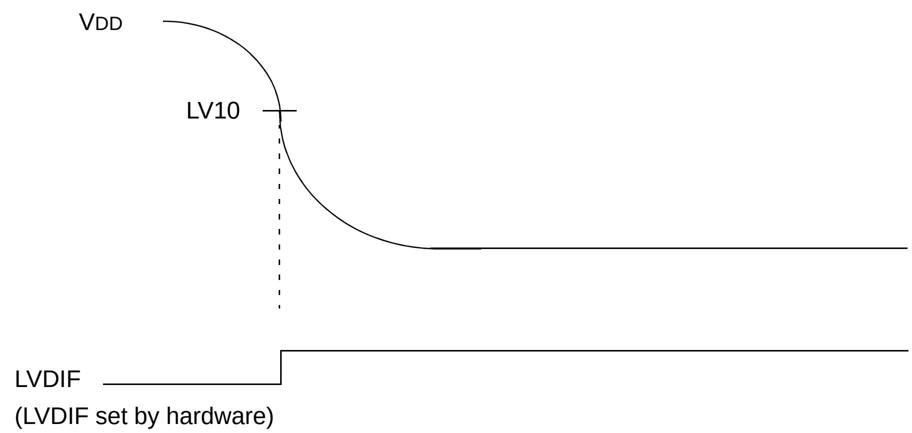


TABLE 20-10: ELECTRICAL CHARACTERISTICS: LVDL

DC CHARACTERISTICS				Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended				
Param No.	**Symbol**	**Characteristic[1]**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
LV10	VPLVD	LVDL Voltage on VDD transition high-to-low	LVDL = `0000`[2]	—	—	—	V	
			LVDL = `0001`[2]	—	—	—	V	
			LVDL = `0010`[2]	—	—	—	V	
			LVDL = `0011`[2]	—	—	—	V	
			LVDL = `0100`	2.50	—	2.65	V	
			LVDL = `0101`	2.70	—	2.86	V	
			LVDL = `0110`	2.80	—	2.97	V	
			LVDL = `0111`	3.00	—	3.18	V	
			LVDL = `1000`	3.30	—	3.50	V	
			LVDL = `1001`	3.50	—	3.71	V	
			LVDL = `1010`	3.60	—	3.82	V	
			LVDL = `1011`	3.80	—	4.03	V	
			LVDL = `1100`	4.00	—	4.24	V	
			LVDL = `1101`	4.20	—	4.45	V	
			LVDL = `1110`	4.50	—	4.77	V	
LV15	VLVDIN	External LVD input pin threshold voltage	LVDL = `1111`	—	—	—	V	

Note 1: These parameters are characterized but not tested in manufacturing.
2: These values not in usable operating range.

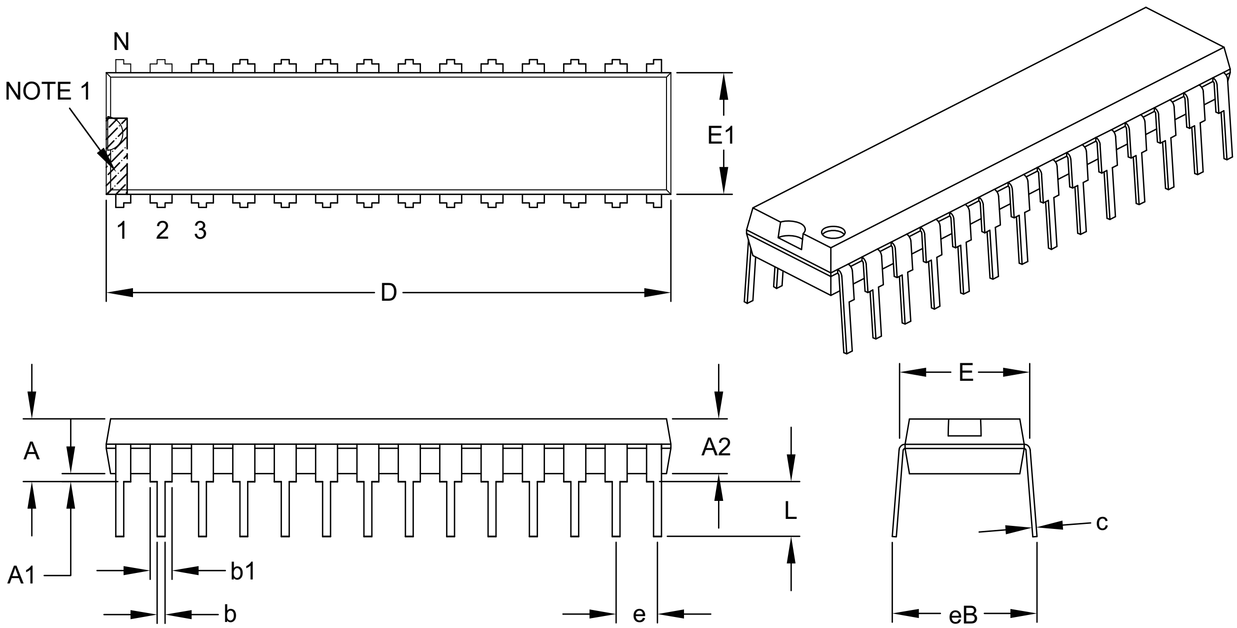
TABLE 20-12: DC CHARACTERISTICS: PROGRAM AND EEPROM

DC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
		Data EEPROM Memory(2)					
D120	E_D	Byte Endurance	100K	1M	—	E/W	-40° C ≤TA ≤+85°C
D121	V_{DRW}	V_{DD} for Read/Write	V_{MIN}	—	5.5	V	Using EECON to Read/Write V_{MIN} = Minimum operating voltage
D122	T_{DEW}	Erase/Write Cycle Time	0.8	2	2.6	ms	RTSP
D123	T_{RETD}	Characteristic Retention	40	100	—	Year	Provided no other specifications are violated
D124	I_{DEW}	I_{DD} During Programming	—	10	30	mA	Row Erase
		Program Flash Memory(2)					
D130	E_P	Cell Endurance	10K	100K	—	E/W	-40° C ≤TA ≤+85°C
D131	V_{PR}	V_{DD} for Read	V_{MIN}	—	5.5	V	V_{MIN} = Minimum operating voltage
D132	V_{EB}	V_{DD} for Bulk Erase	4.5	—	5.5	V	
D133	V_{PEW}	V_{DD} for Erase/Write	3.0	—	5.5	V	
D134	T_{PEW}	Erase/Write Cycle Time	0.8	2	2.6	ms	RTSP
D135	T_{RETD}	Characteristic Retention	40	100	—	Year	Provided no other specifications are violated
D137	I_{PEW}	I_{DD} During Programming	—	10	30	mA	Row Erase
D138	I_{EB}	I_{DD} During Programming	—	10	30	mA	Bulk Erase

Note 1: Data in “Typ” column is at 5V, 25°C unless otherwise stated.
2: These parameters are characterized but not tested in manufacturing.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B