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Details

E·XF

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	20 MIPS
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	12KB (4K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic30f2011-20e-so

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2.4.2.4 Data Space Write Saturation

In addition to adder/subtracter saturation, writes to data space may also be saturated but without affecting the contents of the source accumulator. The data space write saturation logic block accepts a 16-bit, 1.15 fractional value from the round logic block as its input, together with overflow status from the original source (accumulator) and the 16-bit round adder. These are combined and used to select the appropriate 1.15 fractional value as output to write to data space memory.

If the SATDW bit in the CORCON register is set, data (after rounding or truncation) is tested for overflow and adjusted accordingly. For input data greater than 0x007FFF, data written to memory is forced to the maximum positive 1.15 value, 0x7FFF. For input data less than 0xFF8000, data written to memory is forced to the maximum negative 1.15 value, 0x8000. The MSb of the source (bit 39) is used to determine the sign of the operand being tested.

If the SATDW bit in the CORCON register is not set, the input data is always passed through unmodified under all conditions.

2.4.3 BARREL SHIFTER

The barrel shifter is capable of performing up to 16-bit arithmetic or logic right shifts, or up to 16-bit left shifts in a single cycle. The source can be either of the two DSP accumulators, or the X bus (to support multi-bit shifts of register or memory data).

The shifter requires a signed binary value to determine both the magnitude (number of bits) and direction of the shift operation. A positive value shifts the operand right. A negative value shifts the operand left. A value of '0' does not modify the operand.

The barrel shifter is 40 bits wide, thereby obtaining a 40-bit result for DSP shift operations and a 16-bit result for MCU shift operations. Data from the X bus is presented to the barrel shifter between bit positions 16 to 31 for right shifts, and bit positions 0 to 16 for left shifts.

3.1.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

This architecture fetches 24-bit wide program memory. Consequently, instructions are always aligned. However, as the architecture is modified Harvard, data can also be present in program space.

There are two methods by which program space can be accessed: via special table instructions, or through the remapping of a 16K word program space page into the upper half of data space (see Section 3.1.2 "Data Access from Program Memory Using Program Space Visibility"). The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lsw of any address within program space, without going through data space. The TBLRDH and TBLWTH instructions are the only method whereby the upper 8 bits of a program space word can be accessed as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two 16-bit word wide address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space which contains the lsw, and TBLRDH and TBLWTH access the space which contains the MSB.

Figure 3-2 shows how the EA is created for table operations and data space accesses (PSV = 1). Here, P<23:0> refers to a program space word, whereas D<15:0> refers to a data space word.

A set of table instructions are provided to move byte or word-sized data to and from program space. See Figure 3-4 and Figure 3-5.

 TBLRDL: Table Read Low Word: Read the LS Word of the program address; P<15:0> maps to D<15:0>. Byte: Read one of the LSB of the program

address; P < 7:0 > maps to the destination byte when byte select = 0;

P<15:8> maps to the destination byte when byte select = 1.

- TBLWTL: Table Write Low (refer to Section 5.0 "Flash Program Memory" for details on Flash Programming)
- TBLRDH: Table Read High Word: Read the MS Word of the program address; P<23:16> maps to D<7:0>; D<15:8> will always

B = 0.Byte: Read one of the MSB of the program

address;

P<23:16> maps to the destination byte when byte select = 0;

The destination byte will always be = 0 when byte select = 1.

 TBLWTH: Table Write High (refer to Section 5.0 "Flash Program Memory" for details on Flash Programming)

FIGURE 3-3: PROGRAM DATA TABLE ACCESS (Isw)





All byte loads into any W register are loaded into the LSB. The MSB is not modified.

A Sign-Extend (SE) instruction is provided to allow users to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, users can clear the MSB of any W register by executing a Zero-Extend (ZE) instruction on the appropriate address.

Although most instructions are capable of operating on word or byte data sizes, it should be noted that some instructions, including the DSP instructions, operate only on words.

3.2.5 NEAR DATA SPACE

An 8 Kbyte near data space is reserved in X address memory space between 0x0000 and 0x1FFF, which is directly addressable via a 13-bit absolute address field within all memory direct instructions. The remaining X address space and all of the Y address space is addressable indirectly. Additionally, the whole of X data space is addressable using MOV instructions, which support memory direct addressing with a 16-bit address field.

3.2.6 SOFTWARE STACK

The dsPIC DSC devices contain a software stack. W15 is used as the Stack Pointer.

The Stack Pointer always points to the first available free word and grows from lower addresses towards higher addresses. It pre-decrements for stack pops and post-increments for stack pushes, as shown in Figure 3-10. Note that for a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, ensuring that the MSB is always clear.

Note: A PC push during exception processing concatenates the SRL register to the MSB of the PC prior to the push.



There is a Stack Pointer Limit register (SPLIM) associated with the Stack Pointer. SPLIM is uninitialized at Reset. As is the case for the Stack Pointer, SPLIM<0> is forced to '0' because all stack operations must be word aligned. Whenever an Effective Address (EA) is generated using W15 as a source or destination pointer, the address thus generated is compared with the value in SPLIM. If the contents of the Stack Pointer (W15) and the SPLIM register are equal, and a push operation is performed, a stack error trap does not occur. The stack error trap occurs on a subsequent push operation. Thus, for example, if it is desirable to cause a stack error trap when the stack grows beyond address 0x2000 in RAM, initialize the SPLIM with the value, 0x1FFE.

Similarly, a Stack Pointer underflow (stack error) trap is generated when the Stack Pointer address is found to be less than 0x0800, thus preventing the stack from interfering with the Special Function Register (SFR) space.

A write to the SPLIM register should not be immediately followed by an indirect read operation using W15.

NOTES:

8.0 INTERRUPTS

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "dsPIC30F Family Reference Manual" (DS70046). For more information on the device instruction set and programming, refer to the "16-bit MCU and DSC Programmer's Reference Manual" (DS70157).

The dsPIC30F sensor family has up to 21 interrupt sources and 4 processor exceptions (traps) which must be arbitrated based on a priority scheme.

The CPU is responsible for reading the Interrupt Vector Table (IVT) and transferring the address contained in the interrupt vector to the program counter. The interrupt vector is transferred from the program data bus into the program counter via a 24-bit wide multiplexer on the input of the program counter.

The Interrupt Vector Table (IVT) and Alternate Interrupt Vector Table (AIVT) are placed near the beginning of program memory (0x000004). The IVT and AIVT are shown in Figure 8-1.

The interrupt controller is responsible for pre-processing the interrupts and processor exceptions before they are presented to the processor core. The peripheral interrupts and traps are enabled, prioritized and controlled using centralized Special Function Registers (SFRs):

- IFS0<15:0>, IFS1<15:0>, IFS2<15:0> All interrupt request flags are maintained in these three registers. The flags are set by their respective peripherals or external signals and they are cleared via software.
- IEC0<15:0>, IEC1<15:0>, IEC2<15:0> All interrupt enable control bits are maintained in these three registers. These control bits are used to individually enable interrupts from the peripherals or external signals.
- IPC0<15:0> through IPC10<7:0> The user assignable priority level associated with each of these 41 interrupts is held centrally in these eleven registers.
- IPL<3:0> The current CPU priority level is explicitly stored in the IPL bits. IPL<3> is present in the CORCON register, whereas IPL<2:0> are present in the STATUS register (SR) in the processor core.

- INTCON1<15:0>, INTCON2<15:0> Global interrupt control functions are derived from these two registers. INTCON1 contains the control and status flags for the processor exceptions. The INTCON2 register controls the external interrupt request signal behavior and the use of the alternate vector table.
 - Note: Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

All interrupt sources can be user assigned to one of 7 priority levels, 1 through 7, through the IPCx registers. Each interrupt source is associated with an interrupt vector, as shown in Table 8-1. Levels 7 and 1 represent the highest and lowest maskable priorities, respectively.

Note: Assigning a priority level of '0' to an interrupt source is equivalent to disabling that interrupt.

If the NSTDIS bit (INTCON1<15>) is set, nesting of interrupts is prevented. Thus, if an interrupt is currently being serviced, processing of a new interrupt is prevented even if the new interrupt is of higher priority than the one currently being serviced.

Note: The IPL bits become read-only whenever the NSTDIS bit has been set to '1'.

Certain interrupts have specialized control bits for features like edge or level triggered interrupts, interrupt-on-change, etc. Control of these features remains within the peripheral module which generates the interrupt.

The DISI instruction can be used to disable the processing of interrupts of priorities 6 and lower for a certain number of instructions, during which the DISI bit (INTCON2<14>) remains set.

When an interrupt is serviced, the PC is loaded with the address stored in the vector location in program memory that corresponds to the interrupt. There are 63 different vectors within the IVT (refer to Table 8-1). These vectors are contained in locations 0x000004 through 0x0000FE of program memory (refer to Table 8-1). These locations contain 24-bit addresses, and in order to preserve robustness, an address error trap takes place if the PC attempts to fetch any of these words during normal execution. This prevents execution of random data as a result of accidentally decrementing a PC into vector space, accidentally mapping a data space address into vector space, or the PC rolling over to 0x000000 after reaching the end of implemented program memory space. Execution of a GOTO instruction to this vector space also generates an address error trap.

8.6 Fast Context Saving

A context saving option is available using shadow registers. Shadow registers are provided for the DC, N, OV, Z and C bits in SR, and the registers W0 through W3. The shadows are only one level deep. The shadow registers are accessible using the PUSH.S and POP.S instructions only.

When the processor vectors to an interrupt, the PUSH.S instruction can be used to store the current value of the aforementioned registers into their respective shadow registers.

If an ISR of a certain priority uses the PUSH.S and POP.S instructions for fast context saving, then a higher priority ISR should not include the same instructions. Users must save the key registers in software during a lower priority interrupt if the higher priority ISR uses fast context saving.

8.7 External Interrupt Requests

The interrupt controller supports three external interrupt request signals, INT0-INT2. These inputs are edge sensitive; they require a low-to-high or a high-to-low transition to generate an interrupt request. The INTCON2 register has three bits, INT0EP-INT2EP, that select the polarity of the edge detection circuitry.

8.8 Wake-up from Sleep and Idle

The interrupt controller may be used to wake-up the processor from either Sleep or Idle modes, if Sleep or Idle mode is active when the interrupt is generated.

If an enabled interrupt request of sufficient priority is received by the interrupt controller, then the standard interrupt request is presented to the processor. At the same time, the processor wakes up from Sleep or Idle and begins execution of the ISR needed to process the interrupt request. Enabling an interrupt is accomplished via the respective timer interrupt enable bit, T1IE. The timer interrupt enable bit is located in the IEC0 Control register in the interrupt controller.

16.9 Module Power-Down Modes

The module has two internal power modes.

When the ADON bit is '1', the module is in Active mode; it is fully powered and functional.

When ADON is '0', the module is in Off mode. The digital and analog portions of the circuit are disabled for maximum current savings.

In order to return to the Active mode from Off mode, the user must wait for the ADC circuitry to stabilize.

16.10 A/D Operation During CPU Sleep and Idle Modes

16.10.1 A/D OPERATION DURING CPU SLEEP MODE

When the device enters Sleep mode, all clock sources to the module are shut down and stay at logic '0'.

If Sleep occurs in the middle of a conversion, the conversion is aborted. The converter will not continue with a partially completed conversion on exit from Sleep mode.

Register contents are not affected by the device entering or leaving Sleep mode.

The ADC module can operate during Sleep mode if the A/D clock source is set to RC (ADRC = 1). When the RC clock source is selected, the ADC module waits one instruction cycle before starting the conversion. This allows the SLEEP instruction to be executed which eliminates all digital switching noise from the conversion. When the conversion is complete, the CONV bit will be cleared and the result loaded into the ADCBUF register.

If the A/D interrupt is enabled, the device will wake-up from Sleep. If the A/D interrupt is not enabled, the ADC module will then be turned off, although the ADON bit will remain set.

16.10.2 A/D OPERATION DURING CPU IDLE MODE

The ADSIDL bit selects if the module will stop on Idle or continue on Idle. If ADSIDL = 0, the module will continue operation on assertion of Idle mode. If ADSIDL = 1, the module will stop on Idle.

16.11 Effects of a Reset

A device Reset forces all registers to their Reset state. This forces the ADC module to be turned off, and any conversion and sampling sequence is aborted. The values that are in the ADCBUF registers are not modified. The A/D Result register will contain unknown data after a Power-on Reset.

16.12 Output Formats

The A/D result is 12 bits wide. The data buffer RAM is also 12 bits wide. The 12-bit data can be read in one of four different formats. The FORM<1:0> bits select the format. Each of the output formats translates to a 16-bit result on the data bus.

FIGURE 16-4	A/D OUTPUT DATA	FORMATS

RAM Contents:		d11	d10	d09	d08	d07	d06	d05	d04	d03	d02	d01	d00
Read to Bus:													
Signed Fractional	d11 d10 d09 d08	d07	d06	d05	d04	d03	d02	d01	d00	0	0	0	0
Fractional	d11 d10 d09 d08	d07	d06	d05	d04	d03	d02	d01	d00	0	0	0	0
													II
Signed Integer	d11 d11 d11 d11	d11	d10	d09	d08	d07	d06	d05	d04	d03	d02	d01	d00
			1										
Integer	0 0 0 0	d11	d10	d09	d08	d07	d06	d05	d04	d03	d02	d01	d00
		1											11

17.2.7 FAIL-SAFE CLOCK MONITOR

The Fail-Safe Clock Monitor (FSCM) allows the device to continue to operate even in the event of an oscillator failure. The FSCM function is enabled by appropriately programming the FCKSM Configuration bits (clock switch and monitor selection bits) in the FOSC Device Configuration register. If the FSCM function is enabled, the LPRC internal oscillator will run at all times (except during Sleep mode) and will not be subject to control by the SWDTEN bit.

In the event of an oscillator failure, the FSCM will generate a clock failure trap event and will switch the system clock over to the FRC oscillator. The user will then have the option to either attempt to restart the oscillator or execute a controlled shutdown. The user may decide to treat the trap as a warm Reset by simply loading the Reset address into the oscillator fail trap vector. In this event, the CF (Clock Fail) bit (OSCCON<3>) is also set whenever a clock failure is recognized.

In the event of a clock failure, the WDT is unaffected and continues to run on the LPRC clock.

If the oscillator has a very slow start-up time coming out of POR, BOR or Sleep, it is possible that the PWRT timer will expire before the oscillator has started. In such cases, the FSCM will be activated and the FSCM will initiate a clock failure trap, and the COSC<2:0> bits are loaded with FRC oscillator selection. This will effectively shut-off the original oscillator that was trying to start.

The user may detect this situation and restart the oscillator in the clock fail trap ISR.

Upon a clock failure detection, the FSCM module will initiate a clock switch to the FRC oscillator as follows:

- 1. The COSC bits (OSCCON<14:12>) are loaded with the FRC oscillator selection value.
- 2. CF bit is set (OSCCON<3>).
- 3. OSWEN control bit (OSCCON<0>) is cleared.

For the purpose of clock switching, the clock sources are sectioned into four groups:

- Primary (with or without PLL)
- Secondary
- Internal FRC
- Internal LPRC

The user can switch between these functional groups but cannot switch between options within a group. If the primary group is selected, then the choice within the group is always determined by the FPR<4:0> Configuration bits. The OSCCON register holds the Control and Status bits related to clock switching.

- COSC<2:0>: Read-only bits always reflect the current oscillator group in effect.
- NOSC<2:0>: Control bits which are written to indicate the new oscillator group of choice.
 - On POR and BOR, COSC<2:0> and NOSC<2:0> are both loaded with the Configuration bit values FOS<2:0>.
- LOCK: The LOCK bit indicates a PLL lock.
- CF: Read-only bit indicating if a clock fail detect has occurred.
- OSWEN: Control bit changes from a '0' to a '1' when a clock transition sequence is initiated. Clearing the OSWEN control bit will abort a clock transition in progress (used for hang-up situations).

If Configuration bits FCKSM<1:0> = 1x, then the clock switching and Fail-Safe Clock monitoring functions are disabled. This is the default Configuration bit setting.

If clock switching is disabled, then the FOS<2:0> and FPR<4:0> bits directly control the oscillator selection and the COSC<2:0> bits do not control the clock selection. However, these bits will reflect the clock source selection.

Note: The application should not attempt to switch to a clock of frequency lower than 100 kHz when the Fail-Safe Clock Monitor is enabled. If such clock switching is performed, the device may generate an oscillator fail trap and switch to the Fast RC oscillator.

17.2.8 PROTECTION AGAINST ACCIDENTAL WRITES TO OSCCON

A write to the OSCCON register is intentionally made difficult because it controls clock switching and clock scaling.

To write to the OSCCON low byte, the following code sequence must be executed without any other instructions in between:

Byte Write 0x46 to OSCCON low Byte Write 0x57 to OSCCON low

Byte write is allowed for one instruction cycle. Write the desired value or use bit manipulation instruction.

To write to the OSCCON high byte, the following instructions must be executed without any other instructions in between:

Byte Write 0x78 to OSCCON high Byte Write 0x9A to OSCCON high

Byte write is allowed for one instruction cycle. Write the desired value or use bit manipulation instruction.

Table 17-5 shows the Reset conditions for the RCON register. Since the control bits within the RCON register are R/W, the information in the table means that all the bits are negated prior to the action specified in the condition column.

Condition	Program Counter	TRAPR	IOPUWR	EXTR	SWR	WDTO	IDLE	SLEEP	POR	BOR
Power-on Reset	0x000000	0	0	0	0	0	0	0	1	1
Brown-out Reset	0x000000	0	0	0	0	0	0	0	0	1
MCLR Reset during normal operation	0x000000	0	0	1	0	0	0	0	0	0
Software Reset during normal operation	0x000000	0	0	0	1	0	0	0	0	0
MCLR Reset during Sleep	0x000000	0	0	1	0	0	0	1	0	0
MCLR Reset during Idle	0x000000	0	0	1	0	0	1	0	0	0
WDT Time-out Reset	0x000000	0	0	0	0	1	0	0	0	0
WDT Wake-up	PC + 2	0	0	0	0	1	0	1	0	0
Interrupt Wake-up from Sleep	PC + 2 ⁽¹⁾	0	0	0	0	0	0	1	0	0
Clock Failure Trap	0x000004	0	0	0	0	0	0	0	0	0
Trap Reset	0x000000	1	0	0	0	0	0	0	0	0
Illegal Operation Trap	0x000000	0	1	0	0	0	0	0	0	0

TABLE 17-5: INITIALIZATION CONDITION FOR RCON REGISTER: CASE 1

Note 1: When the wake-up is due to an enabled interrupt, the PC is loaded with the corresponding interrupt vector.

Table 17-6 shows a second example of the bit conditions for the RCON register. In this case, it is not assumed the user has set/cleared specific bits prior to action specified in the condition column.

TABLE 17-6: INITIALIZATION CONDITION FOR RCON REGISTER: CASE 2

Condition	Program Counter	TRAPR	IOPUWR	EXTR	SWR	WDTO	IDLE	SLEEP	POR	BOR
Power-on Reset	0x000000	0	0	0	0	0	0	0	1	1
Brown-out Reset	0x000000	u	u	u	u	u	u	u	0	1
MCLR Reset during normal operation	0x000000	u	u	1	0	0	0	0	u	u
Software Reset during normal operation	0x000000	u	u	0	1	0	0	0	u	u
MCLR Reset during Sleep	0x000000	u	u	1	u	0	0	1	u	u
MCLR Reset during Idle	0x000000	u	u	1	u	0	1	0	u	u
WDT Time-out Reset	0x000000	u	u	0	0	1	0	0	u	u
WDT Wake-up	PC + 2	u	u	u	u	1	u	1	u	u
Interrupt Wake-up from Sleep	PC + 2 ⁽¹⁾	u	u	u	u	u	u	1	u	u
Clock Failure Trap	0x000004	u	u	u	u	u	u	u	u	u
Trap Reset	0x000000	1	u	u	u	u	u	u	u	u
Illegal Operation Reset	0x000000	u	1	u	u	u	u	u	u	u

Legend: u = unchanged

Note 1: When the wake-up is due to an enabled interrupt, the PC is loaded with the corresponding interrupt vector.

TABLE 18-2: INSTRUCTION SET OVERVIEW

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycle s	Status Flags Affected
1	ADD	ADD	Acc	Add Accumulators	1	1	OA,OB,SA,SB
		ADD	f	f = f + WREG	1	1	C,DC,N,OV,Z
		ADD	f,WREG	WREG = f + WREG	1	1	C,DC,N,OV,Z
		ADD	#lit10,Wn	Wd = lit10 + Wd	1	1	C,DC,N,OV,Z
		ADD	Wb,Ws,Wd	Wd = Wb + Ws	1	1	C,DC,N,OV,Z
		ADD	Wb,#lit5,Wd	Wd = Wb + lit5	1	1	C,DC,N,OV,Z
		ADD	Wso,#Slit4,Acc	16-bit Signed Add to Accumulator	1	1	OA,OB,SA,SB
2	ADDC	ADDC	f	f = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	f,WREG	WREG = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	#lit10,Wn	Wd = lit10 + Wd + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1	C,DC,N,OV,Z
3	AND	AND	f	f = f .AND. WREG	1	1	N,Z
		AND	f,WREG	WREG = f .AND. WREG	1	1	N,Z
		AND	#lit10,Wn	Wd = lit10 .AND. Wd	1	1	N,Z
		AND	Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1	N,Z
		AND	Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1	N,Z
4	ASR	ASR	f	f = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	f,WREG	WREG = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	Ws,Wd	Wd = Arithmetic Right Shift Ws	1	1	C,N,OV,Z
		ASR	Wb,Wns,Wnd	Wnd = Arithmetic Right Shift Wb by Wns	1	1	N,Z
		ASR	Wb,#lit5,Wnd	Wnd = Arithmetic Right Shift Wb by lit5	1	1	N,Z
5	BCLR	BCLR	f,#bit4	Bit Clear f	1	1	None
		BCLR	Ws,#bit4	Bit Clear Ws	1	1	None
6	BRA	BRA	C,Expr	Branch if Carry	1	1 (2)	None
		BRA	GE, Expr	Branch if greater than or equal	1	1 (2)	None
		BRA	GEU, Expr	Branch if unsigned greater than or equal	1	1 (2)	None
		BRA	GT, Expr	Branch if greater than	1	1 (2)	None
		BRA	GTU, Expr	Branch if unsigned greater than	1	1 (2)	None
		BRA	LE,Expr	Branch if less than or equal	1	1 (2)	None
		BRA	LEU, Expr	Branch if unsigned less than or equal	1	1 (2)	None
		BRA	LT,Expr	Branch if less than	1	1 (2)	None
		BRA	LTU, Expr	Branch if unsigned less than	1	1 (2)	None
		BRA	N,Expr	Branch if Negative	1	1 (2)	None
		BRA	NC,Expr	Branch if Not Carry	1	1 (2)	None
		BRA	NN,Expr	Branch if Not Negative	1	1 (2)	None
		BRA	NOV, Expr	Branch if Not Overflow	1	1 (2)	None
		BRA	NZ,Expr	Branch if Not Zero	1	1 (2)	None
		BRA	OA,Expr	Branch if Accumulator A overflow	1	1 (2)	None
		BRA	OB,Expr	Branch if Accumulator B overflow	1	1 (2)	None
		BRA	OV,Expr	Branch if Overflow	1	1 (2)	None
		BRA	SA, Expr	Branch if Accumulator A saturated	1	1 (2)	None
		BRA	SB, Expr	Branch if Accumulator B saturated	1	1 (2)	None
		BRA	Expr	Branch Unconditionally	1	2	None
		BRA	- Z,Expr	Branch if Zero	1	1 (2)	None
		BRA	Wn	Computed Branch	1	2	None
7	BSET	BSET	f,#bit4	Bit Set f	1	1	None
		BSET	Ws,#bit4	Bit Set Ws	1	1	None
8	BSW	BSW.C	Ws,Wb	Write C bit to Ws <wb></wb>	1	1	None
		BSW.Z	Ws,Wb	Write Z bit to Ws <wb></wb>	1	1	None

19.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC[®] DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

19.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC[®] Flash MCUs and dsPIC[®] Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with incircuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

19.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC[®] Flash microcontrollers and dsPIC[®] DSCs with the powerful, yet easyto-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

19.10 PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC[®] and dsPIC[®] Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming[™].

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

	TABLE 20-4:	DC TEMPERATURE AND VOLTAGE SPECIFICATIONS
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DC CHARACTERISTICS			Standar (unless Operation	rd Operat otherwis ng tempe	t ing Co se state rature	ndition ed) -40°C -40°C	ditions: 2.5V to 5.5V d) -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions				
Operating Voltage ⁽²⁾											
DC10	Vdd	Supply Voltage	2.5	—	5.5	V	Industrial temperature				
DC11	Vdd	Supply Voltage	3.0	—	5.5	V	Extended temperature				
DC12	Vdr	RAM Data Retention Voltage ⁽³⁾	1.75	—	—	V					
DC16	VPOR	VDD Start Voltage (to ensure internal Power-on Reset signal)		_	Vss	V					
DC17	SVDD	VDD Rise Rate (to ensure internal Power-on Reset signal)	0.05	_	—	V/ms	0-5V in 0.1 sec 0-3V in 60 ms				

Note 1: "Typ" column data is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: These parameters are characterized but not tested in manufacturing.

3: This is the limit to which VDD can be lowered without losing RAM data.

FIGURE 20-5: CLKO AND I/O TIMING CHARACTERISTICS



TABLE 20-20: CLKO AND I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Ope (unless other Operating tem	rating Co vise state perature	nditions: ed) -40°C ≤⊺ -40°C ≤⊺	2.5V to Ā ≤+85°(Ā ≤+125°	5.5V C for Indu °C for Ex	ıstrial tended
Param No.	Symbol	Characteristi	Min	Typ ⁽⁴⁾	Max	Units	Conditions	
DO31	TIOR	Port output rise time	—	7	20	ns		
DO32	TIOF	Port output fall time		—	7	20	ns	
DI35	TINP	INTx pin high or low time (output)		20	_		ns	
DI40	Trbp	CNx high or low time	2 TCY		_	ns		

Note 1: These parameters are asynchronous events not related to any internal clock edges

2: Measurements are taken in RC mode and EC mode where CLKO output is 4 x Tosc.

3: These parameters are characterized but not tested in manufacturing.

4: Data in "Typ" column is at 5V, 25°C unless otherwise stated.







TABLE 20-33: I²C[™] BUS DATA TIMING REQUIREMENTS (MASTER MODE)

АС СНА	ARACTER	ISTICS		Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended						
Param No.	Symbol	Charac	teristic	Min ⁽¹⁾	Max	Units	Conditions			
IM10	TLO:SCL	Clock Low Time	100 kHz mode	Tcy/2 (BRG + 1)	_	μs				
			400 kHz mode	TCY/2 (BRG + 1)	—	μs				
			1 MHz mode ⁽²⁾	TCY/2 (BRG + 1)	_	μs				
IM11	THI:SCL	Clock High Time	100 kHz mode	TCY/2 (BRG + 1)	—	μs				
			400 kHz mode	TCY/2 (BRG + 1)	—	μs				
			1 MHz mode ⁽²⁾	TCY/2 (BRG + 1)	_	μs				
IM20	TF:SCL	SDA and SCL	100 kHz mode	—	300	ns	CB is specified to be			
		Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF			
			1 MHz mode ⁽²⁾	—	100	ns				
IM21	TR:SCL	SDA and SCL	100 kHz mode	—	1000	ns	CB is specified to be			
		Rise Time	400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF			
			1 MHz mode ⁽²⁾	—	300	ns				
IM25	TSU:DAT	Data Input	100 kHz mode	250	—	ns				
		Setup Time	400 kHz mode	100	—	ns				
			1 MHz mode ⁽²⁾	—	_	ns				
IM26	THD:DAT	Data Input	100 kHz mode	0	—	ns				
		Hold Time	400 kHz mode	0	0.9	μs				
			1 MHz mode ⁽²⁾	—	—	ns				
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TCY/2 (BRG + 1)	—	μs	Only relevant for			
			400 kHz mode	TCY/2 (BRG + 1)	—	μs	Repeated Start			
			1 MHz mode ⁽²⁾	TCY/2 (BRG + 1)	_	μs	condition			
IM31	THD:STA	Start Condition	100 kHz mode	TCY/2 (BRG + 1)	—	μs	After this period the			
		Hold Time	400 kHz mode	TCY/2 (BRG + 1)	_	μs	first clock pulse is			
			1 MHz mode ⁽²⁾	TCY/2 (BRG + 1)	_	μs	generated			
IM33	TSU:STO	Stop Condition	100 kHz mode	TCY/2 (BRG + 1)	_	μs				
		Setup Time	400 kHz mode	TCY/2 (BRG + 1)	_	μs				
			1 MHz mode ⁽²⁾	TCY/2 (BRG + 1)	—	μs				
IM34	THD:STO	Stop Condition	100 kHz mode	TCY/2 (BRG + 1)	_	ns				
		Hold Time	400 kHz mode	TCY/2 (BRG + 1)	_	ns				
			1 MHz mode ⁽²⁾	TCY/2 (BRG + 1)	_	ns				
IM40	TAA:SCL	Output Valid	100 kHz mode	—	3500	ns				
		From Clock	400 kHz mode	_	1000	ns				
			1 MHz mode ⁽²⁾	—	—	ns				
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be			
			400 kHz mode	1.3	—	μs	free before a new			
			1 MHz mode ⁽²⁾	_	μs		transmission can start			
IM50	Св	Bus Capacitive L	oading	—	400	pF				

Note 1: BRG is the value of the I²C Baud Rate Generator. Refer to Section 21. "Inter-Integrated Circuit™ (I²C)" (DS70068) in the *dsPIC30F Family Reference Manual* (DS70046).

2: Maximum pin capacitance = 10 pF for all I^2C^{TM} pins (for 1 MHz mode only).

TABLE 20-36: 12-BIT ADC MODULE SPECIFICATIONS

АС СНА	C CHARACTERISTICS			Dperatin herwise temperat	g Conditions stated) ture -40°C ≤	s: 2.5V t	o 5.5V °C for Industrial					
Param No.	Symbol	Characteristic	Min.	Тур	-40°C -	SIA ≤+12 Units	Conditions					
			Device Si	ylqqu								
AD01	AVdd	Module VDD Supply	Greater of VDD - 0.3 or 2.7	-	Lesser of VDD + 0.3 or 5.5	V						
AD02	AVss	Module Vss Supply	Vss - 0.3	_	Vss + 0.3	V						
Reference Inputs												
AD05	Vrefh	Reference Voltage High	AVss + 2.7		AVdd	V						
AD06	Vrefl	Reference Voltage Low	AVss		AVDD - 2.7	V						
AD07	Vref	Absolute Reference Voltage	AVss - 0.3	—	AVDD + 0.3	V						
AD08	IREF	Current Drain	—	200 .001	300 2	μΑ μΑ	A/D operating A/D off					
Analog Input												
AD10	VINH-VINL	Full-Scale Input Span	Vrefl	—	Vrefh	V	See Note 1					
AD11	Vin	Absolute Input Voltage	AVss - 0.3	—	AVDD + 0.3	V	—					
AD12		Leakage Current	_	±0.001	±0.610	μA	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5V Source Impedance = $2.5 \text{ k}\Omega$					
AD13	_	Leakage Current	_	±0.001	±0.610	μA	VINL = AVSS = VREFL = 0V, AVDD = VREFH = $3V$ Source Impedance = 2.5 k Ω					
AD15	Rss	Switch Resistance	—	3.2K	—	Ω						
AD16	CSAMPLE	Sample Capacitor	_	18		pF						
AD17	Rin	Recommended Impedance of Analog Voltage Source		—	2.5K	Ω						
		-	DC Accur	acy ⁽²⁾			-					
AD20	Nr	Resolution	1	2 data b	its	bits						
AD21	INL	Integral Nonlinearity	_	—	<±1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5V					
AD21A	INL	Integral Nonlinearity	—	—	<±1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V					
AD22	DNL	Differential Nonlinearity	_	_	<±1	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 5V					
AD22A	DNL	Differential Nonlinearity	—	_	<±1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V					
AD23	Gerr	Gain Error	+1.25	+1.5	+3	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5V					
AD23A	Gerr	Gain Error	+1.25	+1.5	+3	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V					

Note 1: The A/D conversion result never decreases with an increase in the input voltage, and has no missing codes.

2: Measurements taken with external VREF+ and VREF- used as the ADC voltage references.