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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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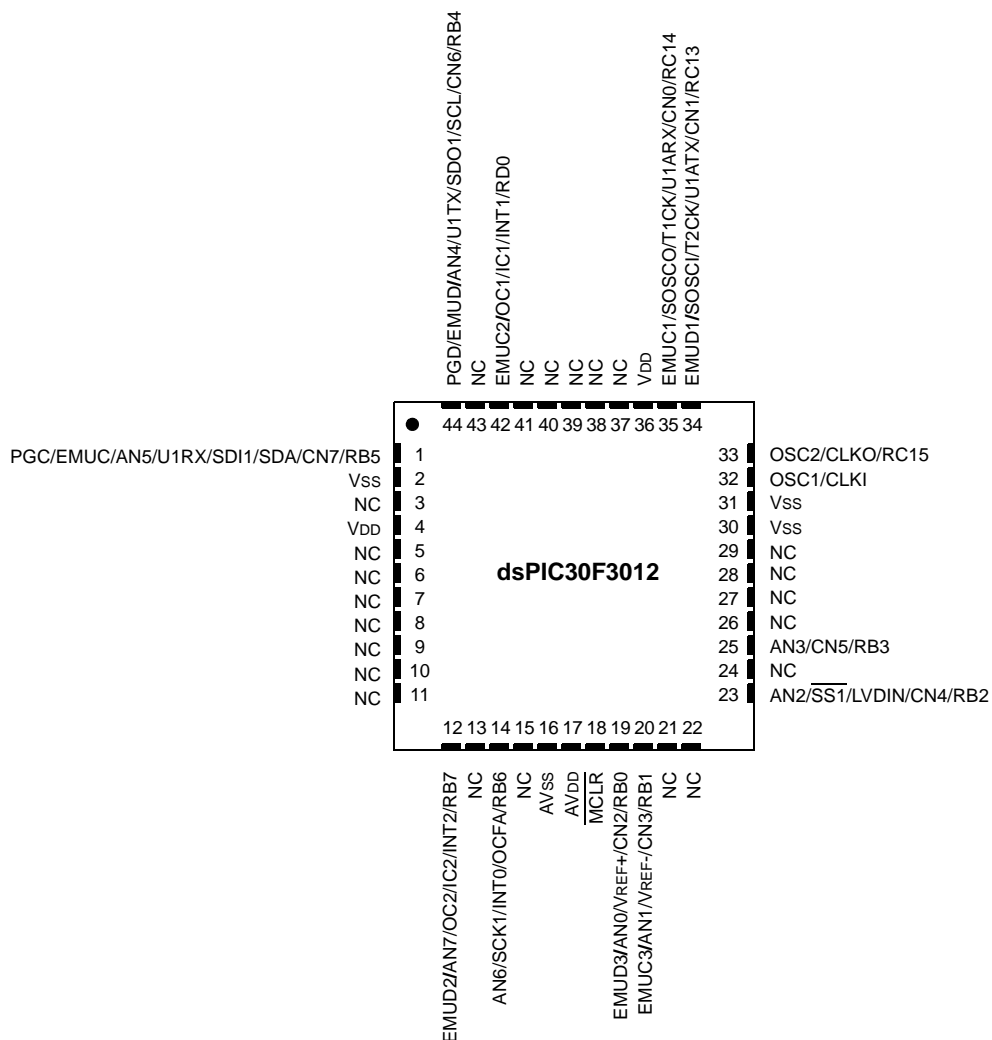
#### Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	20 MIPS
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	12KB (4K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic30f2011t-20e-so">https://www.e-xfl.com/product-detail/microchip-technology/dspic30f2011t-20e-so</a>

# dsPIC30F2011/2012/3012/3013

## Pin Diagram

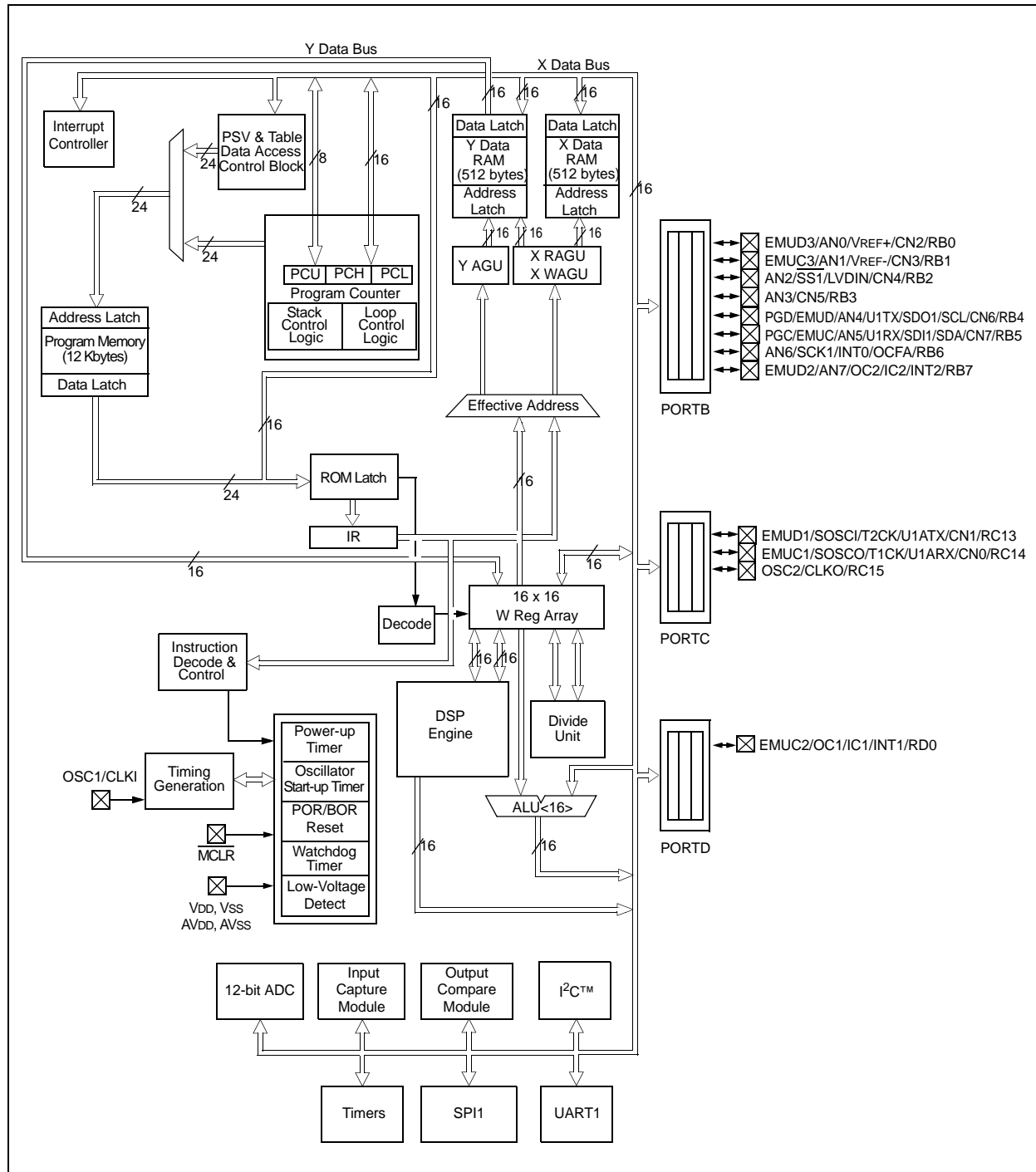
44-Pin QFN<sup>(1)</sup>



**Note 1:** The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

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**FIGURE 1-1: dsPIC30F2011 BLOCK DIAGRAM**





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**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Type	Buffer Type	Description
SCL	I/O	ST	Synchronous serial clock input/output for I <sup>2</sup> C™.
SDA	I/O	ST	Synchronous serial data input/output for I <sup>2</sup> C.
SOSCO	O	—	32 kHz low-power oscillator crystal output.
SOSCI	I	ST/CMOS	32 kHz low-power oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
T1CK	I	ST	Timer1 external clock input.
T2CK	I	ST	Timer2 external clock input.
U1RX	I	ST	UART1 Receive.
U1TX	O	—	UART1 Transmit.
U1ARX	I	ST	UART1 Alternate Receive.
U1ATX	O	—	UART1 Alternate Transmit.
U2RX	I	ST	UART2 Receive.
U2TX	O	—	UART2 Transmit.
VDD	P	—	Positive supply for logic and I/O pins.
VSS	P	—	Ground reference for logic and I/O pins.
VREF+	I	Analog	Analog Voltage Reference (High) input.
VREF-	I	Analog	Analog Voltage Reference (Low) input.

**Legend:** CMOS = CMOS compatible input or output      Analog = Analog input  
ST = Schmitt Trigger input with CMOS levels      O = Output  
I = Input      P = Power

## 2.4 DSP Engine

The DSP engine consists of a high-speed 17-bit x 17-bit multiplier, a barrel shifter and a 40-bit adder/subtractor (with two target accumulators, round and saturation logic).

The DSP engine also has the capability to perform inherent accumulator-to-accumulator operations, which require no additional data. These instructions are ADD, SUB and NEG.

The dsPIC30F is a single-cycle instruction flow architecture, therefore, concurrent operation of the DSP engine with MCU instruction flow is not possible. However, some MCU ALU and DSP engine resources may be used concurrently by the same instruction (e.g., ED, EDAC). See Table 2-2.

The DSP engine has several options selected through various bits in the CPU Core Configuration register (CORCON), which are:

1. Fractional or integer DSP multiply (IF).
2. Signed or unsigned DSP multiply (US).
3. Conventional or convergent rounding (RND).
4. Automatic saturation on/off for ACCA (SATA).
5. Automatic saturation on/off for ACCB (SATB).
6. Automatic saturation on/off for writes to data memory (SATDW).
7. Accumulator Saturation mode selection (ACCSAT).

**Note:** For CORCON layout, see Table 3-3.

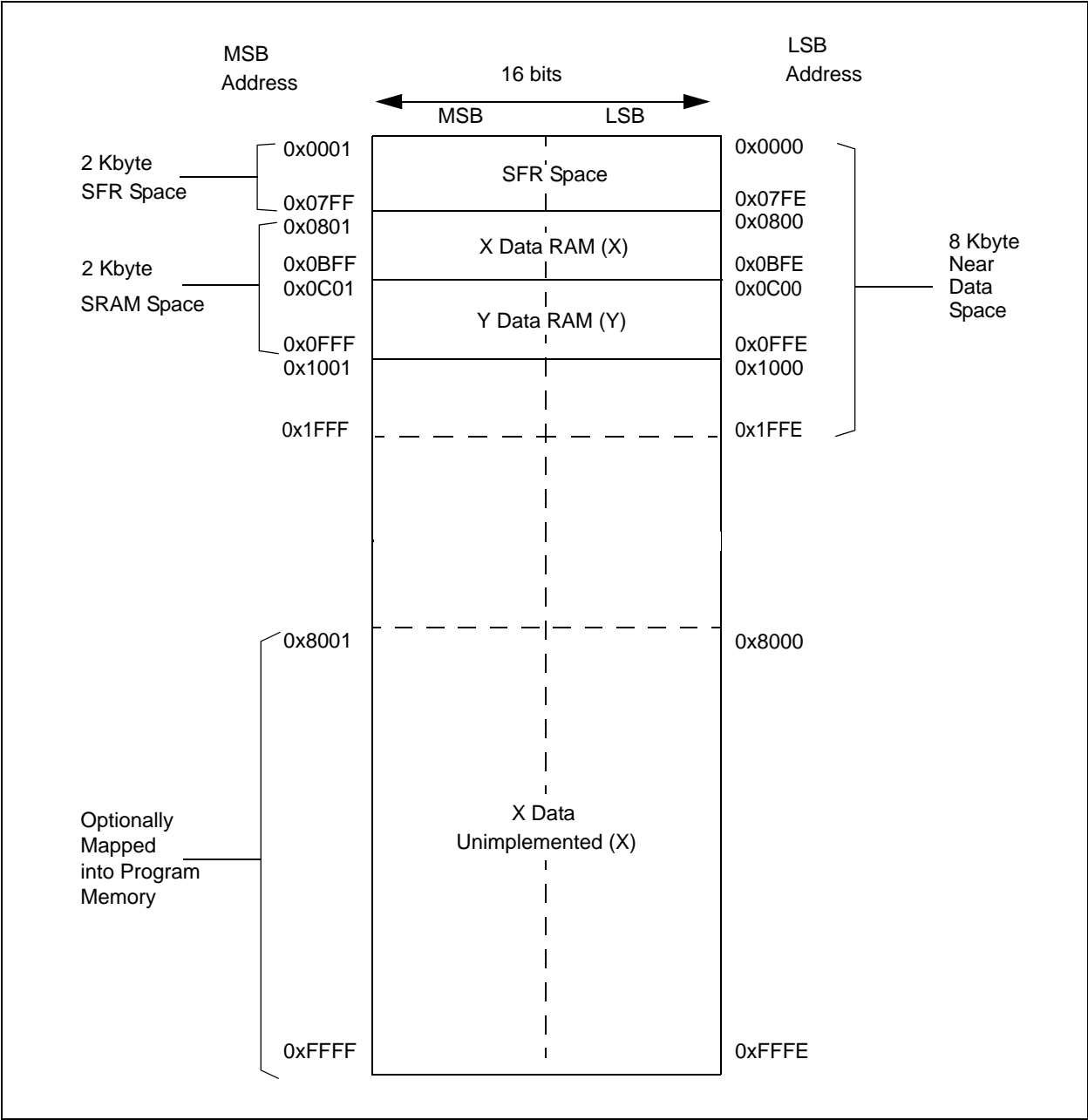
A block diagram of the DSP engine is shown in Figure 2-2.

**TABLE 2-2: DSP INSTRUCTION SUMMARY**

Instruction	Algebraic Operation	ACC WB?
CLR	$A = 0$	Yes
ED	$A = (x - y)^2$	No
EDAC	$A = A + (x - y)^2$	No
MAC	$A = A + (x * y)$	Yes
MAC	$A = A + x^2$	No
MOVSAC	No change in A	Yes
MPY	$A = x * y$	No
MPY.N	$A = -x * y$	No
MSC	$A = A - x * y$	Yes

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FIGURE 3-7: dsPIC30F3012/3013 DATA SPACE MEMORY MAP



**TABLE 3-3: CORE REGISTER MAP (CONTINUED)**

SFR Name	Address (Home)	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
CORCON	0044	—	—	—	US	EDT	DL2	DL1	DL0	SATA	SATB	SATDW	ACCSAT	IPL3	PSV	RND	IF	0000 0000 0010 0000
MODCON	0046	XMODEN	YMODEN	—	—	BWM<3:0>				YWM<3:0>				XWM<3:0>				0000 0000 0000 0000
XMODSRT	0048	XS<15:1>															0	uuuu uuuu uuuu uuu0
XMODEND	004A	XE<15:1>															1	uuuu uuuu uuuu uuu1
YMODSRT	004C	YS<15:1>															0	uuuu uuuu uuuu uuu0
YMODEND	004E	YE<15:1>															1	uuuu uuuu uuuu uuu1
XBREV	0050	BREN	XB<14:0>															uuuu uuuu uuuu uuuu
DISICNT	0052	—	—	DISICNT<13:0>														0000 0000 0000 0000

**Legend:** u = uninitialized bit; — = unimplemented bit, read as '0'

**Note:** Refer to the “dsPIC30F Family Reference Manual” (DS70046) for descriptions of register bit fields.



NOTES:

## 7.0 I/O PORTS

**Note:** This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the “dsPIC30F Family Reference Manual” (DS70046).

All of the device pins (except VDD, VSS, MCLR and OSC1/CLKI) are shared between the peripherals and the parallel I/O ports.

All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

### 7.1 Parallel I/O (PIO) Ports

When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a port.

All port pins have three registers directly associated with the operation of the port pin. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a ‘1’, then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx), read the latch.

Writes to the latch, write the latch (LATx). Reads from the port (PORTx), read the port pins and writes to the port pins, write the latch (LATx).

Any bit and its associated data and Control registers that are not valid for a particular device are disabled. That means the corresponding LATx and TRISx registers and the port pin read as zeros.

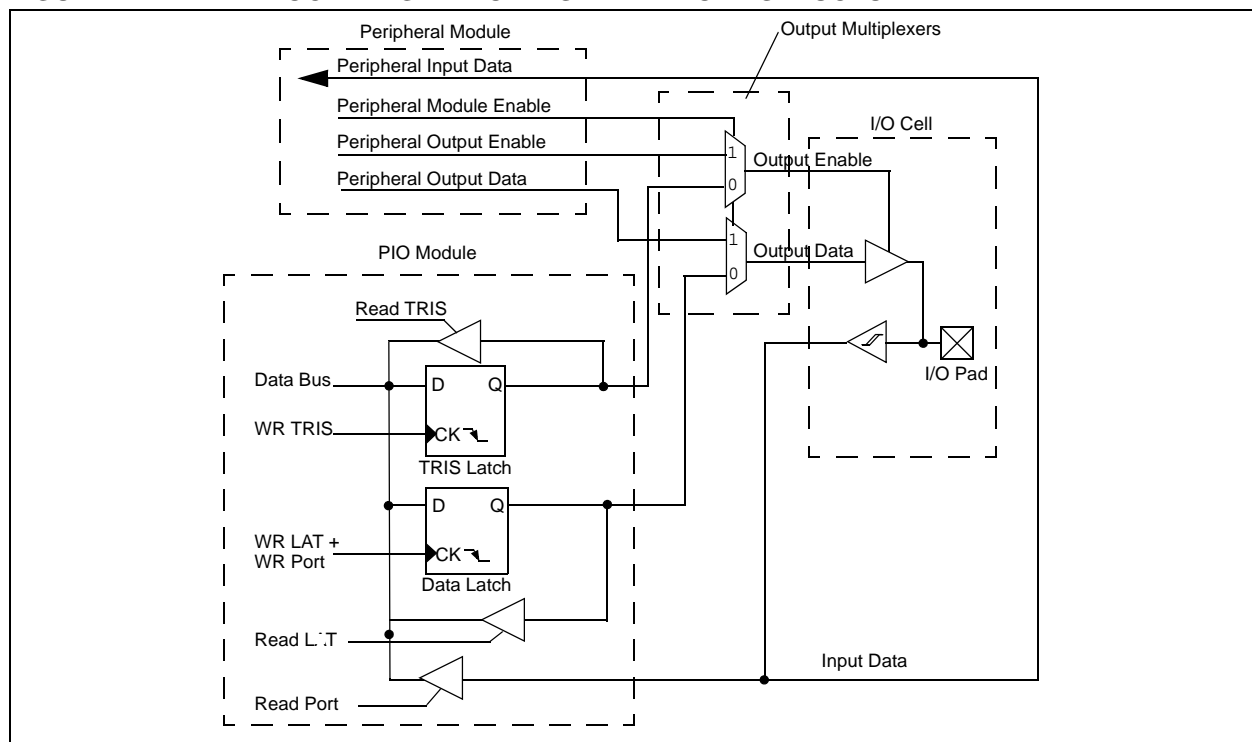
When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

A parallel I/O (PIO) port that shares a pin with a peripheral is, in general, subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pad cell. Figure 7-1 illustrates how ports are shared with other peripherals and the associated I/O cell (pad) to which they are connected.

The format of the registers for the shared ports, (PORTB, PORTC, PORTD and PORTF) are shown in Table 7-1 through Table 7-6.

**Note:** The actual bits in use vary between devices.

**FIGURE 7-1: BLOCK DIAGRAM OF A SHARED PORT STRUCTURE**



## 9.0 TIMER1 MODULE

**Note:** This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the “*dsPIC30F Family Reference Manual*” (DS70046).

This section describes the 16-bit general purpose Timer1 module and associated operational modes. Figure 9-1 depicts the simplified block diagram of the 16-bit Timer1 module. The following sections provide detailed descriptions including setup and Control registers, along with associated block diagrams for the operational modes of the timers.

The Timer1 module is a 16-bit timer that serves as the time counter for the real-time clock or operates as a free-running interval timer/counter. The 16-bit timer has the following modes:

- 16-bit Timer
- 16-bit Synchronous Counter
- 16-bit Asynchronous Counter

These operational characteristics are supported:

- Timer gate operation
- Selectable prescaler settings
- Timer operation during CPU Idle and Sleep modes
- Interrupt on 16-bit Period register match or falling edge of external gate signal

These operating modes are determined by setting the appropriate bit(s) in the 16-bit SFR, T1CON. Figure 9-1 presents a block diagram of the 16-bit timer module.

**16-bit Timer Mode:** In the 16-bit Timer mode, the timer increments on every instruction cycle up to a match value preloaded into the Period register PR1, then resets to '0' and continues to count.

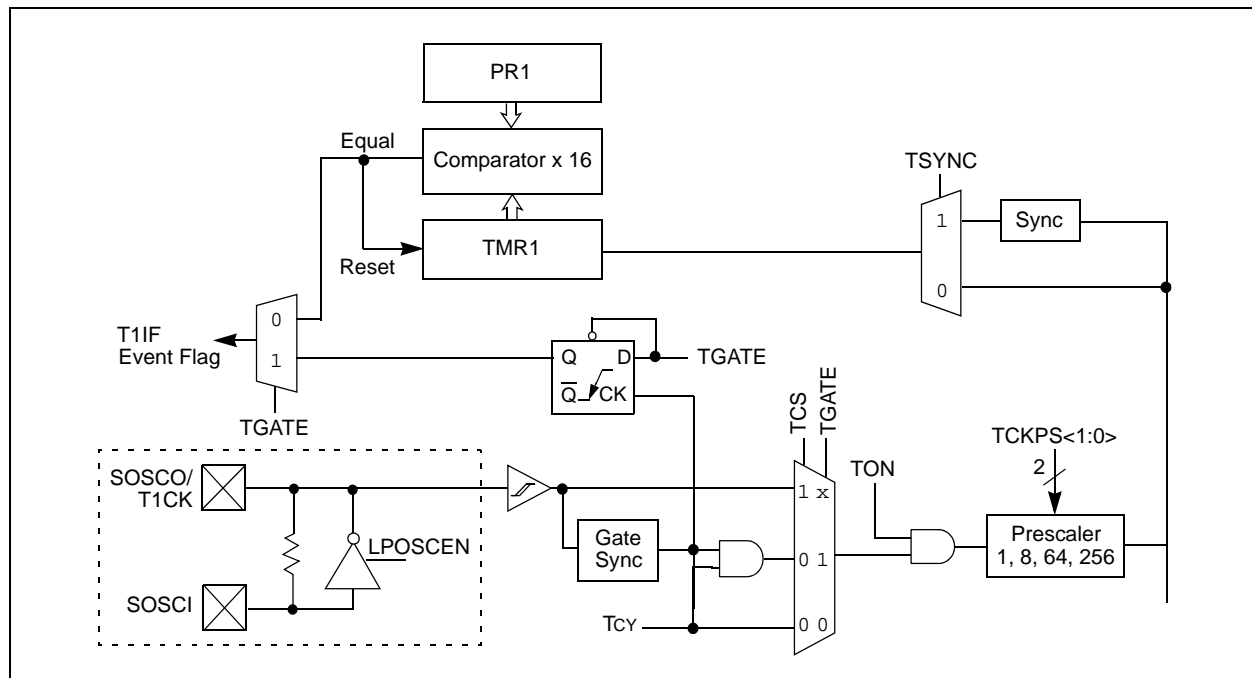
When the CPU goes into the Idle mode, the timer stops incrementing unless the TSIDL (T1CON<3>) bit = 0. If TSIDL = 1, the timer module logic resumes the incrementing sequence on termination of CPU Idle mode.

**16-bit Synchronous Counter Mode:** In the 16-bit Synchronous Counter mode, the timer increments on the rising edge of the applied external clock signal which is synchronized with the internal phase clocks. The timer counts up to a match value preloaded in PR1, then resets to '0' and continues.

When the CPU goes into the Idle mode, the timer stops incrementing unless the respective TSIDL bit = 0. If TSIDL = 1, the timer module logic resumes the incrementing sequence upon termination of the CPU Idle mode.

**16-bit Asynchronous Counter Mode:** In the 16-bit Asynchronous Counter mode, the timer increments on every rising edge of the applied external clock signal. The timer counts up to a match value preloaded in PR1, then resets to '0' and continues.

When the timer is configured for the Asynchronous mode of operation and the CPU goes into the Idle mode, the timer stops incrementing if  $TSIDL = 1$ .

**FIGURE 9-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM**

NOTES:

## 15.3.4 TRANSMIT INTERRUPT

The transmit interrupt flag (U1TXIF or U2TXIF) is located in the corresponding interrupt flag register.

The transmitter generates an edge to set the UxTXIF bit. The condition for generating the interrupt depends on the UTXISEL control bit:

- a) If UTXISEL = 0, an interrupt is generated when a word is transferred from the transmit buffer to the Transmit Shift register (UxTSR). This means that the transmit buffer has at least one empty word.
- b) If UTXISEL = 1, an interrupt is generated when a word is transferred from the transmit buffer to the Transmit Shift register (UxTSR) and the transmit buffer is empty.

Switching between the two Interrupt modes during operation is possible and sometimes offers more flexibility.

## 15.3.5 TRANSMIT BREAK

Setting the UTXBRK bit (UxSTA<11>) will cause the UxTX line to be driven to logic '0'. The UTXBRK bit overrides all transmission activity. Therefore, the user should generally wait for the transmitter to be Idle before setting UTXBRK.

To send a Break character, the UTXBRK bit must be set by software and must remain set for a minimum of 13 baud clock cycles. The UTXBRK bit is then cleared by software to generate Stop bits. The user must wait for a duration of at least one or two baud clock cycles in order to ensure a valid Stop bit(s) before reloading the UxTXB, or starting other transmitter activity. Transmission of a Break character does not generate a transmit interrupt.

## 15.4 Receiving Data

### 15.4.1 RECEIVING IN 8-BIT OR 9-BIT DATA MODE

The following steps must be performed while receiving 8-bit or 9-bit data:

1. Set up the UART (see **Section 15.3.1 "Transmitting in 8-bit data mode"**).
2. Enable the UART (see **Section 15.3.1 "Transmitting in 8-bit data mode"**).
3. A receive interrupt will be generated when one or more data words have been received, depending on the receive interrupt settings specified by the URXISEL bits (UxSTA<7:6>).
4. Read the OERR bit to determine if an overrun error has occurred. The OERR bit must be reset in software.
5. Read the received data from UxRXREG. The act of reading UxRXREG will move the next word to the top of the receive FIFO, and the PERR and FERR values will be updated.

## 15.4.2 RECEIVE BUFFER (UxRXB)

The receive buffer is 4 words deep. Including the Receive Shift register (UxRSR), the user effectively has a 5-word deep FIFO buffer.

URXDA (UxSTA<0>) = 1 indicates that the receive buffer has data available. URXDA = 0 implies that the buffer is empty. If a user attempts to read an empty buffer, the old values in the buffer will be read and no data shift will occur within the FIFO.

The FIFO is reset during any device Reset. It is not affected when the device enters or wakes up from a Power Saving mode.

### 15.4.3 RECEIVE INTERRUPT

The receive interrupt flag (U1RXIF or U2RXIF) can be read from the corresponding interrupt flag register. The interrupt flag is set by an edge generated by the receiver. The condition for setting the receive interrupt flag depends on the settings specified by the URXISEL<1:0> (UxSTA<7:6>) control bits.

- a) If URXISEL<1:0> = 00 or 01, an interrupt is generated every time a data word is transferred from the Receive Shift register (UxRSR) to the receive buffer. There may be one or more characters in the receive buffer.
- b) If URXISEL<1:0> = 10, an interrupt is generated when a word is transferred from the Receive Shift register (UxRSR) to the receive buffer, which as a result of the transfer, contains 3 characters.
- c) If URXISEL<1:0> = 11, an interrupt is set when a word is transferred from the Receive Shift register (UxRSR) to the receive buffer, which as a result of the transfer, contains 4 characters (i.e., becomes full).

Switching between the Interrupt modes during operation is possible, though generally not advisable during normal operation.

## 15.5 Reception Error Handling

### 15.5.1 RECEIVE BUFFER OVERRUN ERROR (OERR BIT)

The OERR bit (UxSTA<1>) is set if all of the following conditions occur:

- a) The receive buffer is full.
- b) The Receive Shift register is full, but unable to transfer the character to the receive buffer.
- c) The Stop bit of the character in the UxRSR is detected, indicating that the UxRSR needs to transfer the character to the buffer.

Once OERR is set, no further data is shifted in UxRSR (until the OERR bit is cleared in software or a Reset occurs). The data held in UxRSR and UxRXREG remains valid.

## 17.4 Watchdog Timer (WDT)

### 17.4.1 WATCHDOG TIMER OPERATION

The primary function of the Watchdog Timer (WDT) is to reset the processor in the event of a software malfunction. The WDT is a free-running timer which runs off an on-chip RC oscillator, requiring no external component. Therefore, the WDT timer will continue to operate even if the main processor clock (e.g., the crystal oscillator) fails.

### 17.4.2 ENABLING AND DISABLING THE WDT

The Watchdog Timer can be “Enabled” or “Disabled” only through a Configuration bit (FWDTEN) in the Configuration register, FWDTC.

Setting FWDTC = 1 enables the Watchdog Timer. The enabling is done when programming the device. By default, after chip erase, FWDTC bit = 1. Any device programmer capable of programming dsPIC30F devices allows programming of this and other Configuration bits.

If enabled, the WDT will increment until it overflows or “times out”. A WDT time-out will force a device Reset (except during Sleep). To prevent a WDT time-out, the user must clear the Watchdog Timer using a CLRWDTC instruction.

If a WDT times out during Sleep, the device will wake-up. The WDTC bit in the RCON register will be cleared to indicate a wake-up resulting from a WDT time-out.

Setting FWDTC = 0 allows user software to enable/disable the Watchdog Timer via the SWDTC (RCON<5>) control bit.

## 17.5 Low-Voltage Detect

The Low-Voltage Detect (LVD) module is used to detect when the VDD of the device drops below a threshold value, VLVD, which is determined by the LVDL<3:0> bits (RCON<11:8>) and is thus user programmable. The internal voltage reference circuitry requires a nominal amount of time to stabilize, and the BGST bit (RCON<13>) indicates when the voltage reference has stabilized.

In some devices, the LVD threshold voltage may be applied externally on the LVDIN pin.

The LVD module is enabled by setting the LVDEN bit (RCON<12>).

## 17.6 Power-Saving Modes

There are two power-saving states that can be entered through the execution of a special instruction, PWRSAV; these are Sleep and Idle.

The format of the PWRSAV instruction is as follows:

PWRSAV <parameter>, where ‘parameter’ defines Idle or Sleep mode.

### 17.6.1 SLEEP MODE

In Sleep mode, the clock to the CPU and peripherals is shut down. If an on-chip oscillator is being used, it is shut down.

The Fail-Safe Clock Monitor is not functional during Sleep since there is no clock to monitor. However, LPRC clock remains active if WDT is operational during Sleep.

The brown-out protection circuit and the Low-Voltage Detect circuit, if enabled, will remain functional during Sleep.

The processor wakes up from Sleep if at least one of the following conditions has occurred:

- any interrupt that is individually enabled and meets the required priority level
- any Reset (POR, BOR and MCLR)
- WDT time-out

On waking up from Sleep mode, the processor will restart the same clock that was active prior to entry into Sleep mode. When clock switching is enabled, bits COSC<2:0> will determine the oscillator source that will be used on wake-up. If clock switch is disabled, then there is only one system clock.

**Note:** If a POR or BOR occurred, the selection of the oscillator is based on the FOS<2:0> and FPR<4:0> Configuration bits.

If the clock source is an oscillator, the clock to the device will be held off until OST times out (indicating a stable oscillator). If PLL is used, the system clock is held off until LOCK = 1 (indicating that the PLL is stable). In either case, TPOR, TLOCK and TPWRT delays are applied.

If EC, FRC, LPRC or ERC oscillators are used, then a delay of TPOR (~ 10 µs) is applied. This is the smallest delay possible on wake-up from Sleep.

Moreover, if LP oscillator was active during Sleep and LP is the oscillator used on wake-up, then the start-up delay will be equal to TPOR. PWRT delay and OST timer delay are not applied. In order to have the smallest possible start-up delay when waking up from Sleep, one of these faster wake-up options should be selected before entering Sleep.

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**TABLE 18-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)**

Field	Description
Wb	Base W register $\in \{W0..W15\}$
Wd	Destination W register $\in \{Wd, [Wd], [Wd++] , [Wd--], [++Wd], [--Wd] \}$
Wdo	Destination W register $\in \{Wnd, [Wnd], [Wnd++] , [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] \}$
Wm,Wn	Dividend, Divisor working register pair (direct addressing)
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions $\in \{W4*W4, W5*W5, W6*W6, W7*W7\}$
Wm*Wn	Multiplicand and Multiplier working register pair for DSP instructions $\in \{W4*W5, W4*W6, W4*W7, W5*W6, W5*W7, W6*W7\}$
Wn	One of 16 working registers $\in \{W0..W15\}$
Wnd	One of 16 destination working registers $\in \{W0..W15\}$
Wns	One of 16 source working registers $\in \{W0..W15\}$
WREG	W0 (working register used in file register instructions)
Ws	Source W register $\in \{Ws, [Ws], [Ws++] , [Ws--], [++Ws], [--Ws] \}$
Wso	Source W register $\in \{Wns, [Wns], [Wns++] , [Wns--], [++Wns], [--Wns], [Wns+Wb] \}$
Wx	X data space prefetch address register for DSP instructions $\in \{[W8] += 6, [W8] += 4, [W8] += 2, [W8], [W8] -= 6, [W8] -= 4, [W8] -= 2, [W9] += 6, [W9] += 4, [W9] += 2, [W9], [W9] -= 6, [W9] -= 4, [W9] -= 2, [W9+W12], \text{none}\}$
Wxd	X data space prefetch destination register for DSP instructions $\in \{W4..W7\}$
Wy	Y data space prefetch address register for DSP instructions $\in \{[W10] += 6, [W10] += 4, [W10] += 2, [W10], [W10] -= 6, [W10] -= 4, [W10] -= 2, [W11] += 6, [W11] += 4, [W11] += 2, [W11], [W11] -= 6, [W11] -= 4, [W11] -= 2, [W11+W12], \text{none}\}$
Wyd	Y data space prefetch destination register for DSP instructions $\in \{W4..W7\}$

# dsPIC30F2011/2012/3012/3013

**TABLE 18-2: INSTRUCTION SET OVERVIEW**

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycle s	Status Flags Affected
1	ADD	ADD Acc	Add Accumulators	1	1	OA,OB,SA,SB
		ADD f	$f = f + WREG$	1	1	C,DC,N,OV,Z
		ADD f, WREG	$WREG = f + WREG$	1	1	C,DC,N,OV,Z
		ADD #lit10, Wn	$Wd = lit10 + Wd$	1	1	C,DC,N,OV,Z
		ADD Wb, Ws, Wd	$Wd = Wb + Ws$	1	1	C,DC,N,OV,Z
		ADD Wb, #lit5, Wd	$Wd = Wb + lit5$	1	1	C,DC,N,OV,Z
		ADD Wso, #Slit4, Acc	16-bit Signed Add to Accumulator	1	1	OA,OB,SA,SB
2	ADDC	ADDC f	$f = f + WREG + (C)$	1	1	C,DC,N,OV,Z
		ADDC f, WREG	$WREG = f + WREG + (C)$	1	1	C,DC,N,OV,Z
		ADDC #lit10, Wn	$Wd = lit10 + Wd + (C)$	1	1	C,DC,N,OV,Z
		ADDC Wb, Ws, Wd	$Wd = Wb + Ws + (C)$	1	1	C,DC,N,OV,Z
		ADDC Wb, #lit5, Wd	$Wd = Wb + lit5 + (C)$	1	1	C,DC,N,OV,Z
3	AND	AND f	$f = f .AND. WREG$	1	1	N,Z
		AND f, WREG	$WREG = f .AND. WREG$	1	1	N,Z
		AND #lit10, Wn	$Wd = lit10 .AND. Wd$	1	1	N,Z
		AND Wb, Ws, Wd	$Wd = Wb .AND. Ws$	1	1	N,Z
		AND Wb, #lit5, Wd	$Wd = Wb .AND. lit5$	1	1	N,Z
4	ASR	ASR f	$f = \text{Arithmetic Right Shift } f$	1	1	C,N,OV,Z
		ASR f, WREG	$WREG = \text{Arithmetic Right Shift } f$	1	1	C,N,OV,Z
		ASR Ws, Wd	$Wd = \text{Arithmetic Right Shift } Ws$	1	1	C,N,OV,Z
		ASR Wb, Wns, Wnd	$Wnd = \text{Arithmetic Right Shift } Wb \text{ by } Wns$	1	1	N,Z
		ASR Wb, #lit5, Wnd	$Wnd = \text{Arithmetic Right Shift } Wb \text{ by } lit5$	1	1	N,Z
5	BCLR	BCLR f, #bit4	Bit Clear f	1	1	None
		BCLR Ws, #bit4	Bit Clear Ws	1	1	None
6	BRA	BRA C, Expr	Branch if Carry	1	1 (2)	None
		BRA GE, Expr	Branch if greater than or equal	1	1 (2)	None
		BRA GEU, Expr	Branch if unsigned greater than or equal	1	1 (2)	None
		BRA GT, Expr	Branch if greater than	1	1 (2)	None
		BRA GTU, Expr	Branch if unsigned greater than	1	1 (2)	None
		BRA LE, Expr	Branch if less than or equal	1	1 (2)	None
		BRA LEU, Expr	Branch if unsigned less than or equal	1	1 (2)	None
		BRA LT, Expr	Branch if less than	1	1 (2)	None
		BRA LTU, Expr	Branch if unsigned less than	1	1 (2)	None
		BRA N, Expr	Branch if Negative	1	1 (2)	None
		BRA NC, Expr	Branch if Not Carry	1	1 (2)	None
		BRA NN, Expr	Branch if Not Negative	1	1 (2)	None
		BRA NOV, Expr	Branch if Not Overflow	1	1 (2)	None
		BRA NZ, Expr	Branch if Not Zero	1	1 (2)	None
		BRA OA, Expr	Branch if Accumulator A overflow	1	1 (2)	None
		BRA OB, Expr	Branch if Accumulator B overflow	1	1 (2)	None
		BRA OV, Expr	Branch if Overflow	1	1 (2)	None
		BRA SA, Expr	Branch if Accumulator A saturated	1	1 (2)	None
		BRA SB, Expr	Branch if Accumulator B saturated	1	1 (2)	None
		BRA Expr	Branch Unconditionally	1	2	None
		BRA Z, Expr	Branch if Zero	1	1 (2)	None
		BRA Wn	Computed Branch	1	2	None
7	BSET	BSET f, #bit4	Bit Set f	1	1	None
		BSET Ws, #bit4	Bit Set Ws	1	1	None
8	BSW	BSW.C Ws, Wb	Write C bit to Ws<Wb>	1	1	None
		BSW.Z Ws, Wb	Write Z bit to Ws<Wb>	1	1	None



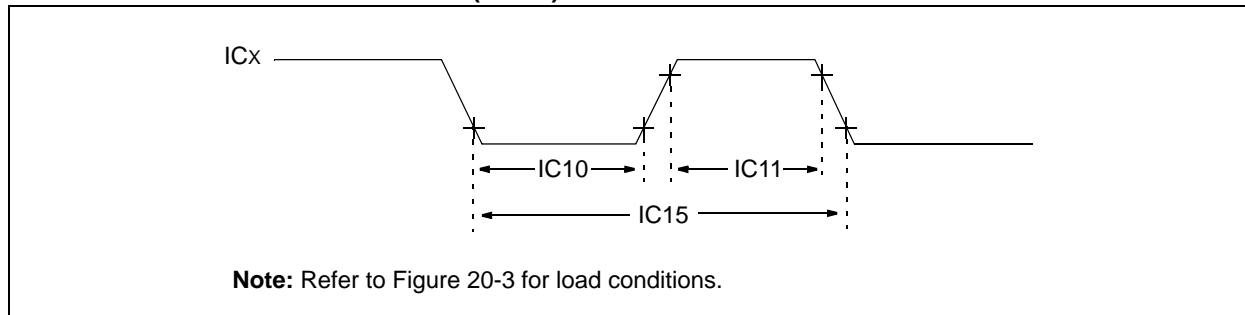
# dsPIC30F2011/2012/3012/3013

**TABLE 18-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
29	DIV	DIV.S Wm, Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD Wm, Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.U Wm, Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD Wm, Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
30	DIVF	DIVF Wm, Wn	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV
31	DO	DO #lit14, Expr	Do code to PC+Expr, lit14+1 times	2	2	None
		DO Wn, Expr	Do code to PC+Expr, (Wn)+1 times	2	2	None
32	ED	ED Wm*Wm, Acc, Wx, Wy, Wxd	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB,SA,SB,SAB
33	EDAC	EDAC Wm*Wm, Acc, Wx, Wy, Wxd	Euclidean Distance	1	1	OA,OB,OAB,SA,SB,SAB
34	EXCH	EXCH Wns, Wnd	Swap Wns with Wnd	1	1	None
35	FBCL	FBCL Ws, Wnd	Find Bit Change from Left (MSb) Side	1	1	C
36	FF1L	FF1L Ws, Wnd	Find First One from Left (MSb) Side	1	1	C
37	FF1R	FF1R Ws, Wnd	Find First One from Right (LSb) Side	1	1	C
38	GOTO	GOTO Expr	Go to address	2	2	None
		GOTO Wn	Go to indirect	1	2	None
39	INC	INC f	f = f + 1	1	1	C,DC,N,OV,Z
		INC f, WREG	WREG = f + 1	1	1	C,DC,N,OV,Z
		INC Ws, Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
40	INC2	INC2 f	f = f + 2	1	1	C,DC,N,OV,Z
		INC2 f, WREG	WREG = f + 2	1	1	C,DC,N,OV,Z
		INC2 Ws, Wd	Wd = Ws + 2	1	1	C,DC,N,OV,Z
41	IOR	IOR f	f = f .IOR. WREG	1	1	N,Z
		IOR f, WREG	WREG = f .IOR. WREG	1	1	N,Z
		IOR #lit10, Wn	Wd = lit10 .IOR. Wd	1	1	N,Z
		IOR Wb, Ws, Wd	Wd = Wb .IOR. Ws	1	1	N,Z
		IOR Wb, #lit5, Wd	Wd = Wb .IOR. lit5	1	1	N,Z
42	LAC	LAC Wso, #Slit4, Acc	Load Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
43	LNK	LNK #lit14	Link frame pointer	1	1	None
44	LSR	LSR f	f = Logical Right Shift f	1	1	C,N,OV,Z
		LSR f, WREG	WREG = Logical Right Shift f	1	1	C,N,OV,Z
		LSR Ws, Wd	Wd = Logical Right Shift Ws	1	1	C,N,OV,Z
		LSR Wb, Wns, Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N,Z
		LSR Wb, #lit5, Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N,Z
45	MAC	MAC Wm*Wn, Acc, Wx, Wxd, Wy, Wyd, AWB	Multiply and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB
		MAC Wm*Wm, Acc, Wx, Wxd, Wy, Wyd	Square and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB
46	MOV	MOV f, Wn	Move f to Wn	1	1	None
		MOV f	Move f to f	1	1	N,Z
		MOV f, WREG	Move f to WREG	1	1	N,Z
		MOV #lit16, Wn	Move 16-bit literal to Wn	1	1	None
		MOV.b #lit8, Wn	Move 8-bit literal to Wn	1	1	None
		MOV Wn, f	Move Wn to f	1	1	None
		MOV Wso, Wdo	Move Ws to Wd	1	1	None
		MOV WREG, f	Move WREG to f	1	1	N,Z
		MOV.D Wns, Wd	Move Double from W(ns):W(ns+1) to Wd	1	2	None
		MOV.D Ws, Wnd	Move Double from Ws to W(nd+1):W(nd)	1	2	None
47	MOVSAC	MOVSAC Acc, Wx, Wxd, Wy, Wyd, AWB	Prefetch and store accumulator	1	1	None

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**FIGURE 20-9: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS**



**TABLE 20-26: INPUT CAPTURE TIMING REQUIREMENTS**

AC CHARACTERISTICS		<b>Standard Operating Conditions: 2.5V to 5.5V</b> <b>(unless otherwise stated)</b> Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended					
Param No.	Symbol	Characteristic <sup>(1)</sup>		Min	Max	Units	Conditions
IC10	TccL	ICx Input Low Time	No Prescaler	$0.5 T_{CY} + 20$	—	ns	
			With Prescaler	10	—	ns	
IC11	TccH	ICx Input High Time	No Prescaler	$0.5 T_{CY} + 20$	—	ns	
			With Prescaler	10	—	ns	
IC15	TccP	ICx Input Period		$(2 T_{CY} + 40)/N$	—	ns	N = prescale value (1, 4, 16)

**Note 1:** These parameters are characterized but not tested in manufacturing.

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**TABLE 20-34: I<sup>2</sup>C™ BUS DATA TIMING REQUIREMENTS (SLAVE MODE) (CONTINUED)**

AC CHARACTERISTICS				Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤T <sub>A</sub> ≤+85°C for Industrial -40°C ≤T <sub>A</sub> ≤+125°C for Extended			
Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
IS25	T <sub>SU</sub> :DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode <sup>(1)</sup>	100	—	ns	
IS26	T <sub>HD</sub> :DAT	Data Input Hold Time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
			1 MHz mode <sup>(1)</sup>	0	0.3	μs	
IS30	T <sub>SU</sub> :STA	Start Condition Setup Time	100 kHz mode	4.7	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	0.6	—	μs	
			1 MHz mode <sup>(1)</sup>	0.25	—	μs	
IS31	T <sub>HD</sub> :STA	Start Condition Hold Time	100 kHz mode	4.0	—	μs	After this period the first clock pulse is generated
			400 kHz mode	0.6	—	μs	
			1 MHz mode <sup>(1)</sup>	0.25	—	μs	
IS33	T <sub>SU</sub> :STO	Stop Condition Setup Time	100 kHz mode	4.7	—	μs	
			400 kHz mode	0.6	—	μs	
			1 MHz mode <sup>(1)</sup>	0.6	—	μs	
IS34	T <sub>HD</sub> :STO	Stop Condition Hold Time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
			1 MHz mode <sup>(1)</sup>	250	—	ns	
IS40	T <sub>AA</sub> :SCL	Output Valid From Clock	100 kHz mode	0	3500	ns	
			400 kHz mode	0	1000	ns	
			1 MHz mode <sup>(1)</sup>	0	350	ns	
IS45	T <sub>BF</sub> :SDA	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode <sup>(1)</sup>	0.5	—	μs	
IS50	C <sub>B</sub>	Bus Capacitive Loading		—	400	pF	

**Note 1:** Maximum pin capacitance = 10 pF for all I<sup>2</sup>C™ pins (for 1 MHz mode only).

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**TABLE 20-37: 12-BIT A/D CONVERSION TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 2.7V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ	Max.	Units	Conditions
<b>Clock Parameters</b>							
AD50	TAD	A/D Clock Period	334	—	—	ns	VDD = 3-5.5V (Note 1)
AD51	tRC	A/D Internal RC Oscillator Period	1.2	1.5	1.8	μs	
<b>Conversion Rate</b>							
AD55	tCONV	Conversion Time	—	14 TAD	—	ns	
AD56a	FCNV	Throughput Rate	—	200	—	ksps	VDD = VREF = 5V, Industrial temperature
AD56b	FCNV	Throughput Rate	—	100	—	ksps	VDD = VREF = 5V, Extended temperature
AD57	TSAMP	Sampling Time	1 TAD	—	—	ns	VDD = 3-5.5V source resistance Rs = 0-2.5 kΩ
<b>Timing Parameters</b>							
AD60	tPCS	Conversion Start from Sample Trigger	—	1 TAD	—	ns	
AD61	tPSS	Sample Start from Setting Sample (SAMP) Bit	0.5 TAD	—	1.5 TAD	ns	
AD62	tCSS	Conversion Completion to Sample Start (ASAM = 1)	—	0.5 TAD	—	ns	
AD63	tDPU <sup>(2)</sup>	Time to Stabilize Analog Stage from A/D Off to A/D On	—	—	20	μs	

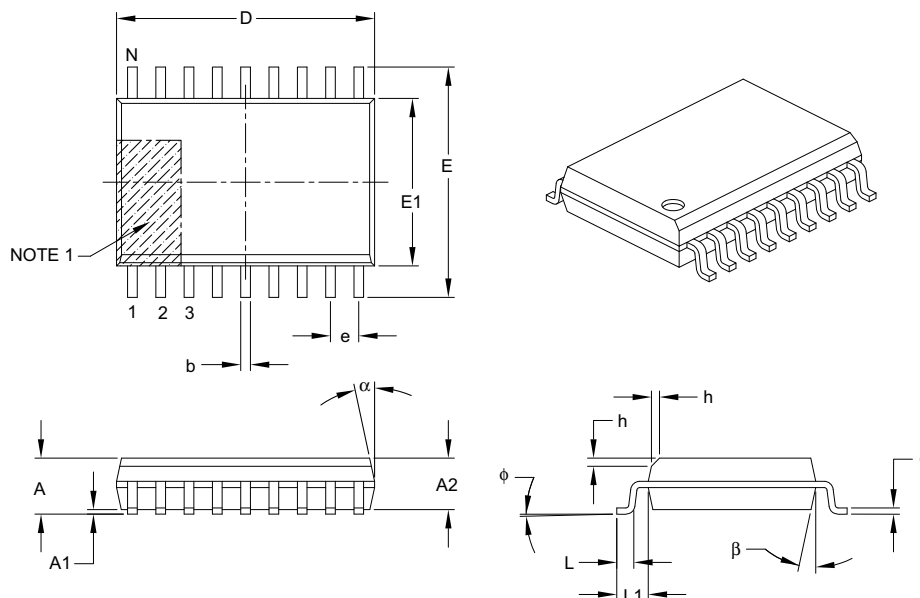
**Note 1:** Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

**2:** tDPU is the time required for the ADC module to stabilize when it is turned on (ADCON1<ADON> = 1). During this time the ADC result is indeterminate.

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## 18-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	18		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	2.65
Molded Package Thickness	A2	2.05	–	–
Standoff §	A1	0.10	–	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	11.55 BSC		
Chamfer (optional)	h	0.25	–	0.75
Foot Length	L	0.40	–	1.27
Footprint	L1	1.40 REF		
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.20	–	0.33
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-051B