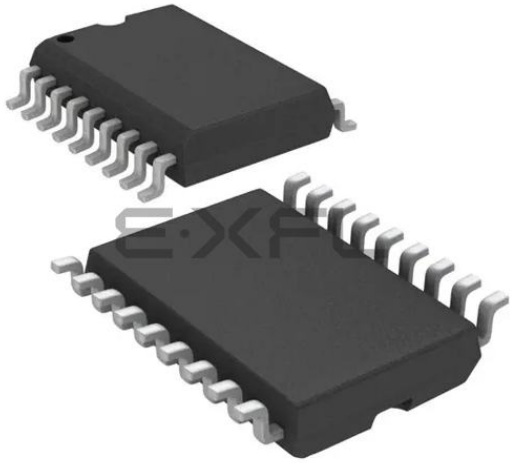


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	30 MIPs
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	12KB (4K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic30f2011t-30i-so

TABLE 3-3: CORE REGISTER MAP

SFR Name	Address (Home)	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
W0	0000	W0/WREG																0000 0000 0000 0000
W1	0002	W1																0000 0000 0000 0000
W2	0004	W2																0000 0000 0000 0000
W3	0006	W3																0000 0000 0000 0000
W4	0008	W4																0000 0000 0000 0000
W5	000A	W5																0000 0000 0000 0000
W6	000C	W6																0000 0000 0000 0000
W7	000E	W7																0000 0000 0000 0000
W8	0010	W8																0000 0000 0000 0000
W9	0012	W9																0000 0000 0000 0000
W10	0014	W10																0000 0000 0000 0000
W11	0016	W11																0000 0000 0000 0000
W12	0018	W12																0000 0000 0000 0000
W13	001A	W13																0000 0000 0000 0000
W14	001C	W14																0000 0000 0000 0000
W15	001E	W15																0000 1000 0000 0000
SPLIM	0020	SPLIM																0000 0000 0000 0000
ACCAL	0022	ACCAL																0000 0000 0000 0000
ACCAH	0024	ACCAH																0000 0000 0000 0000
ACCAU	0026	Sign Extension (ACCA<39>)									ACCAU							0000 0000 0000 0000
ACCBL	0028	ACCBL																0000 0000 0000 0000
ACCBH	002A	ACCBH																0000 0000 0000 0000
ACCBU	002C	Sign Extension (ACCB<39>)									ACCBU							0000 0000 0000 0000
PCL	002E	PCL																0000 0000 0000 0000
PCH	0030	—	—	—	—	—	—	—	—	—	PCH							0000 0000 0000 0000
TBLPAG	0032	—	—	—	—	—	—	—	—	TBLPAG								0000 0000 0000 0000
PSVPAG	0034	—	—	—	—	—	—	—	—	PSVPAG								0000 0000 0000 0000
RCOUNT	0036	RCOUNT																uuuu uuuu uuuu uuuu
DCOUNT	0038	DCOUNT																uuuu uuuu uuuu uuuu
DOSTARTL	003A	DOSTARTL															0	uuuu uuuu uuuu uuu0
DOSTARTH	003C	—	—	—	—	—	—	—	—	—	DOSTARTH							0000 0000 0uuu uuuu
DOENDL	003E	DOENDL															0	uuuu uuuu uuuu uuu0
DOENDH	0040	—	—	—	—	—	—	—	—	—	DOENDH							0000 0000 0uuu uuuu
SR	0042	OA	OB	SA	SB	OAB	SAB	DA	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	C	0000 0000 0000 0000

Legend: u = uninitialized bit; — = unimplemented bit, read as '0'

Note: Refer to the "*dsPIC30F Family Reference Manual*" (DS70046) for descriptions of register bit fields.

NOTES:

5.6 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. A programming operation is nominally 2 msec in duration and the processor stalls (waits) until the operation is finished. Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

5.6.1 PROGRAMMING ALGORITHM FOR PROGRAM FLASH

The user can erase or program one row of program Flash memory at a time. The general process is:

1. Read one row of program Flash (32 instruction words) and store into data RAM as a data “image”.
2. Update the data image with the desired new data.
3. Erase program Flash row.
   a) Set up NVMCON register for multi-word, program Flash, erase, and set WREN bit.
   b) Write address of row to be erased into NVMADRU/NVMDR.
   c) Write 0x55 to NVMKEY.
   d) Write 0xAA to NVMKEY.
   e) Set the WR bit. This begins erase cycle.
   f) CPU stalls for the duration of the erase cycle.
   g) The WR bit is cleared when erase cycle ends.
4. Write 32 instruction words of data from data RAM “image” into the program Flash write latches.
5. Program 32 instruction words into program Flash.
   a) Set up NVMCON register for multi-word, program Flash, program, and set WREN bit.
   b) Write 0x55 to NVMKEY.
   c) Write 0xAA to NVMKEY.
   d) Set the WR bit. This begins program cycle.
   e) CPU stalls for duration of the program cycle.
   f) The WR bit is cleared by the hardware when program cycle ends.
6. Repeat steps 1 through 5 as needed to program desired amount of program Flash memory.

5.6.2 ERASING A ROW OF PROGRAM MEMORY

Example 5-1 shows a code sequence that can be used to erase a row (32 instructions) of program memory.

EXAMPLE 5-1: ERASING A ROW OF PROGRAM MEMORY

```
; Setup NVMCON for erase operation, multi word write
; program memory selected, and writes enabled
       MOV     #0x4041,W0                  ;
       MOV     W0,NVMCON                   ; Init NVMCON SFR
; Init pointer to row to be ERASED
       MOV     #tblpage(PROG_ADDR),W0      ;
       MOV     W0,NVMADRU                  ; Initialize PM Page Boundary SFR
       MOV     #tbloffset(PROG_ADDR),W0    ; Intialize in-page EA[15:0] pointer
       MOV     W0, NVMADR                  ; Initialize NVMADR SFR
       DISI    #5                          ; Block all interrupts with priority <7 for
                                           ; next 5 instructions
       MOV     #0x55,W0
       MOV     W0,NVMKEY                   ; Write the 0x55 key
       MOV     #0xAA,W1                    ;
       MOV     W1,NVMKEY                   ; Write the 0xAA key
       BSET    NVMCON,#WR                  ; Start the erase sequence
       NOP                                 ; Insert two NOPs after the erase
       NOP                                 ; command is asserted
```

NOTES:

FIGURE 10-2: 16-BIT TIMER2 BLOCK DIAGRAM

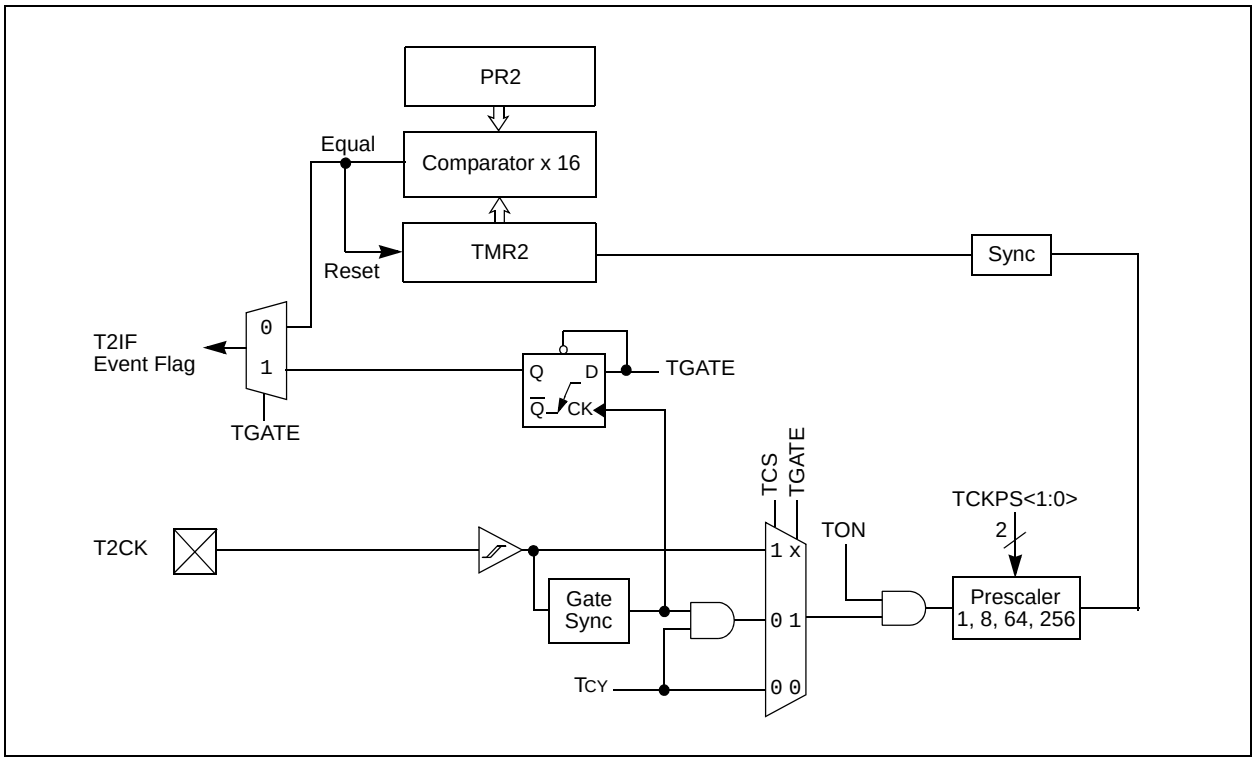
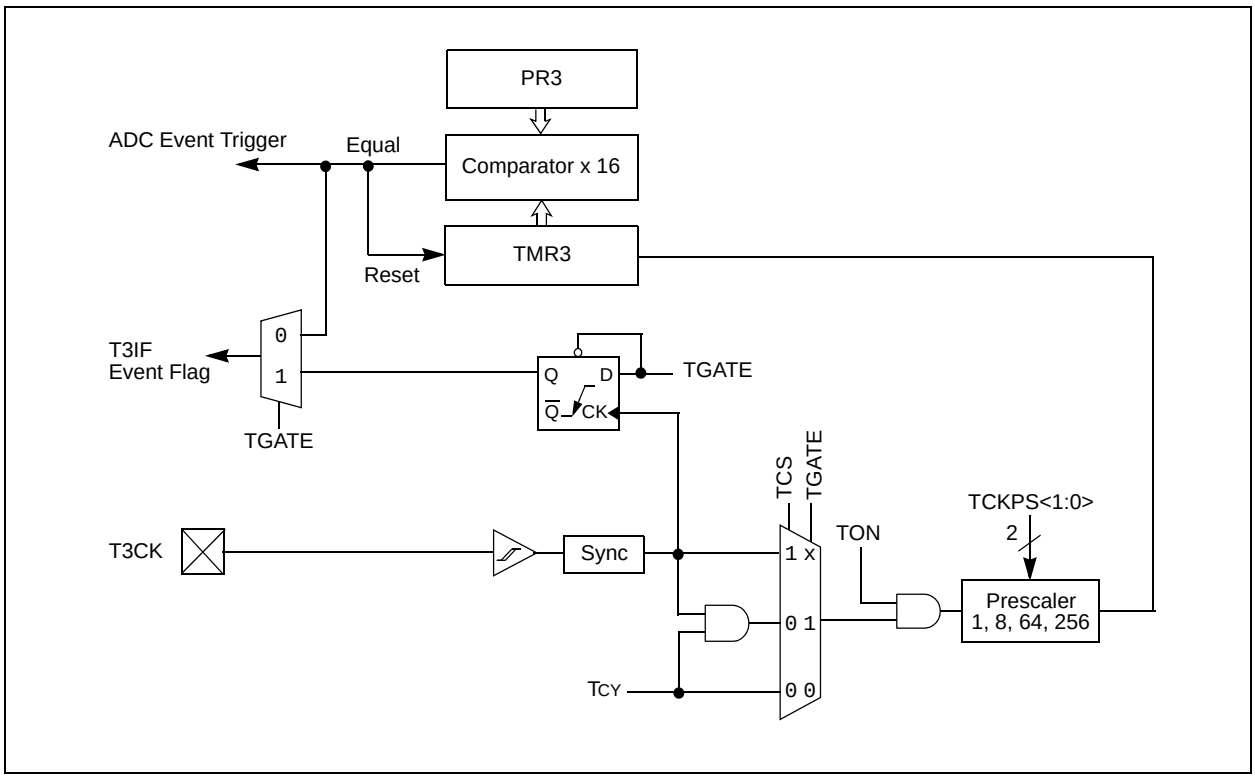


FIGURE 10-3: 16-BIT TIMER3 BLOCK DIAGRAM



13.0 SPI™ MODULE

Note:	This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046).

The Serial Peripheral Interface (SPI™) module is a synchronous serial interface. It is useful for communicating with other peripheral devices, such as EEPROMs, shift registers, display drivers and A/D converters, or other microcontrollers. It is compatible with Motorola's SPI and SIOP interfaces. The dsPIC30F2011/2012/3012/3013 devices feature one SPI module, SPI1.

13.1 Operating Function Description

Figure 13-1 is a simplified block diagram of the SPI module, which consists of a 16-bit shift register, SPI1SR, used for shifting data in and out, and a buffer register, SPI1BUF. Control register SPI1CON (not shown) configures the module. Additionally, status register SPI1STAT (not shown) indicates various status conditions.

Note:	See "*dsPIC30F Family Reference Manual*" (DS70046) for detailed information on the control and status registers.

Four I/O pins comprise the serial interface:

- SDI1 (serial data input)
- SDO1 (serial data output)
- SCK1 (shift clock input or output)
- $\overline{SS1}$ (active-low slave select).

In Master mode operation, SCK1 is a clock output. In Slave mode, it is a clock input.

A series of eight (8) or sixteen (16) clock pulses shift out bits from the SPI1SR to SDO1 pin and simultaneously shift in data from SDI1 pin. An interrupt is generated when the transfer is complete and the interrupt flag bit (SPI1IF) is set. This interrupt can be disabled through the interrupt enable bit, SPI1IE.

The receive operation is double-buffered. When a complete byte is received, it is transferred from SPI1SR to SPI1BUF.

If the receive buffer is full when new data is being transferred from SPI1SR to SPI1BUF, the module will set the SPIROV bit indicating an overflow condition. The transfer of the data from SPI1SR to SPI1BUF is not completed and the new data is lost. The module will not respond to SCL transitions while SPIROV is '1', effectively disabling the module until SPI1BUF is read by user software.

Transmit writes are also double-buffered. The user writes to SPI1BUF. When the master or slave transfer is completed, the contents of the shift register (SPI1SR) are moved to the receive buffer. If any transmit data has been written to the buffer register, the contents of the transmit buffer are moved to SPI1SR. The received data is thus placed in SPI1BUF and the transmit data in SPI1SR is ready for the next transfer.

Note:	Both the transmit buffer (SPI1TXB) and the receive buffer (SPI1RXB) are mapped to the same register address, SPI1BUF.

14.7 Interrupts

The I²C module generates two interrupt flags, MI2CIF (I²C Master Interrupt Flag) and SI2CIF (I²C Slave Interrupt Flag). The MI2CIF interrupt flag is activated on completion of a master message event. The SI2CIF interrupt flag is activated on detection of a message directed to the slave.

14.8 Slope Control

The I²C standard requires slope control on the SDA and SCL signals for Fast mode (400 kHz). The control bit, DISSLW, enables the user to disable slew rate control if desired. It is necessary to disable the slew rate control for 1 MHz mode.

14.9 IPMI Support

The control bit, IPMIEN, enables the module to support Intelligent Peripheral Management Interface (IPMI). When this bit is set, the module accepts and acts upon all addresses.

14.10 General Call Address Support

The general call address can address all devices. When this address is used, all devices should, in theory, respond with an acknowledgement.

The general call address is one of eight addresses reserved for specific purposes by the I²C protocol. It consists of all '0's with R_W = 0.

The general call address is recognized when the General Call Enable (GCEN) bit is set (I2CCON<7> = 1). Following a Start bit detection, 8 bits are shifted into I2CRSR and the address is compared with I2CADD, and is also compared with the general call address which is fixed in hardware.

If a general call address match occurs, the I2CRSR is transferred to the I2CRCV after the eighth clock, the RBF flag is set and on the falling edge of the ninth bit (ACK bit), the master event interrupt flag (MI2CIF) is set.

When the interrupt is serviced, the source for the interrupt can be checked by reading the contents of the I2CRCV to determine if the address was device specific or a general call address.

14.11 I²C Master Support

As a master device, six operations are supported:

- Assert a Start condition on SDA and SCL.
- Assert a Restart condition on SDA and SCL.
- Write to the I2CTRN register initiating transmission of data/address.
- Generate a Stop condition on SDA and SCL.
- Configure the I²C port to receive data.
- Generate an ACK condition at the end of a received byte of data.

14.12 I²C Master Operation

The master device generates all of the serial clock pulses and the Start and Stop conditions. A transfer is ended with a Stop condition or with a Repeated Start condition. Since the Repeated Start condition is also the beginning of the next serial transfer, the I²C bus will not be released.

In Master Transmitter mode, serial data is output through SDA, while SCL outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the data direction bit. In this case, the data direction bit (R_W) is logic '0'. Serial data is transmitted 8 bits at a time. After each byte is transmitted, an ACK bit is received. Start and Stop conditions are output to indicate the beginning and the end of a serial transfer.

In Master Receive mode, the first byte transmitted contains the slave address of the transmitting device (7 bits) and the data direction bit. In this case, the data direction bit (R_W) is logic '1'. Thus, the first byte transmitted is a 7-bit slave address, followed by a '1' to indicate receive bit. Serial data is received via SDA while SCL outputs the serial clock. Serial data is received 8 bits at a time. After each byte is received, an ACK bit is transmitted. Start and Stop conditions indicate the beginning and end of transmission.

14.12.1 I²C MASTER TRANSMISSION

Transmission of a data byte, a 7-bit address, or the second half of a 10-bit address, is accomplished by simply writing a value to I2CTRN register. The user should only write to I2CTRN when the module is in a WAIT state. This action will set the Buffer Full Flag (TBF) and allow the Baud Rate Generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDA pin after the falling edge of SCL is asserted. The Transmit Status Flag, TRSTAT (I2CSTAT<14>), indicates that a master transmit is in progress.

NOTES:

15.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART) MODULE

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046).

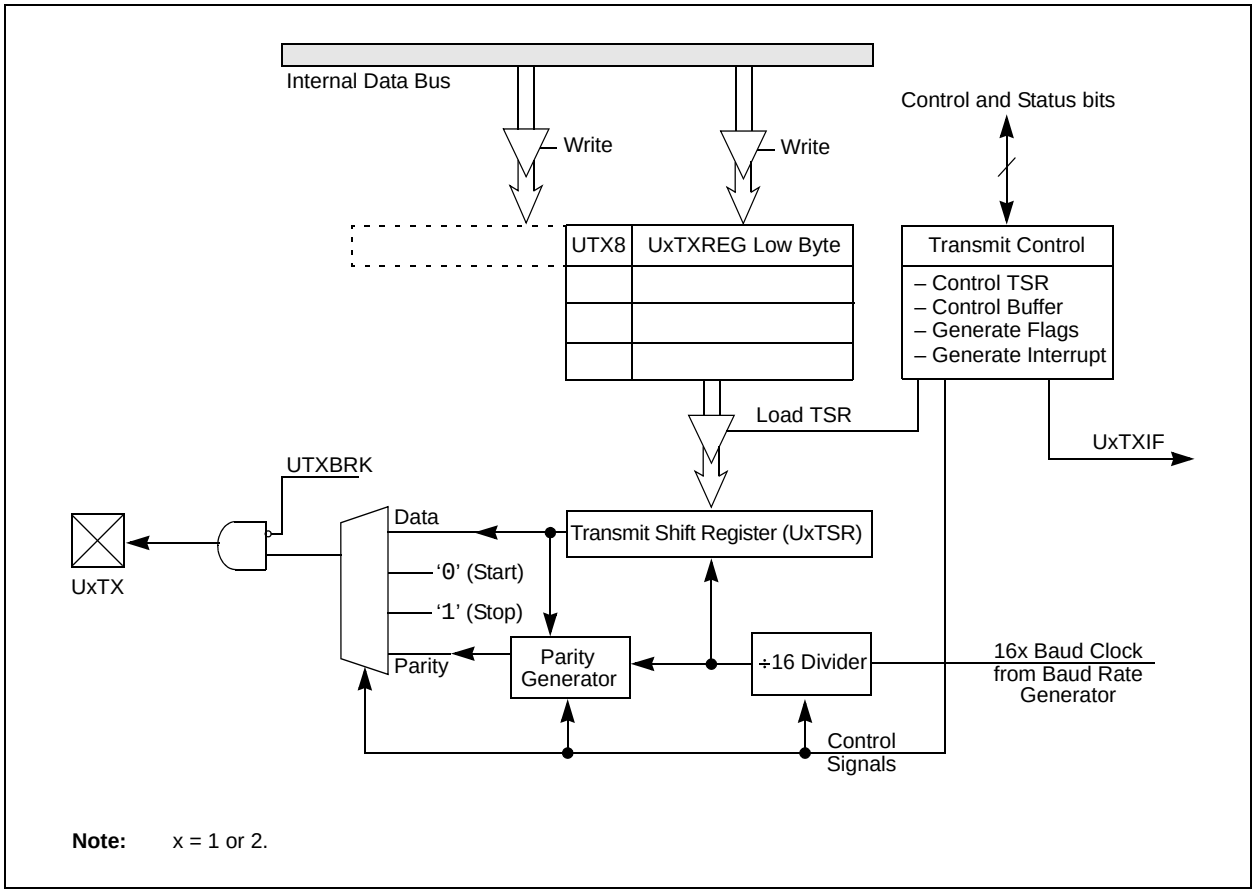
This section describes the Universal Asynchronous Receiver/Transmitter Communications module. The dsPIC30F2011/2012/3012 processors have one UART module (UART1). The dsPIC30F3013 processor has two UART modules (UART1 and UART2).

15.1 UART Module Overview

The key features of the UART module are:

- Full-duplex, 8 or 9-bit data communication
- Even, odd or no parity options (for 8-bit data)
- One or two Stop bits
- Fully integrated Baud Rate Generator with 16-bit prescaler
- Baud rates range from 38 bps to 1.875 Mbps at a 30 MHz instruction rate
- 4-word deep transmit data buffer
- 4-word deep receive data buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt only on address detect (9th bit = 1)
- Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- Alternate receive and transmit pins for UART1

FIGURE 15-1: UART TRANSMITTER BLOCK DIAGRAM



Note: x = 1 or 2.

The configuration procedures in the next section provide the required setup values for the conversion speeds above 100 ksps.

16.7.1 200 KSPS CONFIGURATION GUIDELINE

The following configuration items are required to achieve a 200 ksps conversion rate.

- Comply with conditions provided in Table 16-1.
- Connect external VREF+ and VREF- pins following the recommended circuit shown in Figure 16-2.
- Set SSRC<2.0> = 111 in the ADCON1 register to enable the auto convert option.
- Enable automatic sampling by setting the ASAM control bit in the ADCON1 register.
- Write the SMPI<3.0> control bits in the ADCON2 register for the desired number of conversions between interrupts.
- Configure the ADC clock period to be:

$$\frac{1}{(14 + 1) \times 200{,}000} = 334 \text{ ns}$$

  by writing to the ADCS<5:0> control bits in the ADCON3 register.
- Configure the sampling time to be 1 TAD by writing: SAMC<4:0> = 00001.

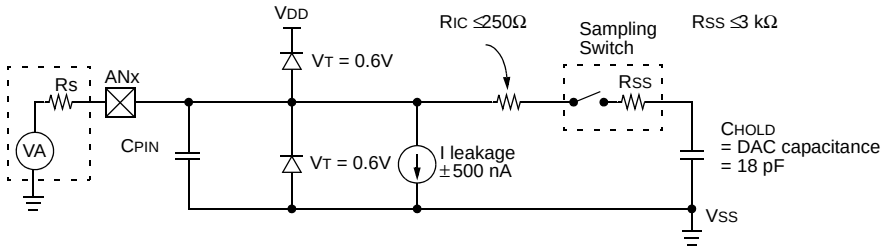
The following figure shows the timing diagram of the ADC running at 200 ksps. The TAD selection in conjunction with the guidelines described above allows a conversion speed of 200 ksps. See Example 16-1 for code example.

16.8 A/D Acquisition Requirements

The analog input model of the 12-bit ADC is shown in Figure 16-3. The total sampling time for the A/D is a function of the internal amplifier settling time and the holding capacitor charge time.

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the voltage level on the analog input pin. The source impedance (RS), the interconnect impedance (RIC) and the internal sampling switch (RSS) impedance combine to directly affect the time required to charge the capacitor CHOLD. The combined impedance of the analog sources must therefore be small enough to fully charge the holding capacitor within the chosen sample time. To minimize the effects of pin leakage currents on the accuracy of the ADC, the maximum recommended source impedance, RS, is 2.5 kΩ. After the analog input channel is selected (changed), this sampling function must be completed prior to starting the conversion. The internal holding capacitor will be in a discharged state prior to each sample operation.

FIGURE 16-3: 12-BIT A/D CONVERTER ANALOG INPUT MODEL



Legend: CPIN = input capacitance; VT = threshold voltage; I leakage = leakage current at the pin due to various junctions; RIC = interconnect resistance; RSS = sampling switch resistance; CHOLD = sample/hold capacitance (from DAC)

Note: CPIN value depends on device package and is not tested. Effect of CPIN negligible if Rs ≤2.5 kΩ

TABLE 16-3: A/D CONVERTER REGISTER MAP FOR dsPIC30F2012/3013

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
ADCBUF0	0280	—	—	—	—	ADC Data Buffer 0												0000 uuuu uuuu uuuu
ADCBUF1	0282	—	—	—	—	ADC Data Buffer 1												0000 uuuu uuuu uuuu
ADCBUF2	0284	—	—	—	—	ADC Data Buffer 2												0000 uuuu uuuu uuuu
ADCBUF3	0286	—	—	—	—	ADC Data Buffer 3												0000 uuuu uuuu uuuu
ADCBUF4	0288	—	—	—	—	ADC Data Buffer 4												0000 uuuu uuuu uuuu
ADCBUF5	028A	—	—	—	—	ADC Data Buffer 5												0000 uuuu uuuu uuuu
ADCBUF6	028C	—	—	—	—	ADC Data Buffer 6												0000 uuuu uuuu uuuu
ADCBUF7	028E	—	—	—	—	ADC Data Buffer 7												0000 uuuu uuuu uuuu
ADCBUF8	0290	—	—	—	—	ADC Data Buffer 8												0000 uuuu uuuu uuuu
ADCBUF9	0292	—	—	—	—	ADC Data Buffer 9												0000 uuuu uuuu uuuu
ADCBUFA	0294	—	—	—	—	ADC Data Buffer 10												0000 uuuu uuuu uuuu
ADCBUFB	0296	—	—	—	—	ADC Data Buffer 11												0000 uuuu uuuu uuuu
ADCBUFC	0298	—	—	—	—	ADC Data Buffer 12												0000 uuuu uuuu uuuu
ADCBUFD	029A	—	—	—	—	ADC Data Buffer 13												0000 uuuu uuuu uuuu
ADCBUFE	029C	—	—	—	—	ADC Data Buffer 14												0000 uuuu uuuu uuuu
ADCBUFF	029E	—	—	—	—	ADC Data Buffer 15												0000 uuuu uuuu uuuu
ADCON1	02A0	ADON	—	ADSIDL	—	—	—	FORM<1:0>		SSRC<2:0>			—	—	ASAM	SAMP	DONE	0000 0000 0000 0000
ADCON2	02A2	VCFG<2:0>			—	—	CSCNA	—	—	BUFS	—	SMPI<3:0>				BUFM	ALTS	0000 0000 0000 0000
ADCON3	02A4	—	—	—	SAMC<4:0>					ADRC	—	ADCS<5:0>						0000 0000 0000 0000
ADCHS	02A6	—	—	—	CH0NB	CH0SB<3:0>				—	—	—	CH0NA	CH0SA<3:0>				0000 0000 0000 0000
ADPCFG	02A8	—	—	—	—	—	—	PCFG9	PCFG8	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000 0000 0000 0000
ADCSSL	02AA	—	—	—	—	—	—	CSSL9	CSSL8	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0	0000 0000 0000 0000

Legend: u = uninitialized bit; — = unimplemented bit, read as '0'

Note: Refer to the "*dsPIC30F Family Reference Manual*" (DS70046) for descriptions of register bit fields.

Any interrupt that is individually enabled (using the corresponding IE bit) and meets the prevailing priority level will be able to wake-up the processor. The processor will process the interrupt and branch to the ISR. The Sleep Status bit in the RCON register is set upon wake-up.

Note:	In spite of various delays applied (TPOR, TLOCK and TPWRT), the crystal oscillator (and PLL) may not be active at the end of the time-out (e.g., for low-frequency crystals). In such cases, if FSCM is enabled, then the device will detect this as a clock failure and process the clock failure trap, the FRC oscillator will be enabled and the user will have to re-enable the crystal oscillator. If FSCM is not enabled, then the device will simply suspend execution of code until the clock is stable and will remain in Sleep until the oscillator clock has started.

All Resets will wake-up the processor from Sleep mode. Any Reset, other than POR, will set the Sleep Status bit. In a POR, the Sleep bit is cleared.

If the Watchdog Timer is enabled, then the processor will wake-up from Sleep mode upon WDT time-out. The Sleep and WDTO Status bits are both set.

17.6.2 IDLE MODE

In Idle mode, the clock to the CPU is shut down while peripherals keep running. Unlike Sleep mode, the clock source remains active.

Several peripherals have a control bit in each module that allows them to operate during Idle.

LPRC Fail-Safe Clock remains active if clock failure detect is enabled.

The processor wakes up from Idle if at least one of the following conditions has occurred:

- any interrupt that is individually enabled (IE bit is '1') and meets the required priority level
- any Reset (POR, BOR, $\overline{\text{MCLR}}$)
- WDT time-out

Upon wake-up from Idle mode, the clock is re-applied to the CPU and instruction execution begins immediately, starting with the instruction following the PWRSAV instruction.

Any interrupt that is individually enabled (using IE bit) and meets the prevailing priority level will be able to wake-up the processor. The processor will process the interrupt and branch to the ISR. The Idle Status bit in the RCON register is set upon wake-up.

Any Reset other than POR will set the Idle Status bit. On a POR, the Idle bit is cleared.

If Watchdog Timer is enabled, then the processor will wake-up from Idle mode upon WDT time-out. The Idle and WDTO Status bits are both set.

Unlike wake-up from Sleep, there are no time delays involved in wake-up from Idle.

17.7 Device Configuration Registers

The Configuration bits in each device Configuration register specify some of the device modes and are programmed by a device programmer, or by using the In-Circuit Serial Programming™ (ICSP™) feature of the device. Each device Configuration register is a 24-bit register, but only the lower 16 bits of each register are used to hold configuration data. There are five device Configuration registers available to the user:

1. FOSC (0xF80000): Oscillator Configuration Register
2. FWDT (0xF80002): Watchdog Timer Configuration Register
3. FBORPOR (0xF80004): BOR and POR Configuration Register
4. FGS (0xF8000A): General Code Segment Configuration Register
5. FICD (0xF8000C): Debug Configuration Register

The placement of the Configuration bits is automatically handled when you select the device in your device programmer. The desired state of the Configuration bits may be specified in the source code (dependent on the language tool used), or through the programming interface. After the device has been programmed, the application software may read the Configuration bit values through the table read instructions. For additional information, please refer to the Programming Specifications of the device.

Note:	If the code protection Configuration fuse bits (FGS<GCP> and FGS<GWRP>) have been programmed, an erase of the entire code-protected device is only possible at voltages $V_{DD} \geq 4.5V$.

TABLE 18-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)

Field	Description
Wb	Base W register ∈ {W0..W15}
Wd	Destination W register ∈ { Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd] }
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] }
Wm,Wn	Dividend, Divisor working register pair (direct addressing)
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions ∈ {W4*W4,W5*W5,W6*W6,W7*W7}
Wm*Wn	Multiplicand and Multiplier working register pair for DSP instructions ∈ {W4*W5,W4*W6,W4*W7,W5*W6,W5*W7,W6*W7}
Wn	One of 16 working registers ∈ {W0..W15}
Wnd	One of 16 destination working registers ∈ {W0..W15}
Wns	One of 16 source working registers ∈ {W0..W15}
WREG	W0 (working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws--], [++Ws], [--Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns--], [++Wns], [--Wns], [Wns+Wb] }
Wx	X data space prefetch address register for DSP instructions ∈ {[W8]+=6, [W8]+=4, [W8]+=2, [W8], [W8]-=6, [W8]-=4, [W8]-=2, [W9]+=6, [W9]+=4, [W9]+=2, [W9], [W9]-=6, [W9]-=4, [W9]-=2, [W9+W12],none}
Wxd	X data space prefetch destination register for DSP instructions ∈ {W4..W7}
Wy	Y data space prefetch address register for DSP instructions ∈ {[W10]+=6, [W10]+=4, [W10]+=2, [W10], [W10]-=6, [W10]-=4, [W10]-=2, [W11]+=6, [W11]+=4, [W11]+=2, [W11], [W11]-=6, [W11]-=4, [W11]-=2, [W11+W12], none}
Wyd	Y data space prefetch destination register for DSP instructions ∈ {W4..W7}

TABLE 20-9: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	VOL	**Output Low Voltage(2)**					
DO10		I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 5V
			—	—	0.15	V	IOL = 2.0 mA, VDD = 3V
DO16		OSC2/CLKO	—	—	0.6	V	IOL = 1.6 mA, VDD = 5V
		(RC or EC Osc mode)	—	—	0.72	V	IOL = 2.0 mA, VDD = 3V
	VOH	**Output High Voltage(2)**					
DO20		I/O ports	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 5V
			VDD – 0.2	—	—	V	IOH = -2.0 mA, VDD = 3V
DO26		OSC2/CLKO	VDD – 0.7	—	—	V	IOH = -1.3 mA, VDD = 5V
		(RC or EC Osc mode)	VDD – 0.1	—	—	V	IOH = -2.0 mA, VDD = 3V
		Capacitive Loading Specs on Output Pins(2)					
DO50	COSC2	OSC2/SOSC2 pin	—	—	15	pF	In XTL, XT, HS and LP modes when external clock is used to drive OSC1.
DO56	CIO	All I/O pins and OSC2	—	—	50	pF	RC or EC Osc mode
DO58	CB	SCL, SDA	—	—	400	pF	In I^2C mode

Note 1: Data in “Typ” column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: These parameters are characterized but not tested in manufacturing.

FIGURE 20-2: BROWN-OUT RESET CHARACTERISTICS

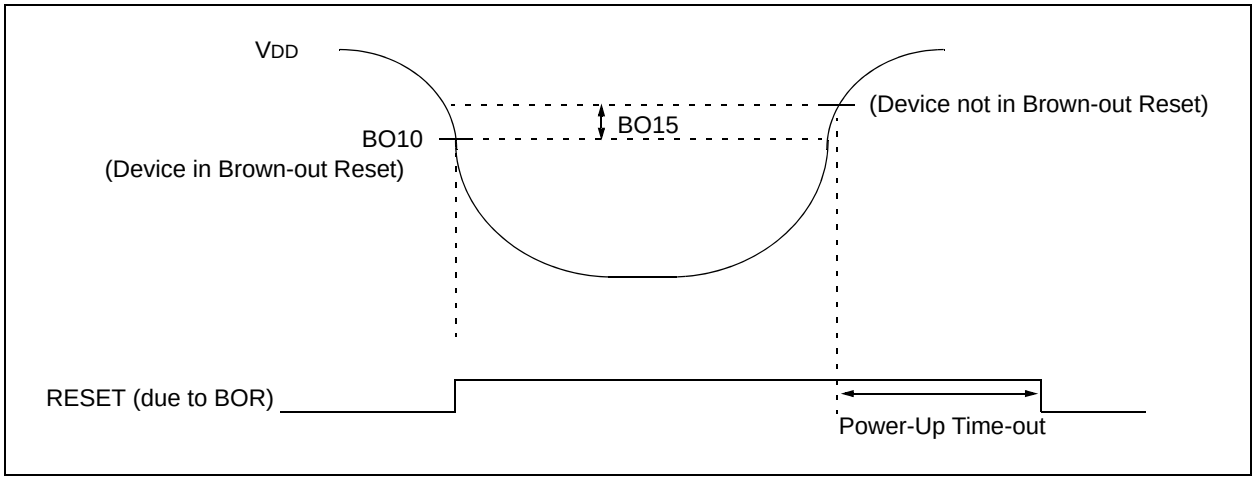


TABLE 20-11: ELECTRICAL CHARACTERISTICS: BOR

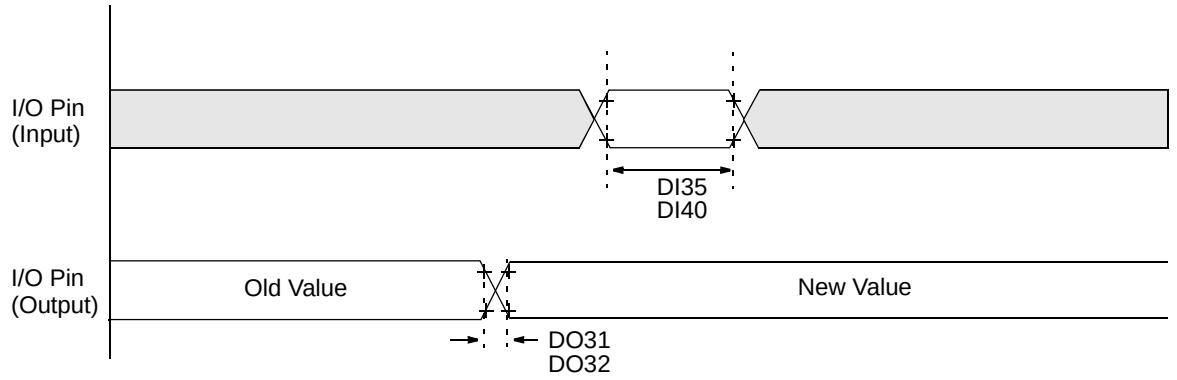
DC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended					
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
BO10	VBOR	BOR Voltage(2) on VDD transition high to low	BORV = 11(3)	—	—	—	V	Not in operating range
			BORV = 10	2.6	—	2.71	V	
			BORV = 01	4.1	—	4.4	V	
			BORV = 00	4.58	—	4.73	V	
BO15	VBHYS			—	5	—	mV	

Note 1: Data in “Typ” column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: These parameters are characterized but not tested in manufacturing.

3: 11 values not in usable operating range.

FIGURE 20-5: CLKO AND I/O TIMING CHARACTERISTICS



Note: Refer to Figure 20-3 for load conditions.

TABLE 20-20: CLKO AND I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			**Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated)** Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)(2)(3)**	**Min**	**Typ(4)**	**Max**	**Units**	**Conditions**
DO31	TIOR	Port output rise time	—	7	20	ns	
DO32	TIOF	Port output fall time	—	7	20	ns	
DI35	TINP	INTx pin high or low time (output)	20	—	—	ns	
DI40	TRBP	CNx high or low time (input)	2 TCY	—	—	ns	

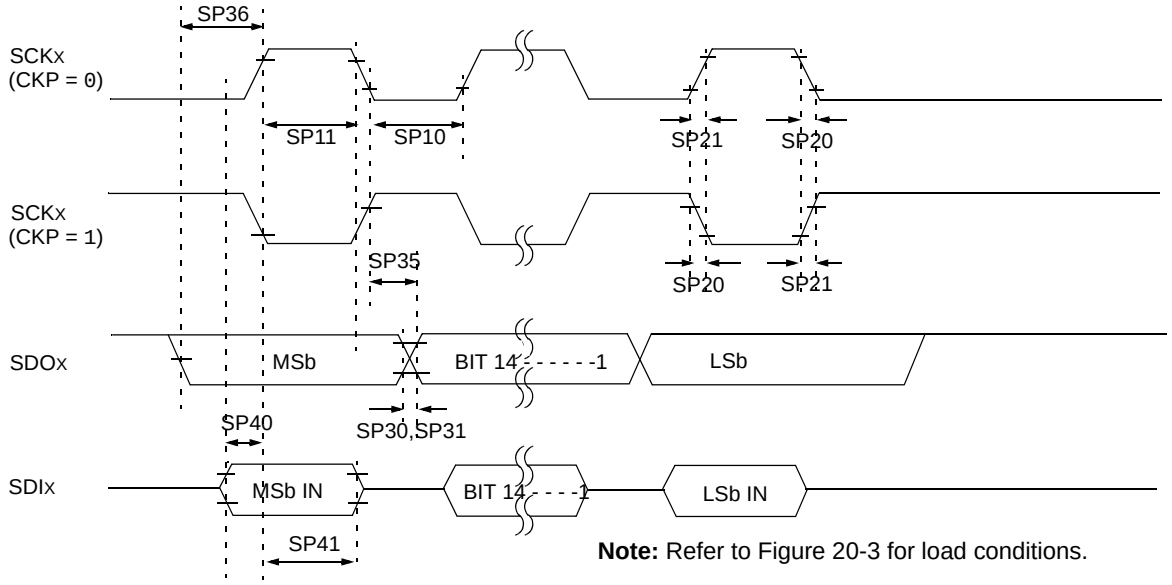
Note 1: These parameters are asynchronous events not related to any internal clock edges

2: Measurements are taken in RC mode and EC mode where CLKO output is 4 x TOSC.

3: These parameters are characterized but not tested in manufacturing.

4: Data in “Typ” column is at 5V, 25°C unless otherwise stated.

FIGURE 20-13: SPI MODULE MASTER MODE (CKE =1) TIMING CHARACTERISTICS



Note: Refer to Figure 20-3 for load conditions.

TABLE 20-30: SPI MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤TA ≤+85°C for Industrial -40°C ≤TA ≤+125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ(2)**	**Max**	**Units**	**Conditions**
SP10	TscL	SCKx output low time(3)	TCY/2	—	—	ns	—
SP11	TscH	SCKx output high time(3)	TCY/2	—	—	ns	—
SP20	TscF	SCKx output fall time(4)	—	—	—	ns	See parameter DO32
SP21	TscR	SCKx output rise time(4)	—	—	—	ns	See parameter DO31
SP30	TdoF	SDOx data output fall time(4)	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx data output rise time(4)	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx data output valid after SCKx edge	—	—	30	ns	—
SP36	TdoV2sc, TdoV2scL	SDOx data output setup to first SCKx edge	30	—	—	ns	—
SP40	TdiV2scH, TdiV2scL	Setup time of SDIx data input to SCKx edge	20	—	—	ns	—
SP41	TscH2diL, TscL2diL	Hold time of SDIx data input to SCKx edge	20	—	—	ns	—

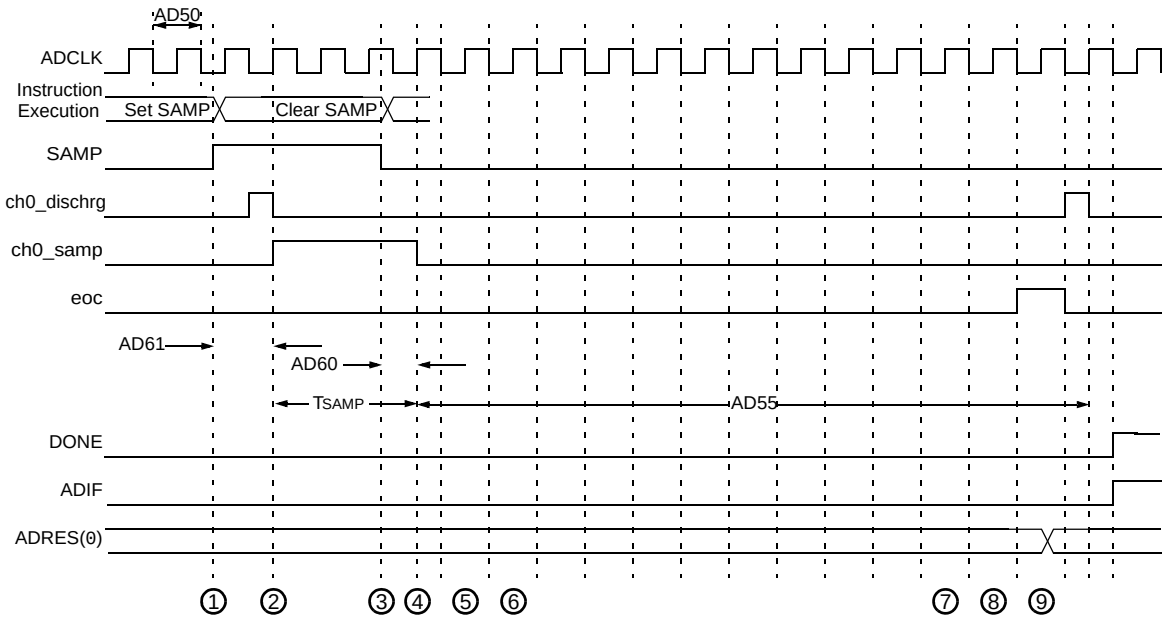
Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in “Typ” column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCK is 100 ns. Therefore, the clock generated in master mode must not violate this specification.

4: Assumes 50 pF load on all SPI pins.

FIGURE 20-21: 12-BIT A/D CONVERSION TIMING CHARACTERISTICS (ASAM = 0, SSRC = 000)



1 - Software sets ADCON. SAMP to start sampling.

2 - Sampling starts after discharge period.
TSAMP is described in **Section 18. "12-bit A/D Converter"** in the *dsPIC30F Family Reference Manual* (DS70046).

3 - Software clears ADCON. SAMP to Start conversion.

4 - Sampling ends, conversion sequence starts.

5 - Convert bit 11.

6 - Convert bit 10.

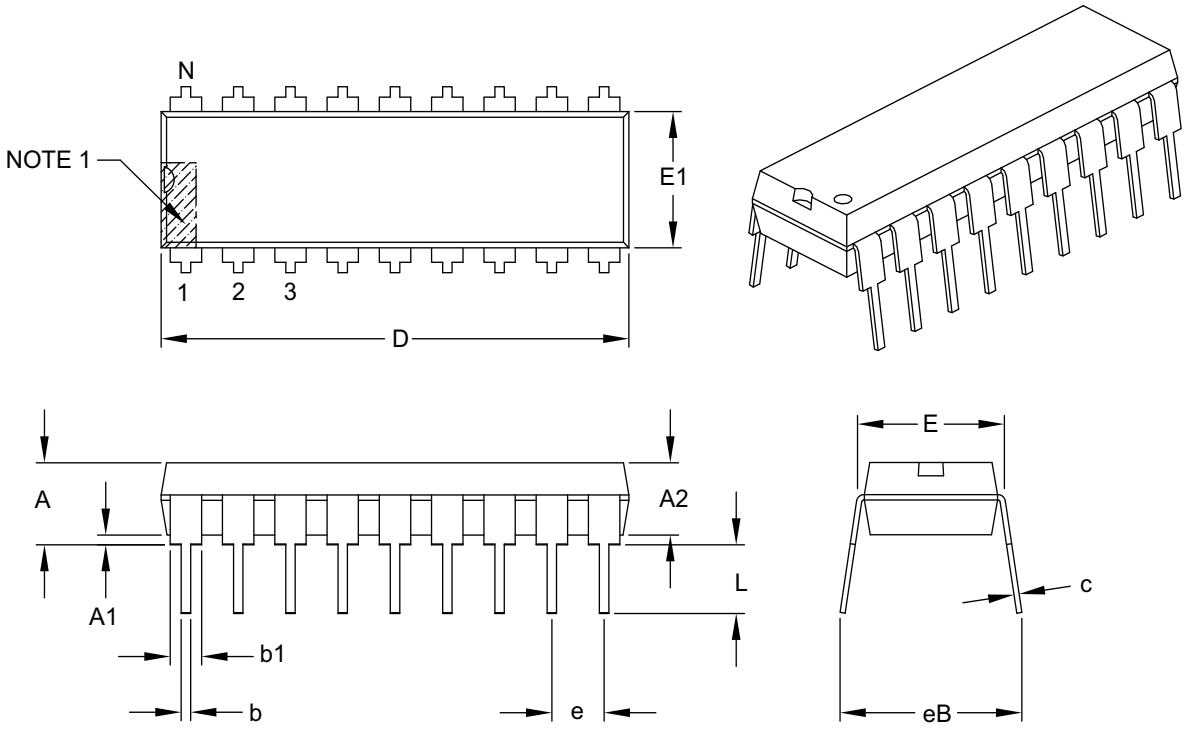
7 - Convert bit 1.

8 - Convert bit 0.

9 - One TAD for end of conversion.

18-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		18	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.300	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.880	.900	.920
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.014
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-007B